Next-gen Fan-out Interconnect for Chiplets and Beyond

Craig Bishop

CTO, Deca Technologies

January 24th, 2023

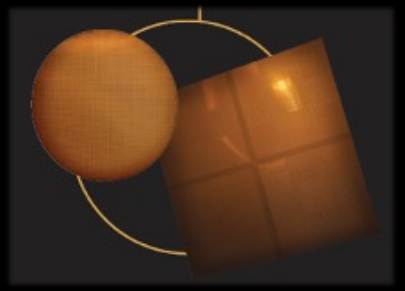
Outline

- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

Outline

- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

Company Introduction



2009 — TTLA #1

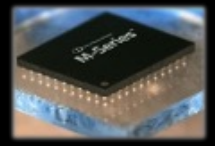
CYPRESS EMBEDDED IN TOMORROW™ & SUNPOWER

Founding of Deca USA & Philippines

Initial Activities
- Factory & technology development
- WLCSP for validity
- M-Series & Adaptive Patterning creation

2013 — TTLA #1

M-Series & Adaptive Patterning Introduced



& Adaptive Patterning

Technology Introduction
- Won best paper IWLPC 2013
- Initial M-Series & Adaptive Patterning customers engage

2016 — TTLA #1

Qualcomm & ASE GROUP

Qualcomm Adopts & ASE Becomes 1st TTLA Licensee

2nd Round Investors
- Leading customer
- Industry's #1 OSAT

2020 — TTLA #2

Nepes Becomes 2nd TTLA Licensee

nepes

3rd Round Investment
- Factory acquisition
- Equity investment

2021 — TTLA #3

Deca transformed into pure-play technology company

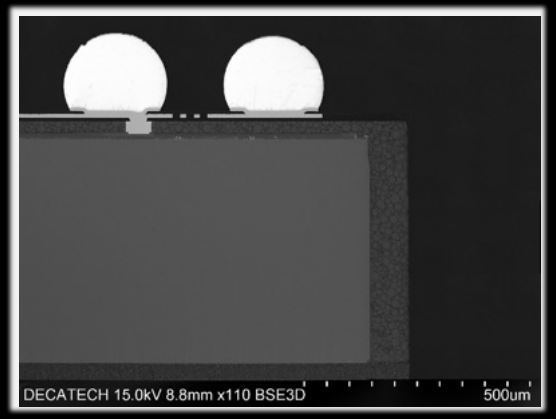
Market Success
- M-Series becomes #1 fan-out
- 600mm production starts
- SkyWater becomes 3rd TTLA licensee

skywater

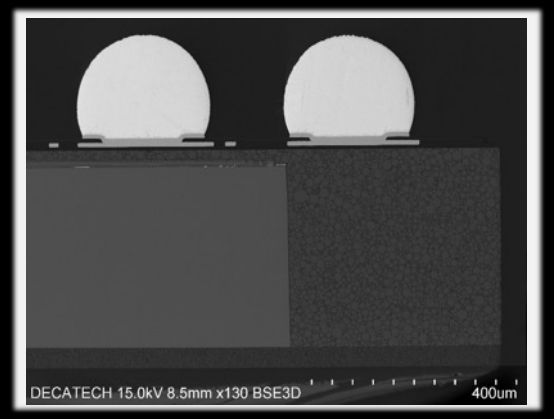
Our Name DECA 'represents our 10X thinking' inspired by *Greek déka* (δέκα)

M-Series™ is the #1 Fan-out Technology in the Industry

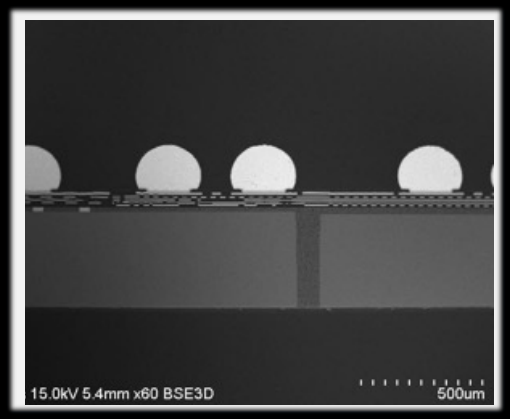
- Over 5 billion M-Series devices are in the field since production shipments began in 2018
- Main package types are protected fan-in and protected fan-out, single die, multi-die & modules



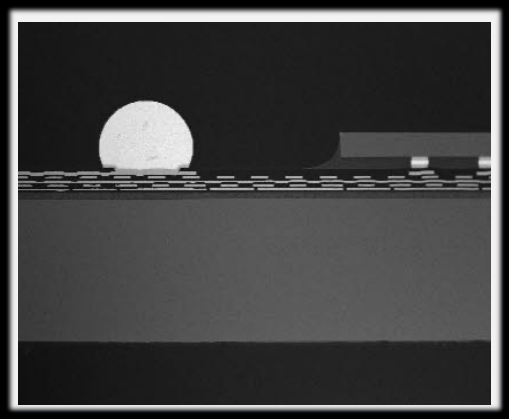
Protected Fan-In



Protected Fan-Out



Multi-Die



Five RDL + IPD

- Smartphones, handheld electronics & compute are major end applications (growing automotive adoption)
- Main devices types qualified include multiple forms of PMICs, Codecs, RF, CPU, GPU and APU
- Exceptional quality with < 0.01 DPM on 1st billion units shipped (0.01 DPM vs. baseline 30 DPM for conventional WLCSP)
- Significant production capacity installed in Taiwan, Philippines & Korea
  a) Nine production lines using 300mm wafer format (each line defined by LDI tool capacity)
  b) Three production line using 600mm panel format

DECA

Technology Partners & Licensees

Significant industry adoption through leading advanced packaging providers

CHIPS Act funding stimulating multiple US companies to consider new factory implementations

Existing Technology Partners & Licensees

1. ASE GROUP
   1. 300mm round (Taiwan)
   2. *600mm square (Taiwan) – likely in 2023*
2. nepes corporation
   3. 300mm round (Philippines)
   4. 600mm square (Korea) – continuing growth
3. skywater
   5. 200mm round (USA)
   6. *300mm or 600mm (USA) – likely in 2023 & beyond*

New Technology Partner Targets

(Currently in various stages of engagement)

Blue text represents signed preliminary agreements

4. **IDM #1**
   600mm square – 2023
   M-Series & Adaptive Patterning for broad array of package types
5. **IDM #2**
   600mm square – 2023
   M-Series & Adaptive Patterning for broad array of package types
6. **OEM #1**
   300mm round – 2023
   Interest in ultra-high density system module applications
7. **OEM #2**
   200mm round – 2023
   Interest in ultra-high density system module applications
8. **University #1**
   300mm round – 2023
   Interest in M-Series & Adaptive Patterning for advanced heterogeneous integration
9. **OSAT #3**
   600mm square – likely 2024
   Interest in M-Series & Adaptive Patterning for broad array of package types

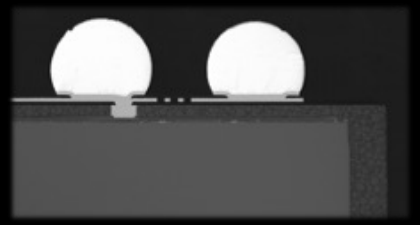
Deca's Technology – M-Series & Adaptive Patterning

- *M-Series is currently the industry's leading fan-out technology (in volume shipments)*
- #1 independent technology development & licensing company in the advanced packaging industry in 2021[1]

[1]*Fan-out WLP & PLP Technologies 2021- Markets & Technology Report, Yole Developpement, June 2021*

- 10X breakthroughs with M-Series™ & Adaptive Patterning®

1.



M-Series*

Chips first, chips up fan-out technology

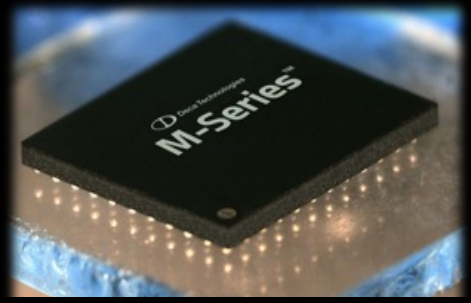
Gen 1 & Gen 2

2.

Adaptive Patterning™

Adaptive Patterning*

Real-time optimized design during manufacturing (every device on every wafer)



M-Series is now the industry's #1 fan-out technology

Over 5 million devices shipping per day

*> 140 patents issued & pending

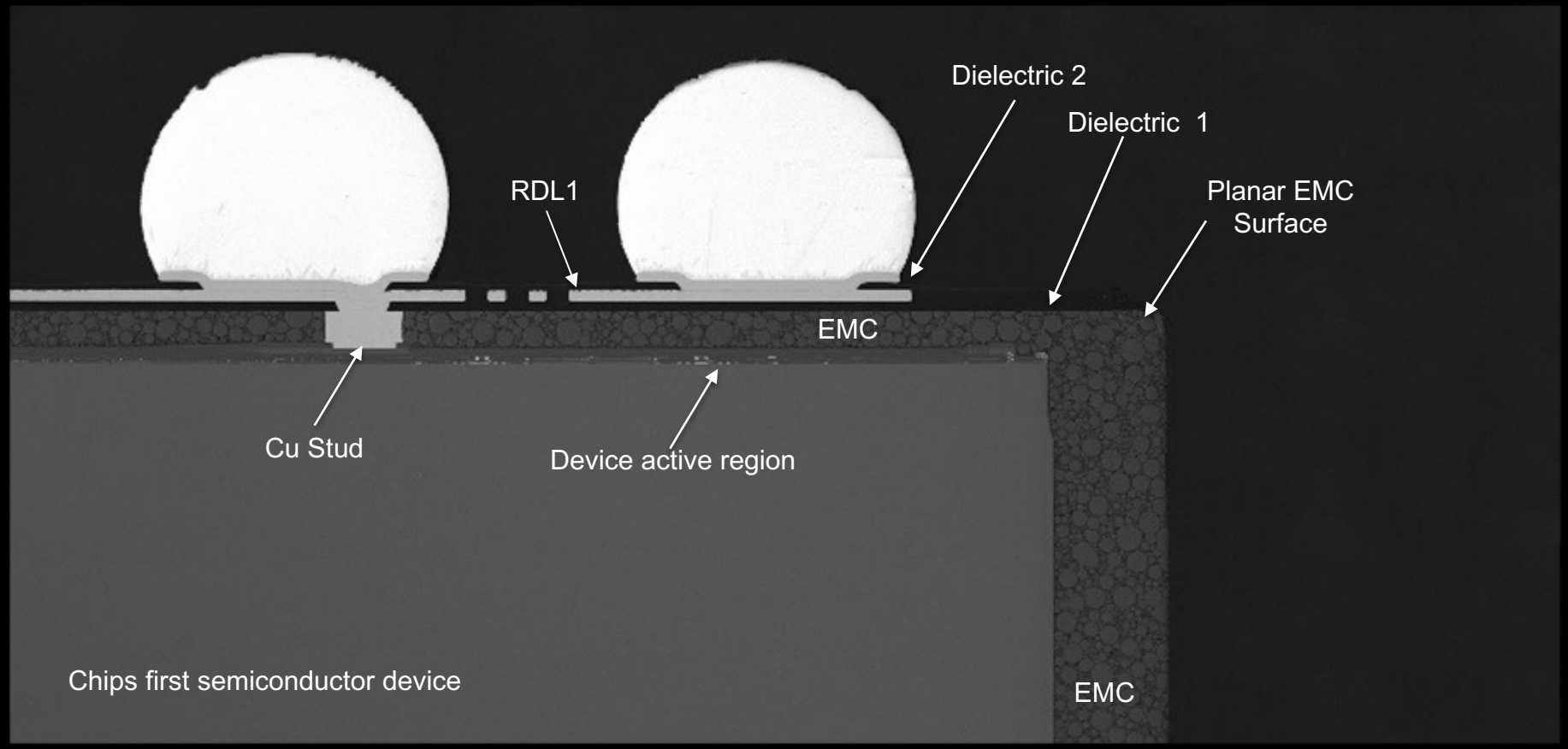
DECA

Outline

- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

Fan-out Fundamentals – A look at M-Series™

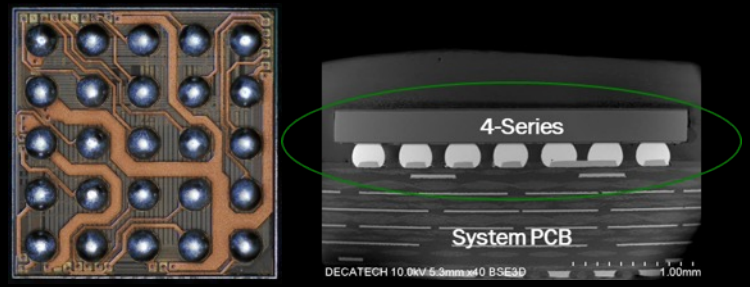
- Chips-first – die are embedded first and then interconnect is additively formed
- Chips-up – active die surface is encapsulated and then revealed
- Fully encapsulated – protection on all sides including active device region (EMC on 5 sides of chip)

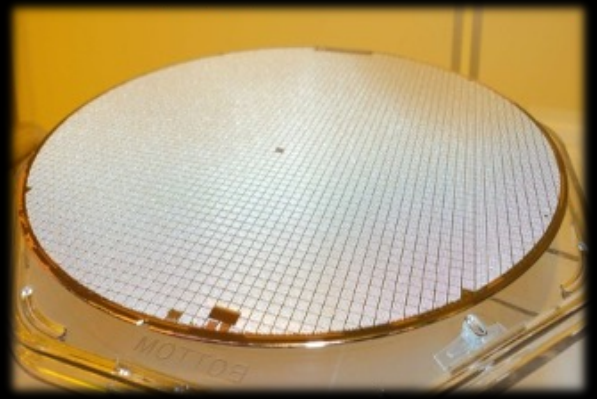


Fan-out originally driven by Smartphone industry

Fan-in WLCSP

- Smallest form-factor
- Excellent electrical performance
- I/O limited to die area

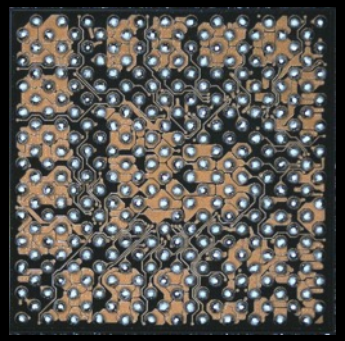


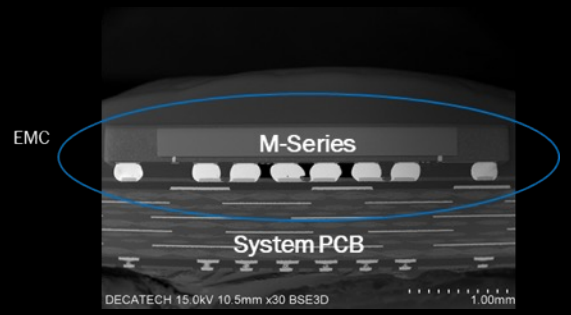


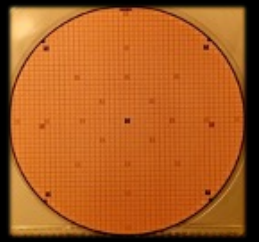
Wafer-level processing, 200mm or 300mm

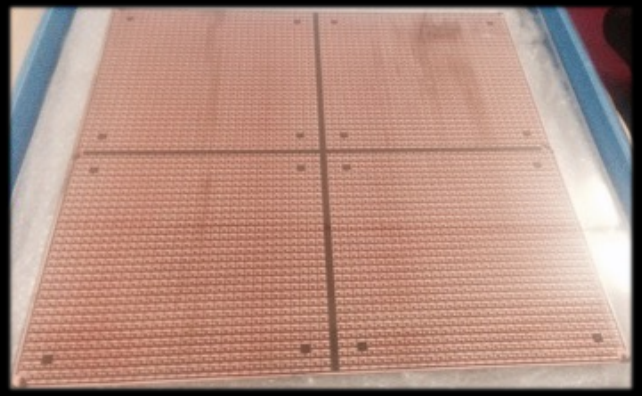
Fan-out WLP & PLP

- Expand I/O beyond die area
- Integrate multiple die
- Scale up manufacturing





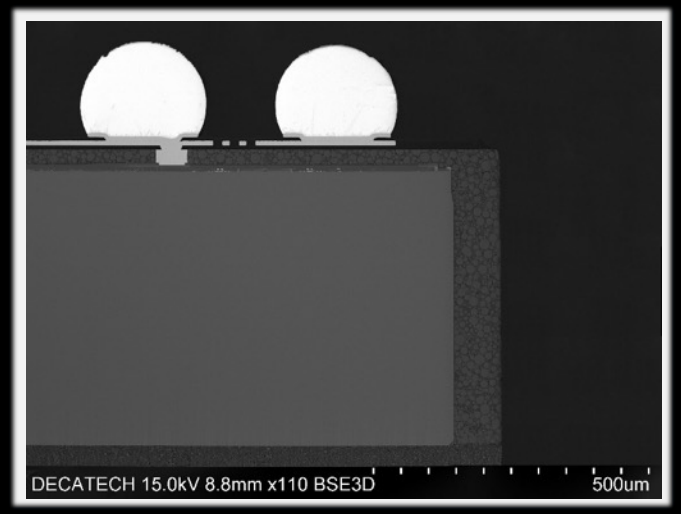




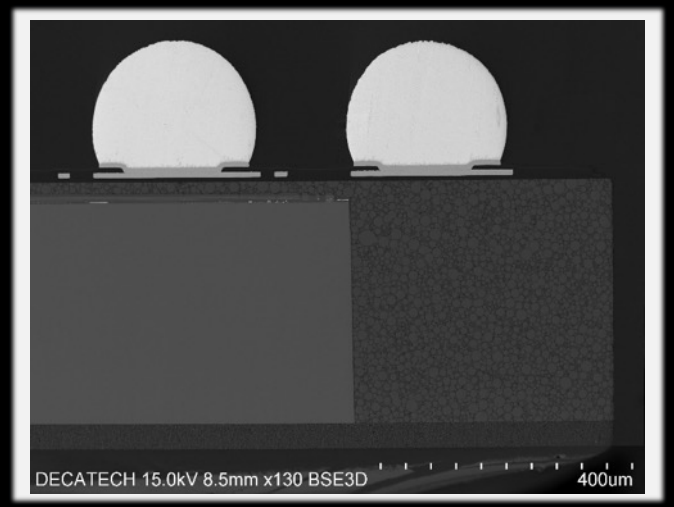
300mm wafer or 600mm panel processing

DECA

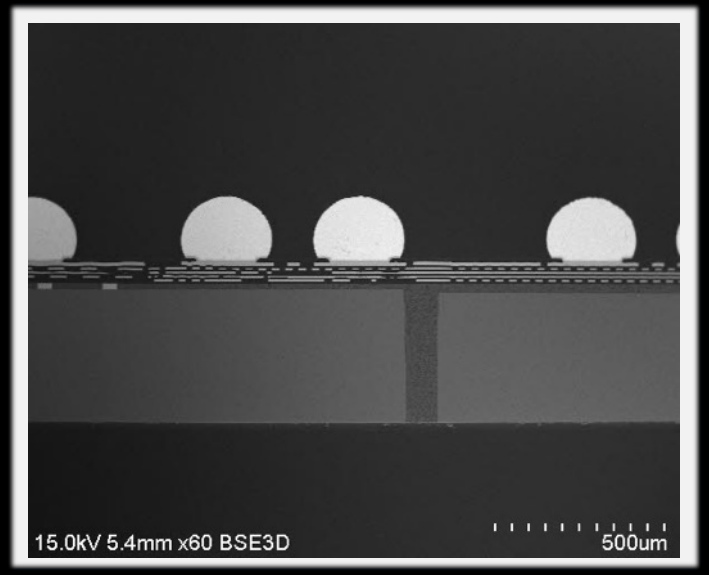
Fan-out Fundamentals – A look at M-Series™



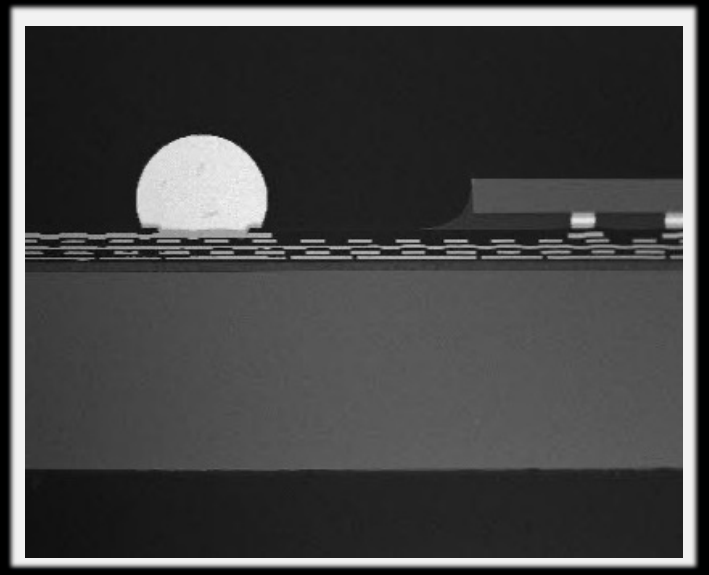
Protected Fan-In



Protected Fan-Out



Multi-Die



Five RDL + IPD

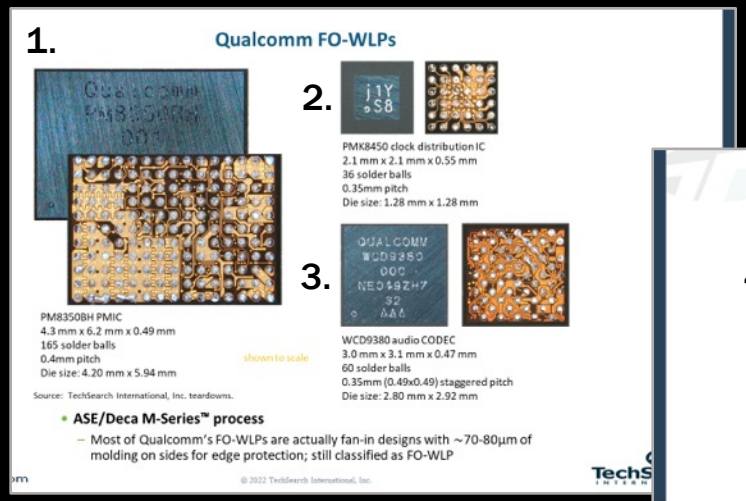
DECA

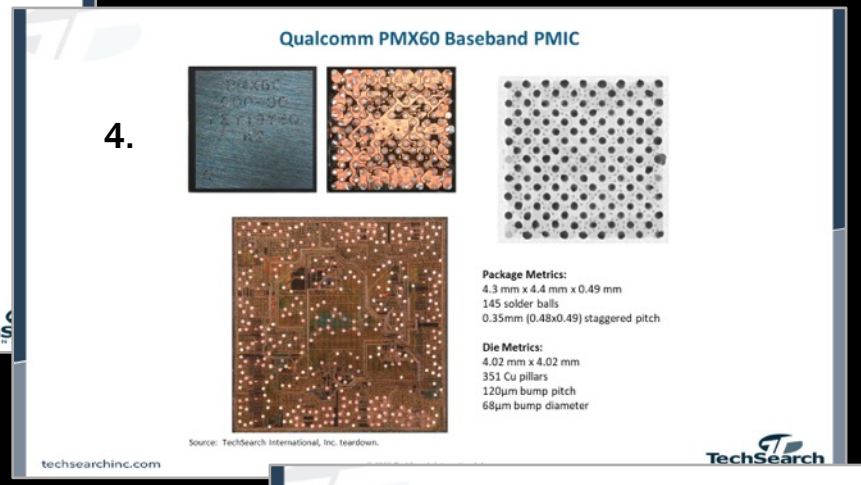
Outline

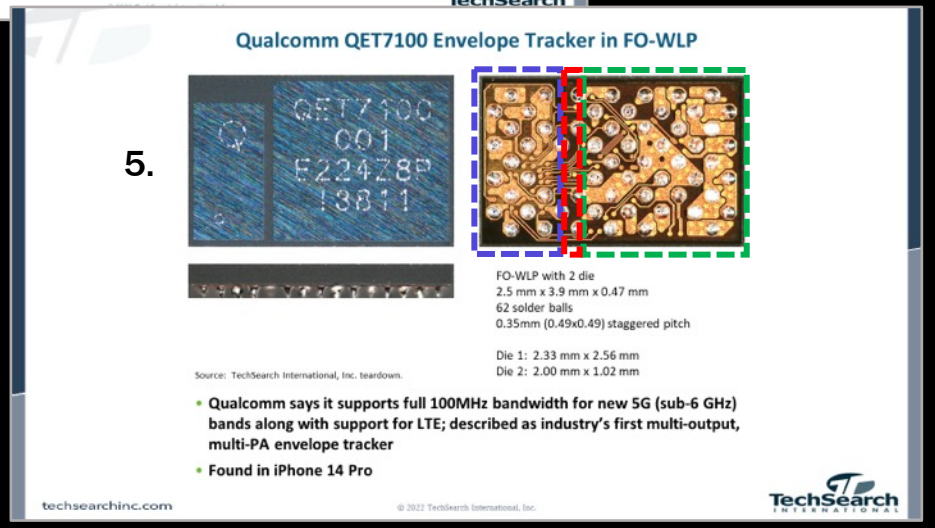
- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

M-Series™ Fan-out in iPhone 14

5 M-Series devices found in new Apple iPhone 14 teardown by TechSearch *(fan-out & protected fan-in)*





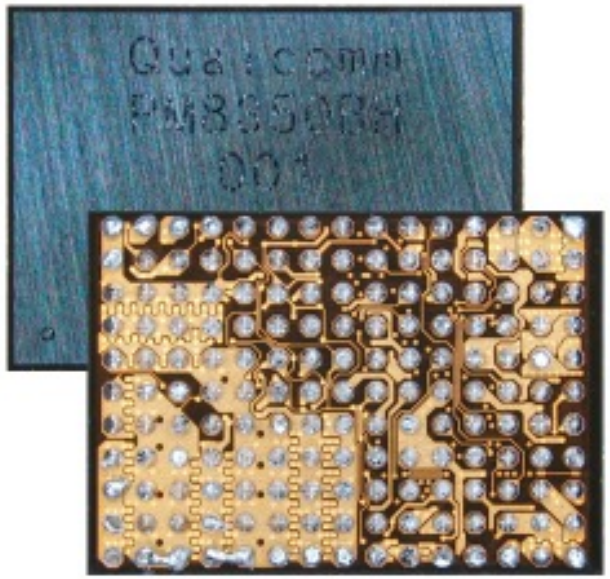


DECA

Traditional Fan-out Applications

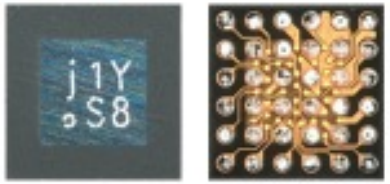
- PMICs
- CODECs
- Clocks
- RF

Qualcomm FO-WLPs



PM8350BH PMIC
4.3 mm x 6.2 mm x 0.49 mm
165 solder balls
0.4mm pitch
Die size: 4.20 mm x 5.94 mm

shown to scale



PMK8450 clock distribution IC
2.1 mm x 2.1 mm x 0.55 mm
36 solder balls
0.35mm pitch
Die size: 1.28 mm x 1.28 mm

WCD9380 audio CODEC
3.0 mm x 3.1 mm x 0.47 mm
60 solder balls
0.35mm (0.49x0.49) staggered pitch
Die size: 2.80 mm x 2.92 mm

Source: TechSearch International, Inc. teardowns.

- **ASE/Deca M-Series™ process**
  - Most of Qualcomm's FO-WLPs are actually fan-in designs with ~70-80µm of molding on sides for edge protection; still classified as FO-WLP

© 2022 TechSearch International, Inc.

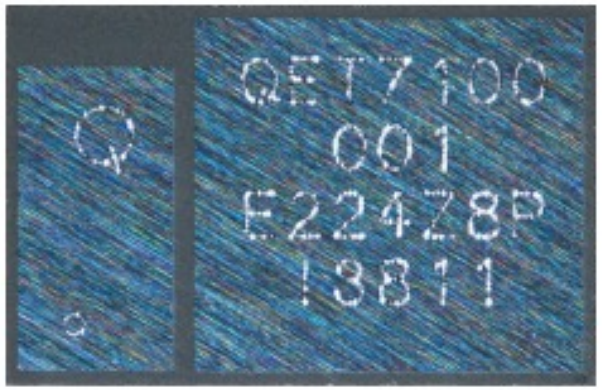
TechSearch INTERNATIONAL

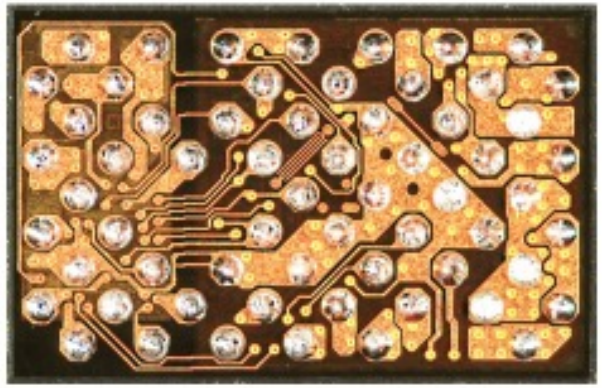
DECA

Traditional Fan-out Applications

- PMICs
- CODECs
- Clocks
- RF

Qualcomm QET7100 Envelope Tracker in FO-WLP





FO-WLP with 2 die
2.5 mm x 3.9 mm x 0.47 mm
62 solder balls
0.35mm (0.49x0.49) staggered pitch

Die 1: 2.33 mm x 2.56 mm
Die 2: 2.00 mm x 1.02 mm

Source: TechSearch International, Inc. teardown.

- **Qualcomm says it supports full 100MHz bandwidth for new 5G (sub-6 GHz) bands along with support for LTE; described as industry's first multi-output, multi-PA envelope tracker**
- **Found in iPhone 14 Pro**

ic.com
© 2022 TechSearch International, Inc.

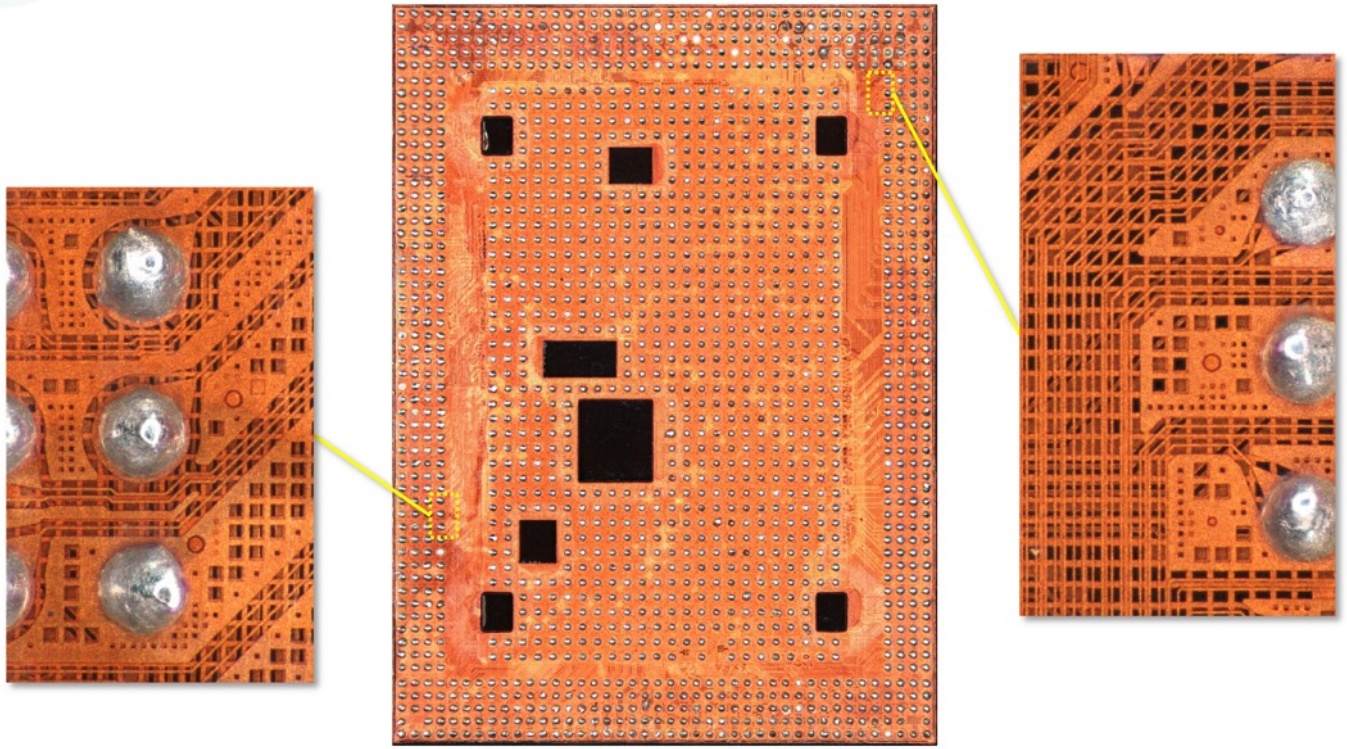
TechSearch INTERNATIONAL

DECA

Traditional Fan-out Applications

- **Mobile APU**

Apple A16 in iPhone 14 Pro



- **17.3mm x 12.7mm package size**
- **1,623 solder balls**
  - 7% more than on A15 (1,521)
  - 0.30mm pitch

- **Cu InFO RDLs**
  - 3 layers with ~5µm/8µm L/S
  - 1 additional layer at the die contacts

- **8 decoupling capacitor IPDs flip-chip attached to bottom**

techsearchinc.com

© 2022 TechSearch International, Inc.

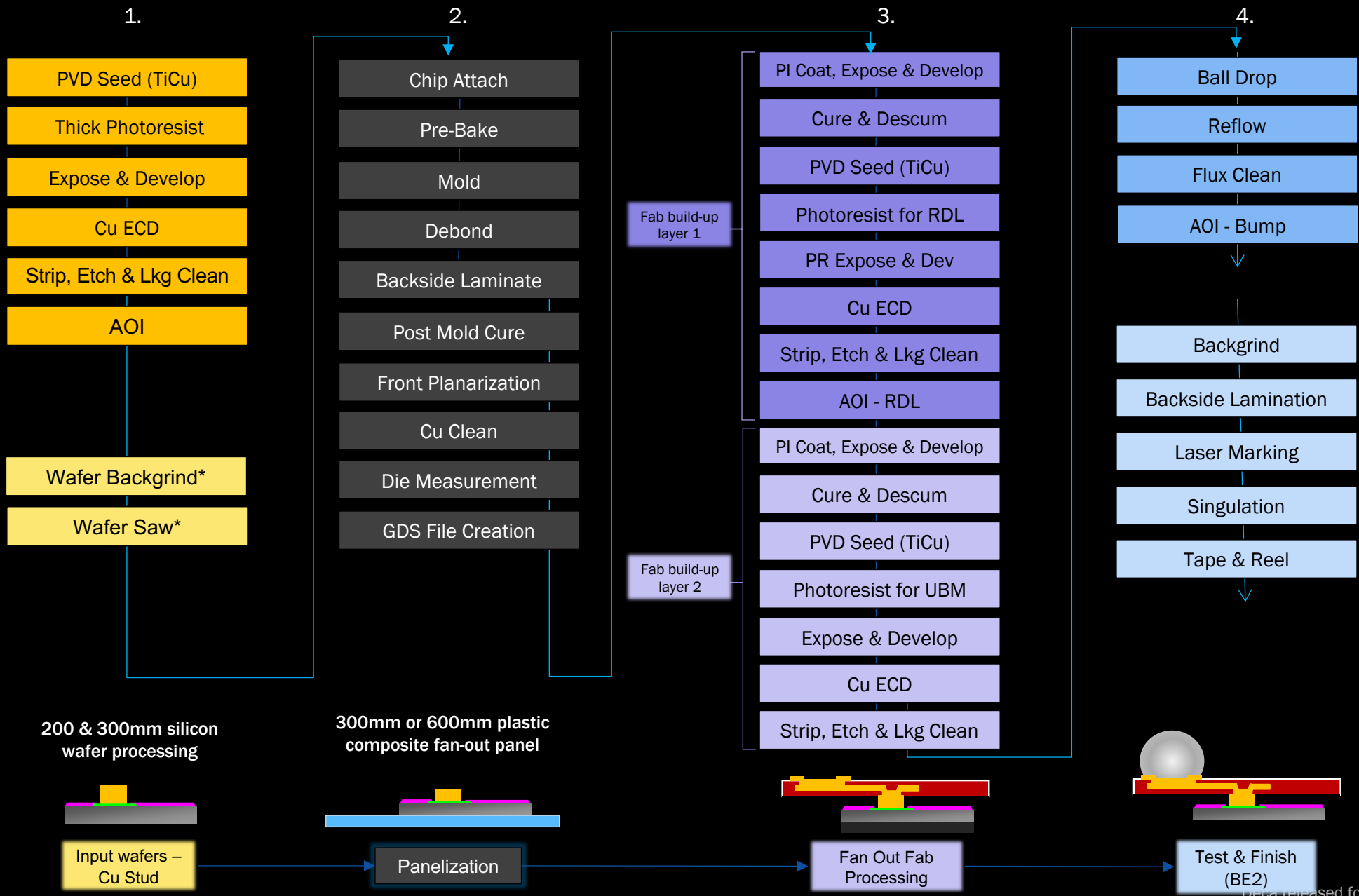
TechSearch INTERNATIONAL

DECA

Outline

- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

Process Flow – High Level Overview



Process Flow – High Level Overview

1.

PVD Seed (TiCu)

Thick Photoresist

Expose & Develop

Cu ECD

Strip, Etch & Lkg Clean

AOI

Wafer Backgrind*

Wafer Saw*

200 & 300mm silicon wafer processing

Input wafers – Cu Stud

2.

Chip Attach

Pre-Bake

Mold

Debond

Backside Laminate

Post Mold Cure

Front Planarization

Cu Clean

Die Measurement

GDS File Creation

300mm or 600mm plastic composite fan-out panel

Panelization

3.

Fab build-up layer 1

PI Coat, Expose & Develop

Cure & Descum

PVD Seed (TiCu)

Photoresist for RDL

PR Expose & Dev

Cu ECD

Strip, Etch & Lkg Clean

AOI - RDL

Fab build-up layer 2

PI Coat, Expose & Develop

Cure & Descum

PVD Seed (TiCu)

Photoresist for UBM

Expose & Develop

Cu ECD

Strip, Etch & Lkg Clean

Fan Out Fab Processing

4.

Ball Drop

Reflow

Flux Clean

AOI - Bump

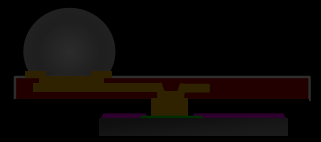
Backgrind

Backside Lamination

Laser Marking

Singulation

Tape & Reel



Test & Finish (BE2)

DECA

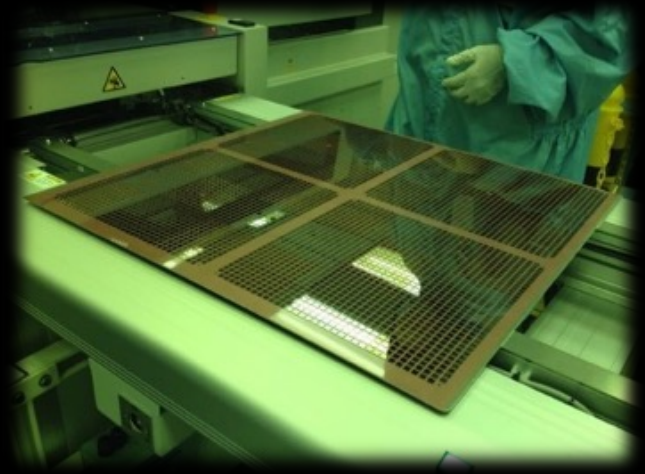
DECA released for Chiplet Summit 2023

Chip-attach

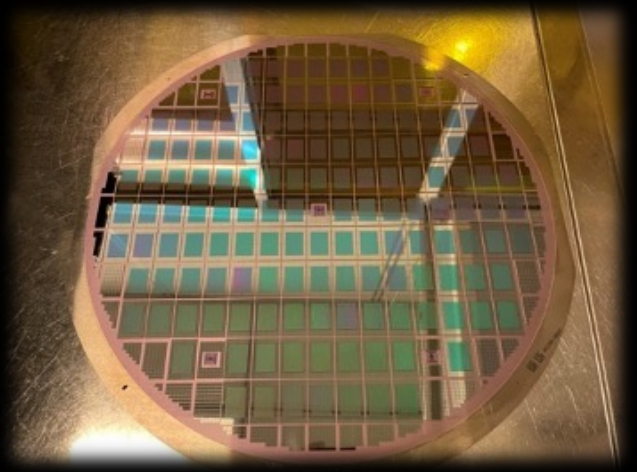
Panelization Process

- Chip Attach
- Pre-Bake
- **Mold**
- Debond
- Backside Laminate
- Post Mold Cure
- Front Planarization
- Cu Clean
- Die Measurement
- GDS File Creation

300mm + 600mm chip-attach machine



600mm post chip attach



300mm post chip attach

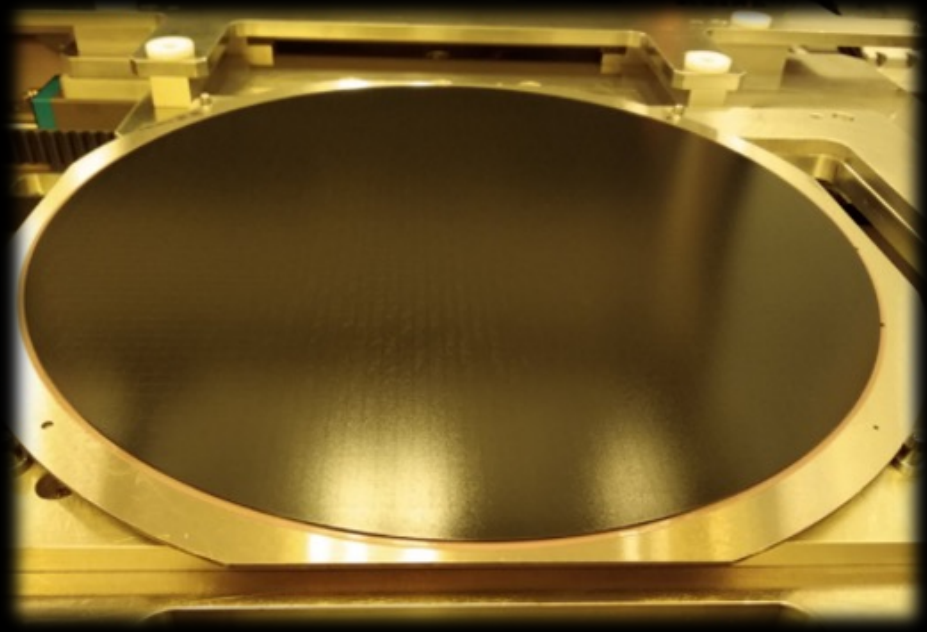
DECA

Molding

Panelization Process

- Chip Attach
- Pre-Bake
- **Mold**
- Debond
- Backside Laminate
- Post Mold Cure
- Front Planarization
- Cu Clean
- Die Measurement
- GDS File Creation

300mm panel after mold dispense



300mm panel after molding

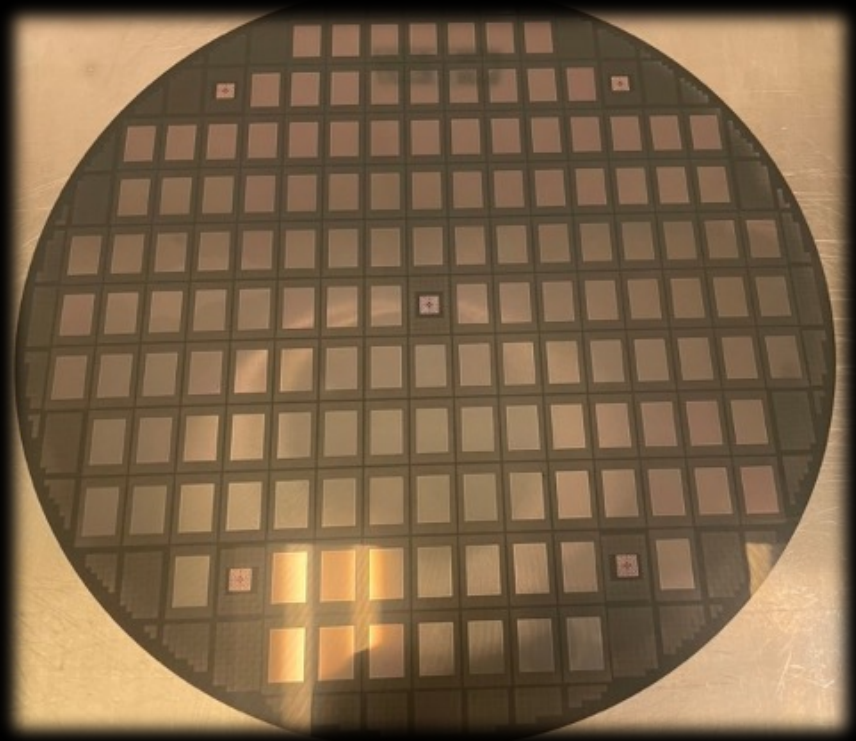
DECA

Front planarization & Cu stud reveal

Panelization Process

- Chip Attach
- Pre-Bake
- Mold
- Debond
- Backside Laminate
- Post Mold Cure
- **Front Planarization**
- Cu Clean
- Die Measurement
- GDS File Creation

Front-grind machine with 300mm + 600mm chuck



300mm panel after front-grind

DECA

Process Flow – High Level Overview

1.

PVD Seed (TiCu)

Thick Photoresist

Expose & Develop

Cu ECD

Strip, Etch & Lkg Clean

AOI

Wafer Backgrind*

Wafer Saw*

200 & 300mm silicon wafer processing

Input wafers – Cu Stud

2.

Chip Attach

Pre-Bake

Mold

Debond

Backside Laminate

Post Mold Cure

Front Planarization

Cu Clean

Die Measurement

GDS File Creation

300mm or 600mm plastic composite fan-out panel

Panelization

3.

Fab build-up layer 1

PI Coat, Expose & Develop

Cure & Descum

PVD Seed (TiCu)

Photoresist for RDL

PR Expose & Dev

Cu ECD

Strip, Etch & Lkg Clean

AOI - RDL

Fab build-up layer 2

PI Coat, Expose & Develop

Cure & Descum

PVD Seed (TiCu)

Photoresist for UBM

Expose & Develop

Cu ECD

Strip, Etch & Lkg Clean

Fan Out Fab Processing

4.

Ball Drop

Reflow

Flux Clean

AOI - Bump

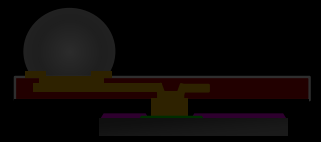
Backgrind

Backside Lamination

Laser Marking

Singulation

Tape & Reel



Test & Finish (BE2)

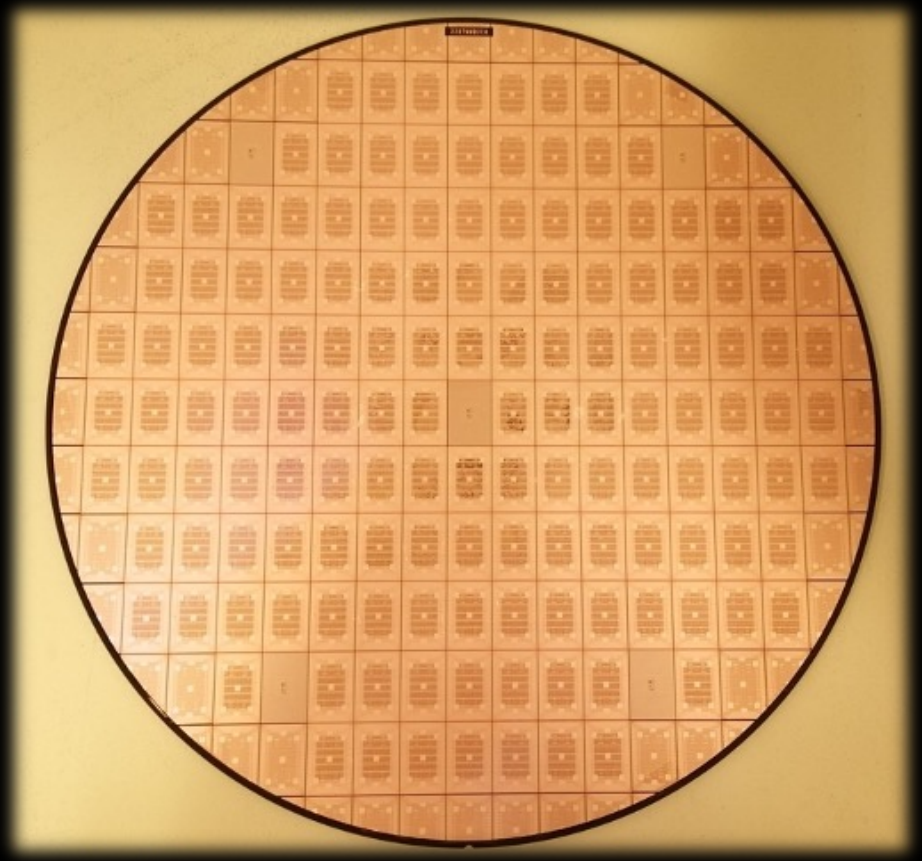
DECA

Deca released for Chiplet Summit 2023

RDL Build-up

- PI Coat, Expose & Develop
- Cure & Descum
- PVD Seed (TiCu)
- Photoresist for RDL
- PR Expose & Dev
- Cu ECD
- Strip, Etch & Lkg Clean
- AOI - RDL
- PI Coat, Expose & Develop
- Cure & Descum
- PVD Seed (TiCu)
- Photoresist for UBM
- Expose & Develop
- Cu ECD
- Strip, Etch & Lkg Clean

Laser direct imaging (LDI) lithography machine



300mm with 5 RDLs built up

DECA

Process Flow – High Level Overview

1.

- PVD Seed (TiCu)
- Thick Photoresist
- Expose & Develop
- Cu ECD
- Strip, Etch & Lkg Clean
- AOI

- Wafer Backgrind*
- Wafer Saw*

200 & 300mm silicon wafer processing

Input wafers – Cu Stud

2.

- Chip Attach
- Pre-Bake
- Mold
- Debond
- Backside Laminate
- Post Mold Cure
- Front Planarization
- Cu Clean
- Die Measurement
- GDS File Creation

300mm or 600mm plastic composite fan-out panel

Panelization

3.

Fab build-up layer 1

- PI Coat, Expose & Develop
- Cure & Descum
- PVD Seed (TiCu)
- Photoresist for RDL
- PR Expose & Dev
- Cu ECD
- Strip, Etch & Lkg Clean
- AOI - RDL

Fab build-up layer 2

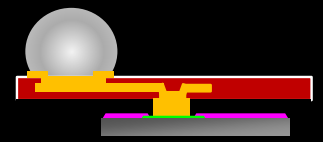
- PI Coat, Expose & Develop
- Cure & Descum
- PVD Seed (TiCu)
- Photoresist for UBM
- Expose & Develop
- Cu ECD
- Strip, Etch & Lkg Clean

Fan Out Fab Processing

4.

- Ball Drop
- Reflow
- Flux Clean
- AOI - Bump

- Backgrind
- Backside Lamination
- Laser Marking
- Singulation
- Tape & Reel

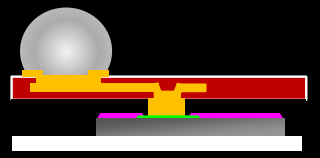


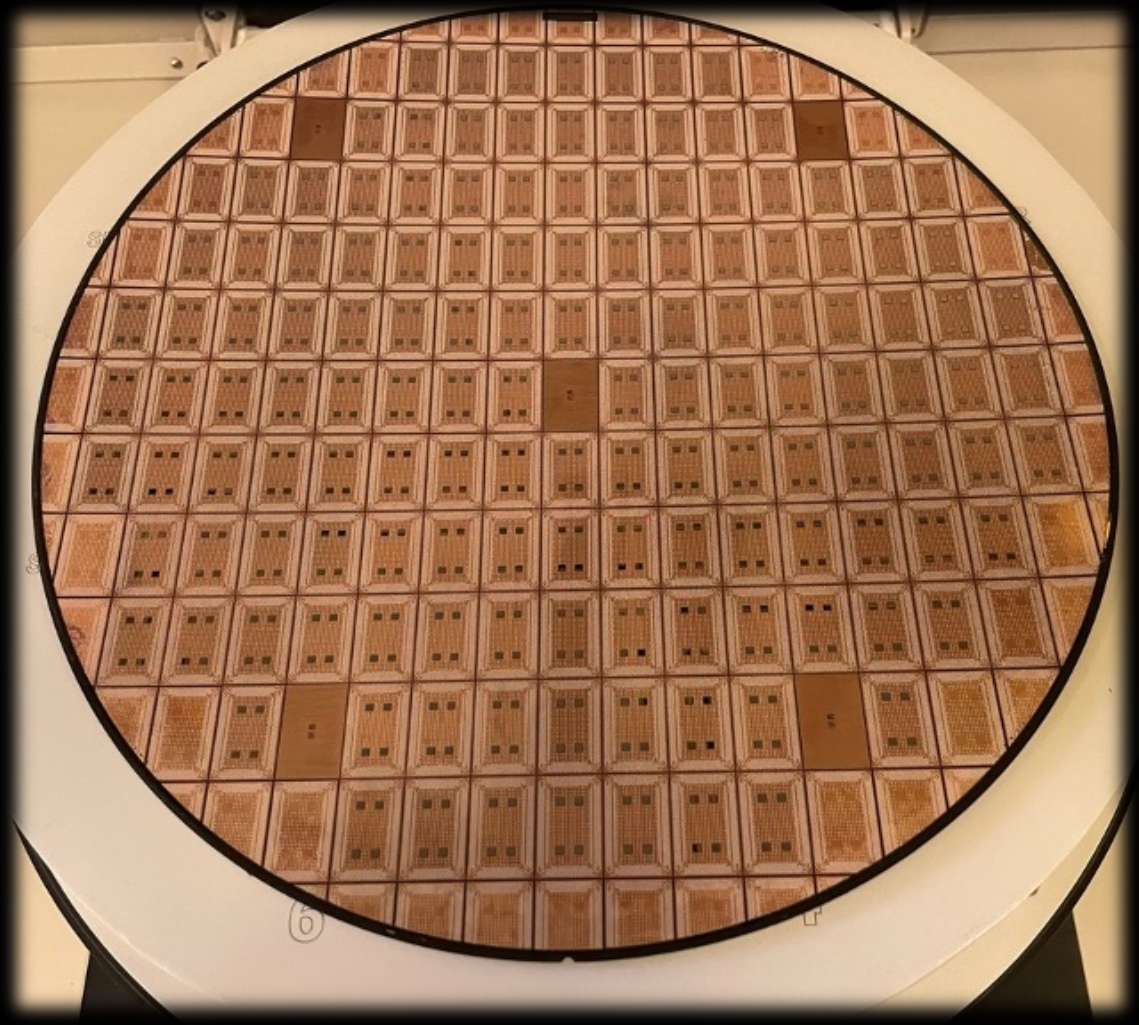
Test & Finish (BE2)

DECA

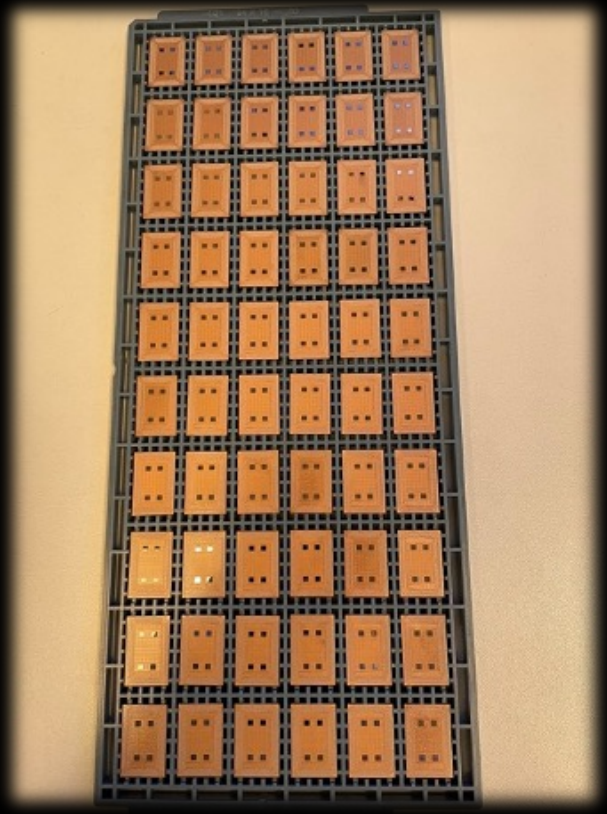
Finishing

- Ball Drop
- Reflow
- Flux Clean
- AOI - Bump
- Backgrind
- Backside Lamination
- Laser Marking
- Singulation
- Tape & Reel





300mm panel after ball-attach, marking, & singulation

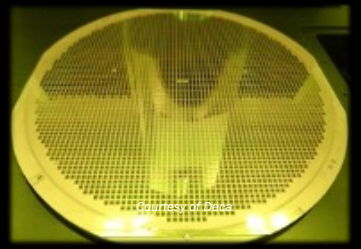


Final parts in tray

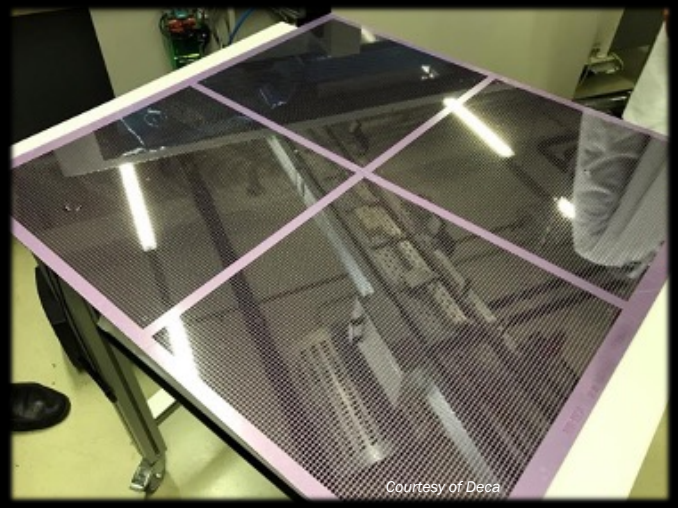
DECA

Scaling Up to Large Panel Format

After Chip Attach



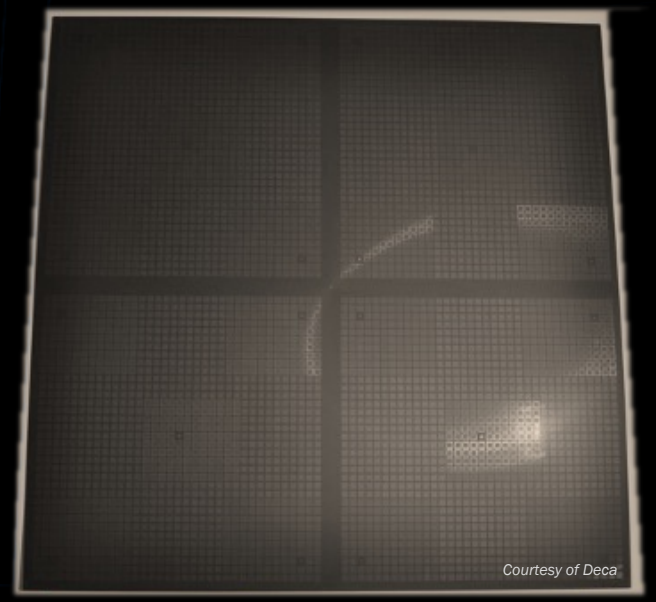
300mm round

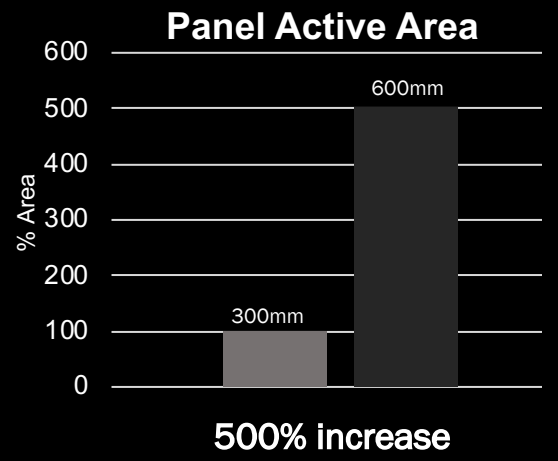


600mm x 600mm square

600mm delivers 5X increase in usable area per panel

After Panelization



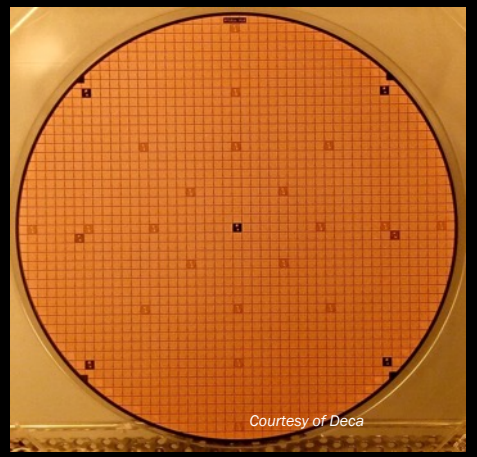


500% increase

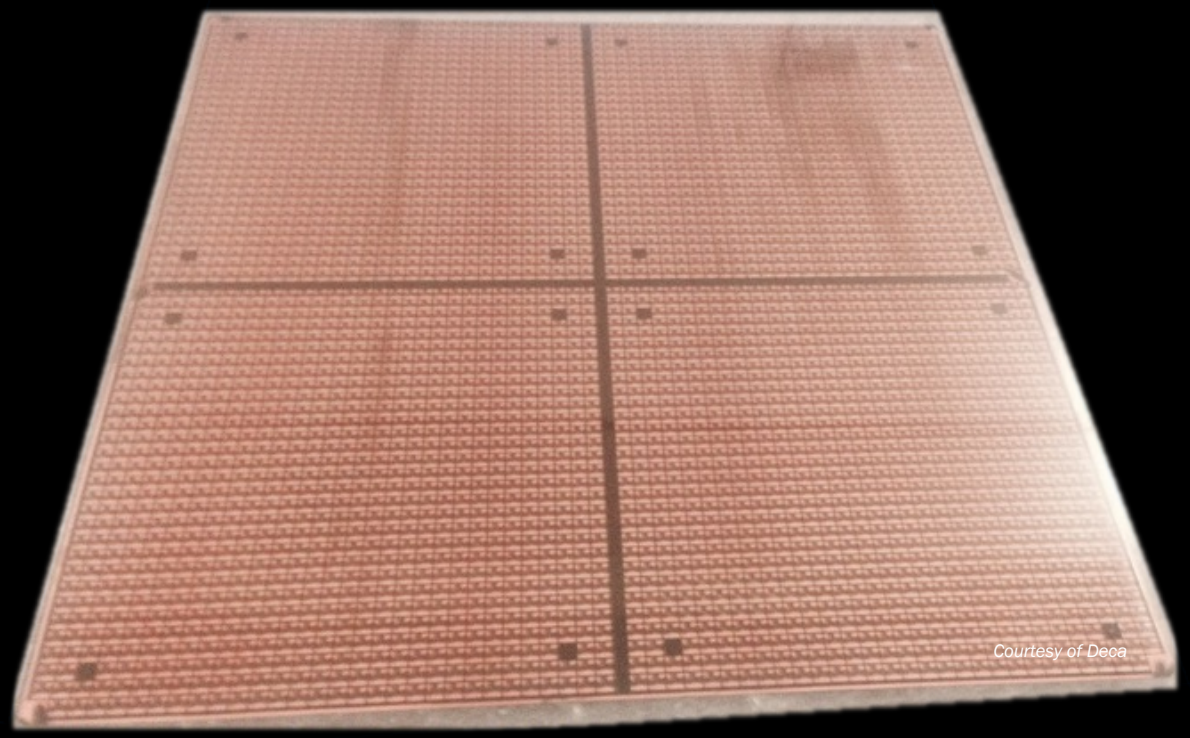
DECA

Scaling Up to Large Panel Format

300mm Wafer Production



Large Panel Production



600mm x 600mm square panel

600mm delivers

- *Estimated 25% reduction in the cost of capital per unit output*
- *Estimated 15% reduction in the cost of materials (higher utilization of PI & PR)*
- *Projected 20% overall cost reduction vs. 300mm round*

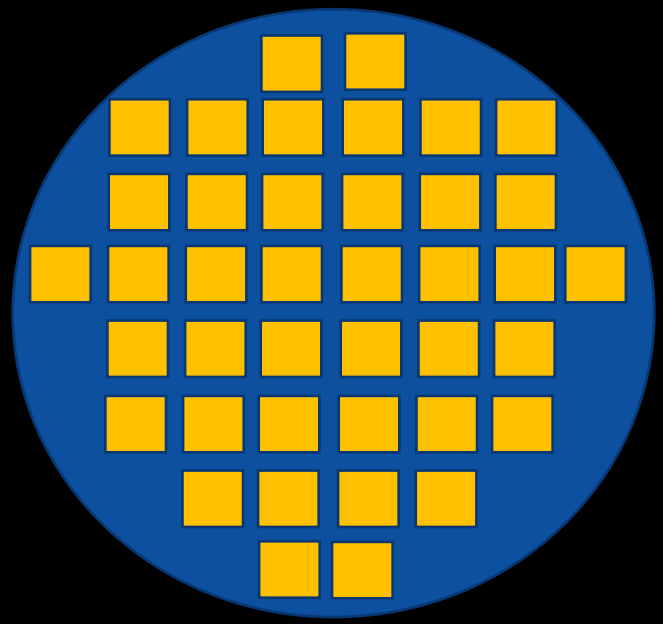
DECA

Outline

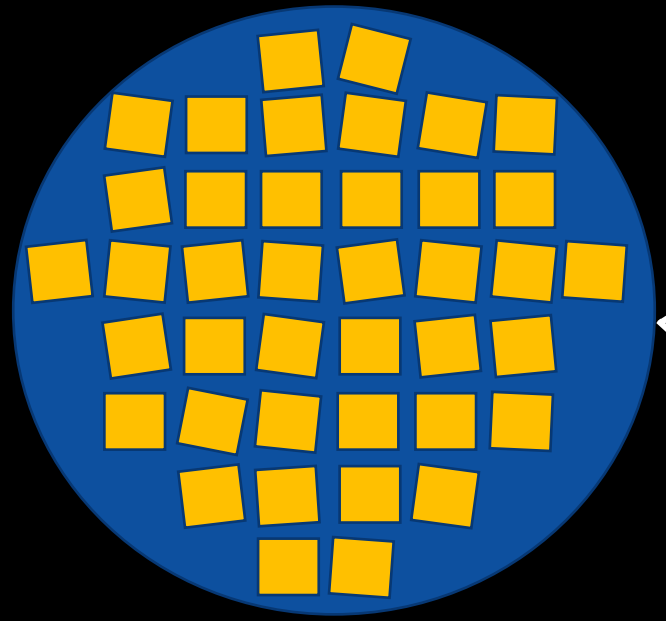
- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

Adaptive Patterning Motivation

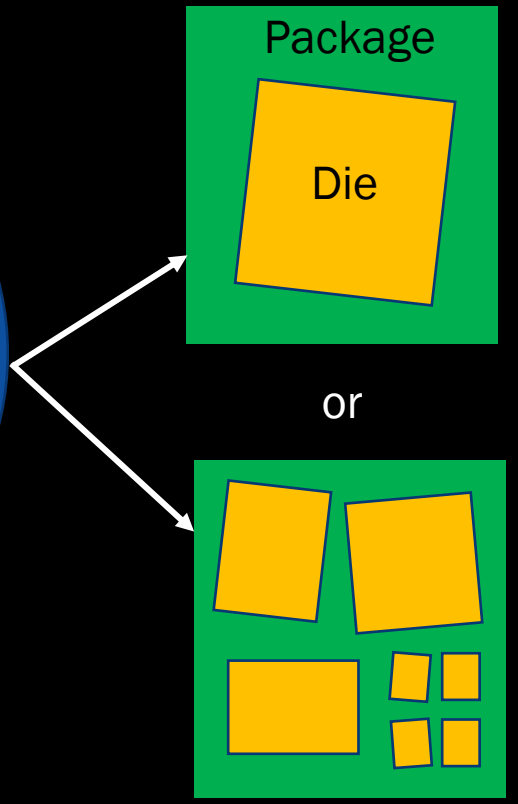
- In a stepper, each chip position is aligned and then exposed
- Some systems use area alignment, sacrificing accuracy
- Die by die alignment decreases through-put and multi-die packages are difficult to manage



Designed die locations on reconstituted wafer



Actual die locations after die attach and mold



Stepper = each package is an exposure aligned to the die offset

Multi-die or chiplets become difficult to manage

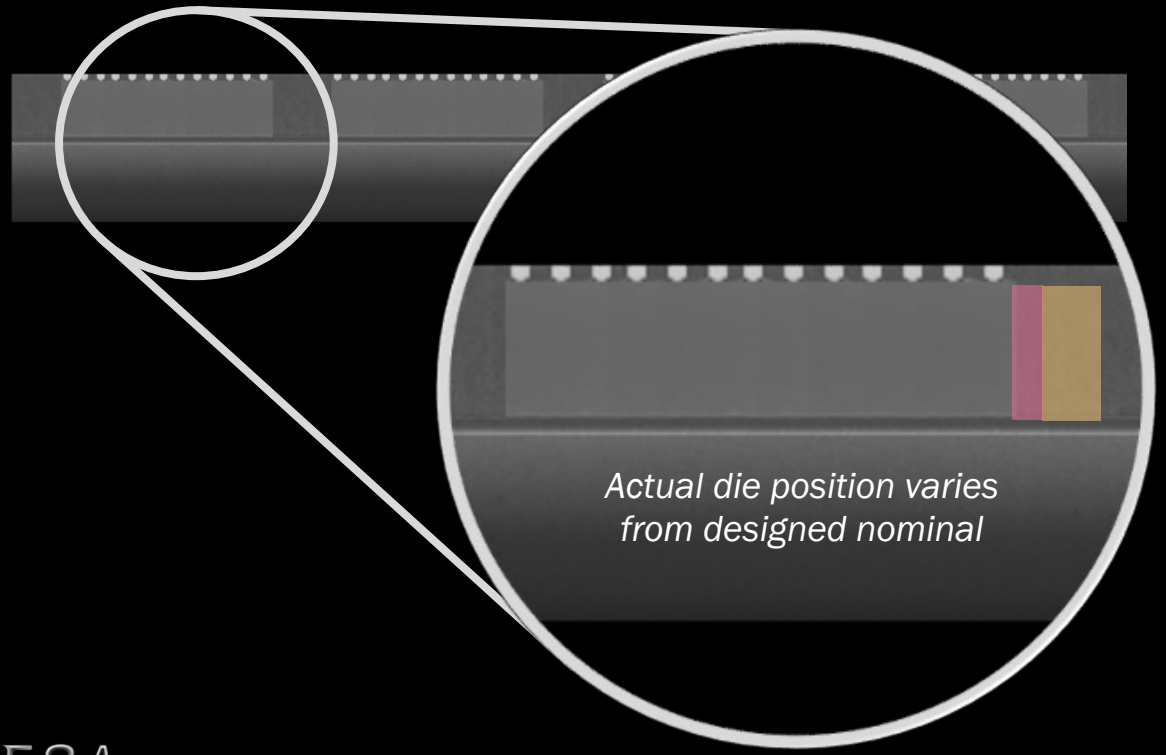
DECA

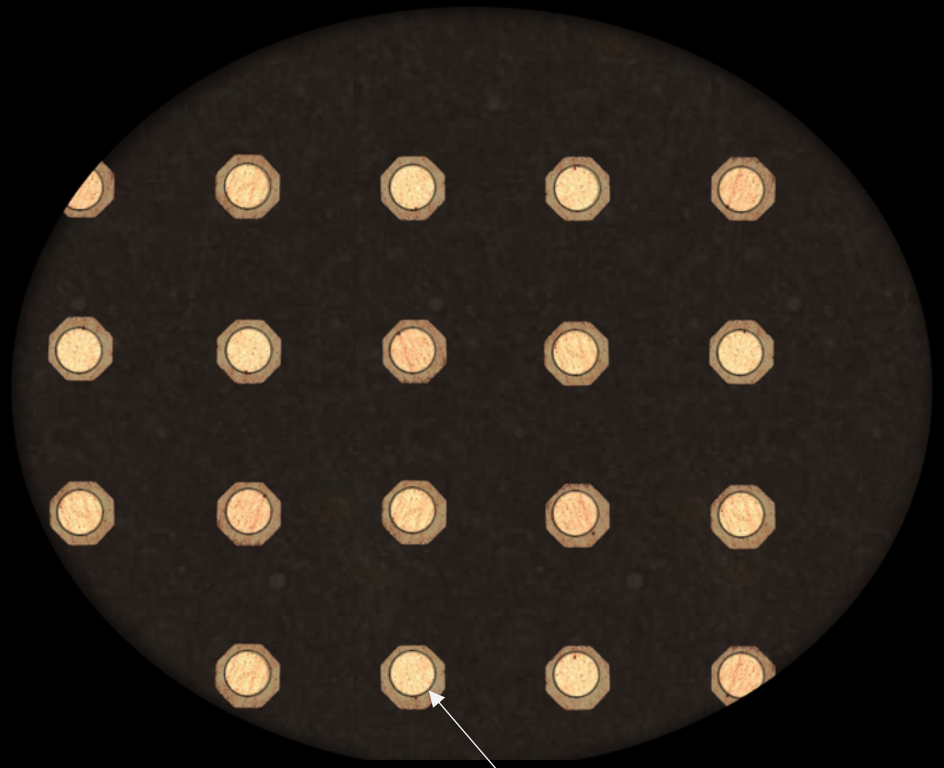
Why Adaptive Patterning?

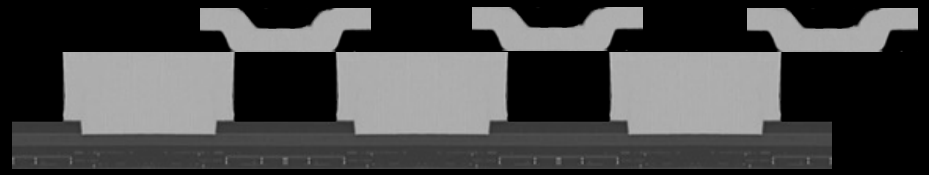
Shift Happens™

1. Variation in mechanical placement of die

2. Displacement during encapsulation (molding)





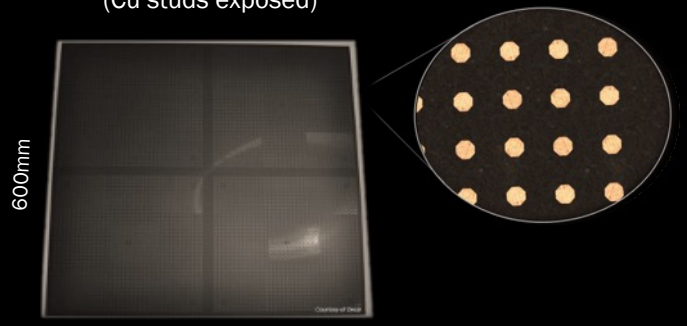


DECA

Adaptive Patterning – High level process overview

1. Measure actual die positions using high-speed optical scanner

Planarized molded panel
(Cu studs exposed)



High speed precision optical scanner

100% die measurement results

-112480	4.452	-75300	11.505	-0.07094
-112480	10.433	-60240	-5.664	0.07657
-112480	33.628	-45180	56.964	0.22095
-112480	17.823	-30120	-4.514	-0.06077
-112480	-0.121	-15060	7.748	0.14871
-112480	9.098	0	-2.332	0.15948
-112480	1.766	15060	1.994	0.04271
-112480	7.599	30120	9.588	0.05149
-112480	-2.226	45180	24.771	-0.01267
-112480	-1.291	60240	-13.819	0.04688
-112480	5.439	75300	-0.659	0.13094
-98420	0.127	-90360	7.939	-0.03352
-98420	3.053	-60240	-4.68	-0.01368

2. Generate unique lithography patterns for dielectric & photoresist layers during manufacturing (every device, every panel)

Actual die position
measurements

-112480	4.452	-75300	11.505	-0.07094
-112480	10.433	-60240	-5.664	0.07657
-112480	33.628	-45180	56.964	0.22095
-112480	17.823	-30120	-4.514	-0.06077
-112480	-0.121	-15060	7.748	0.14871
-112480	9.098	0	-2.332	0.15948
-112480	1.766	15060	1.994	0.04271
-112480	7.599	30120	9.588	0.05149
-112480	-2.226	45180	24.771	-0.01267
-112480	-1.291	60240	-13.819	0.04688
-112480	5.439	75300	-0.659	0.13094
-98420	0.127	-90360	7.939	-0.03352
-98420	3.053	-60240	-4.68	-0.01368

Real-time
Design-during-manufacturing

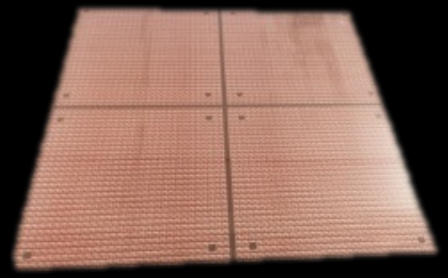
ENGINE

Lithography pattern for the whole
panel is dynamically generated

Mask-less LDI lithography system

High throughput scan

Unique lithography
pattern per panel

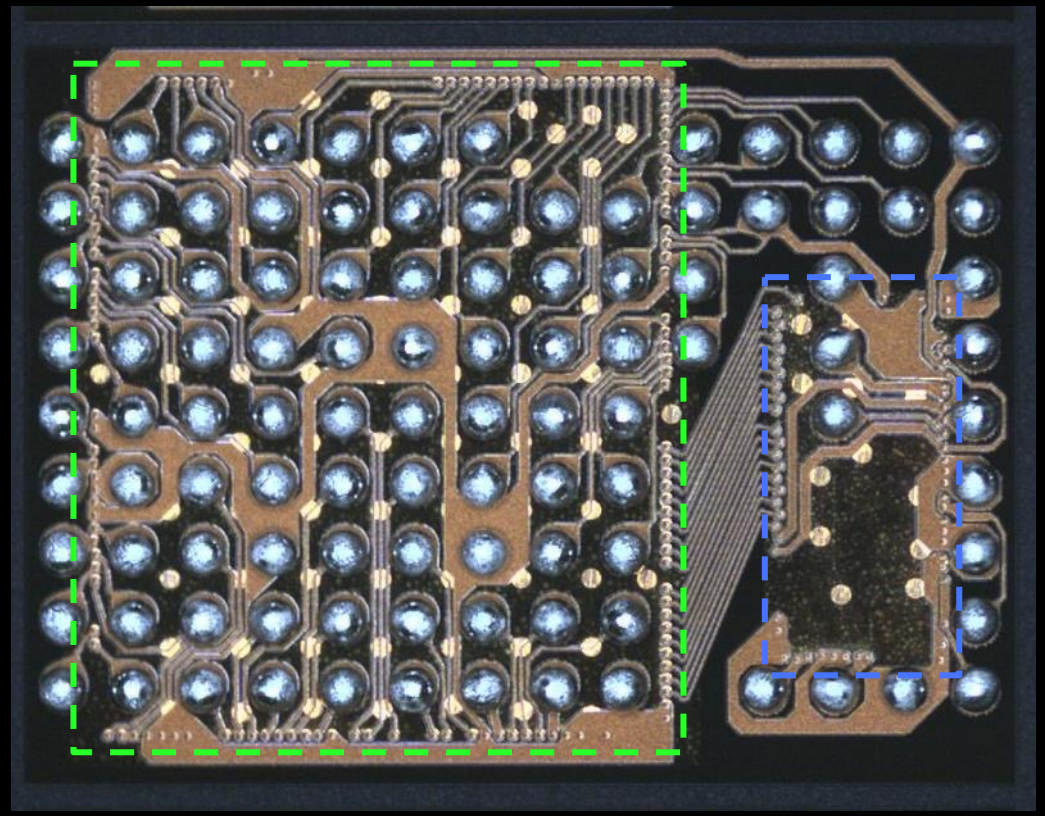


Unique optimized GDSII file for every panel
(no reticle size limitations)

Multi-mode Adaptive Patterning

IoT Module – 2 chips

- High performance MCU – 40nm
- Bluetooth radio – 55nm



Package 5.0 x 3.8 mm

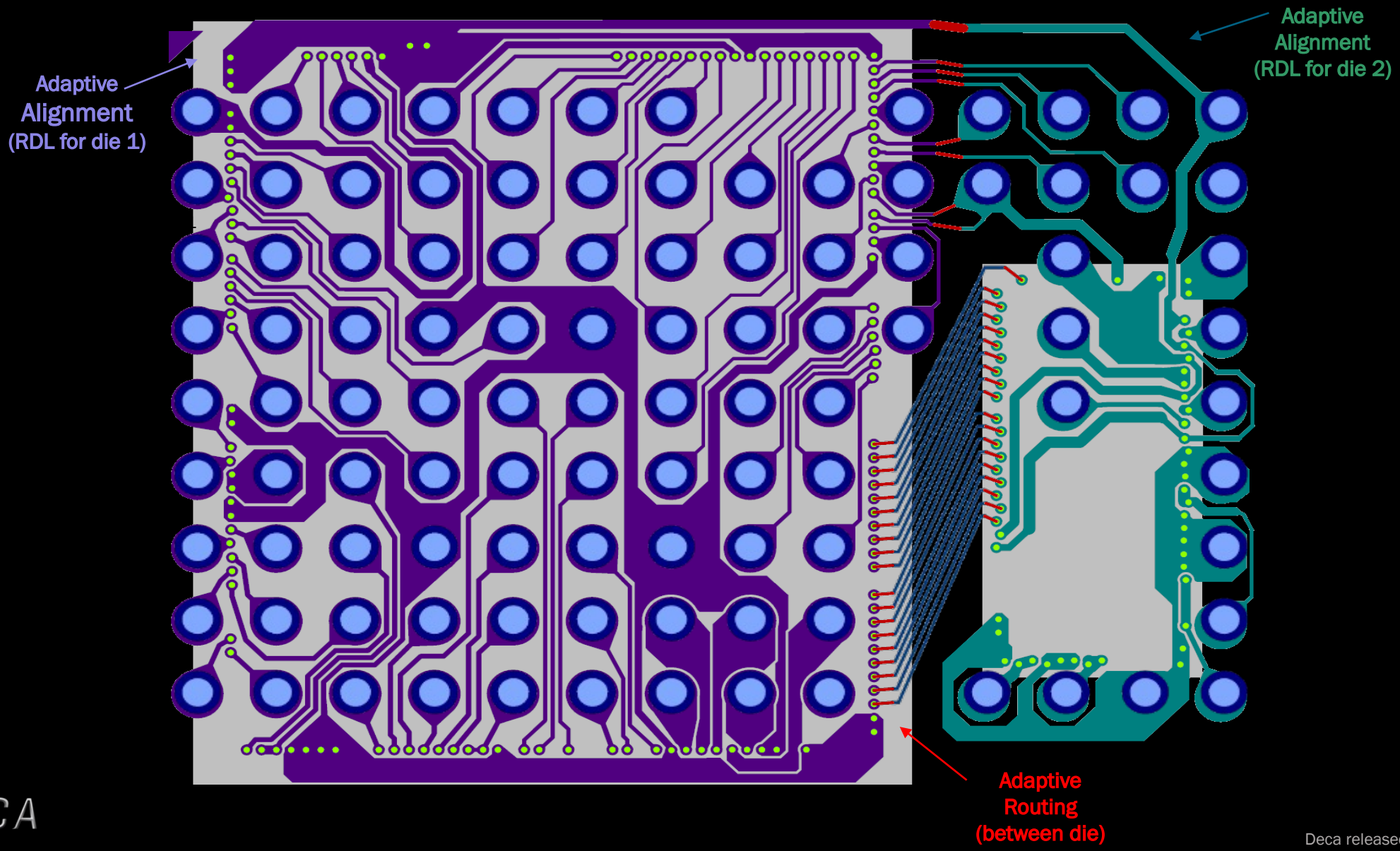
104 IO, 0.4mm pitch

Die 1: 3.7 x 3.2 mm

Die 2: 1.0 x 2.0 mm

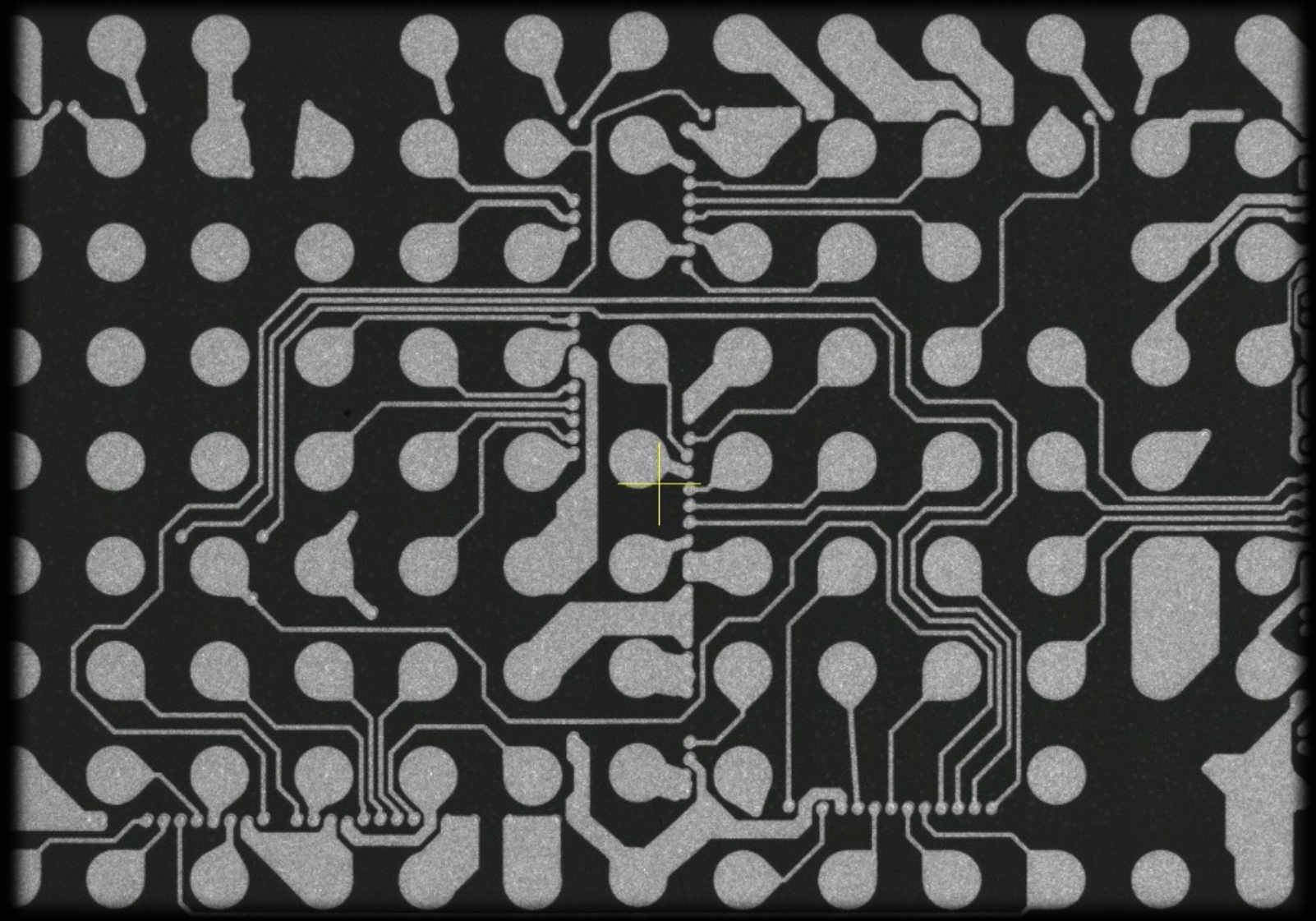
DECA

Multi-mode Adaptive Patterning



DECA

Multi-mode Adaptive Patterning – Actual AOI images



DECA

Adaptive Patterning Overcomes Process Variation

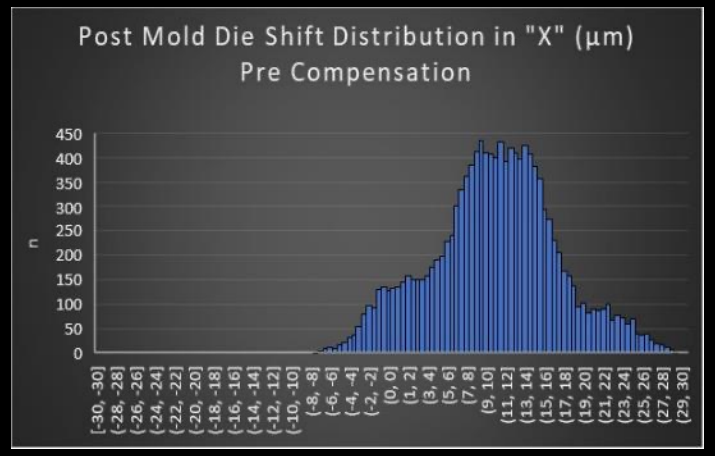
- High speed moderate accuracy chip attach specs ± 15µm X & Y, 0.10º theta
- Molding process variation typically ± 6µm X & Y

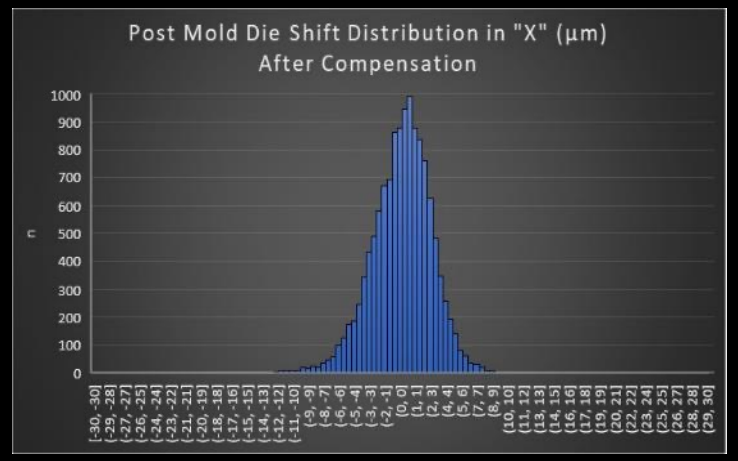
1. New product initial run on 600mm

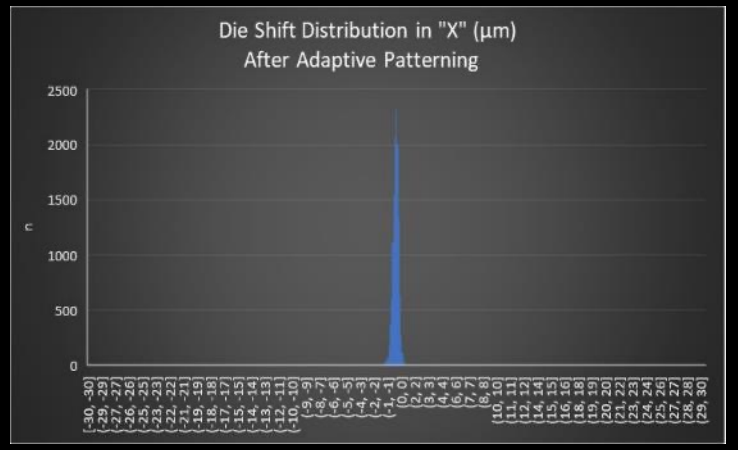
2. After chip attach compensation

3. After Adaptive Patterning

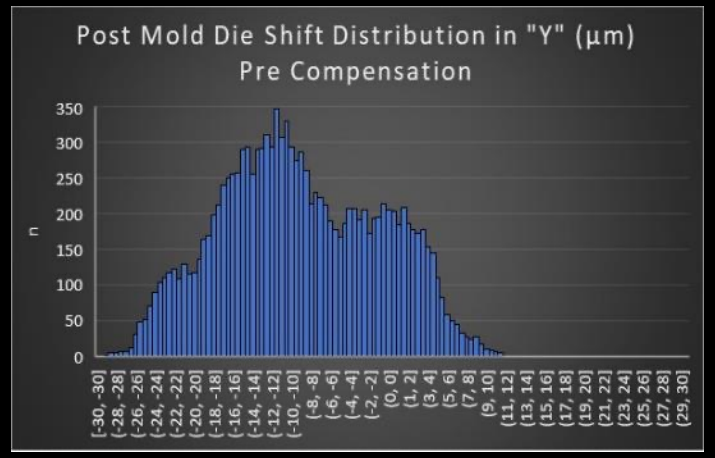
X

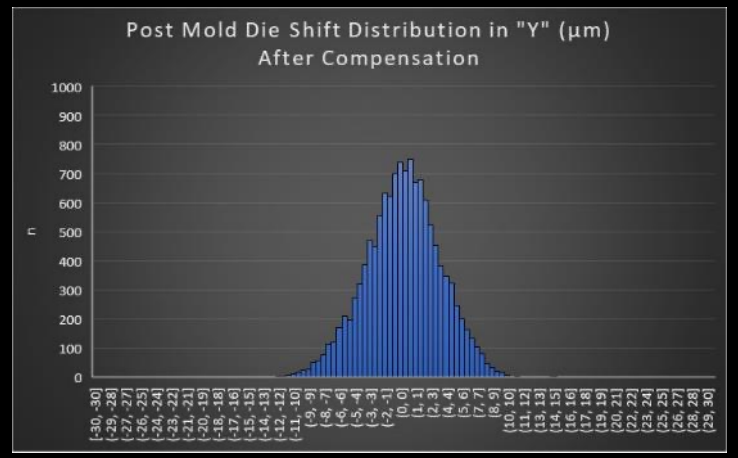


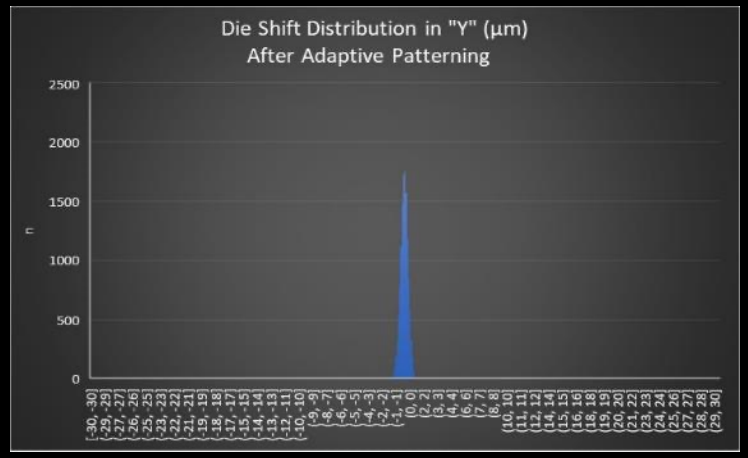




Y



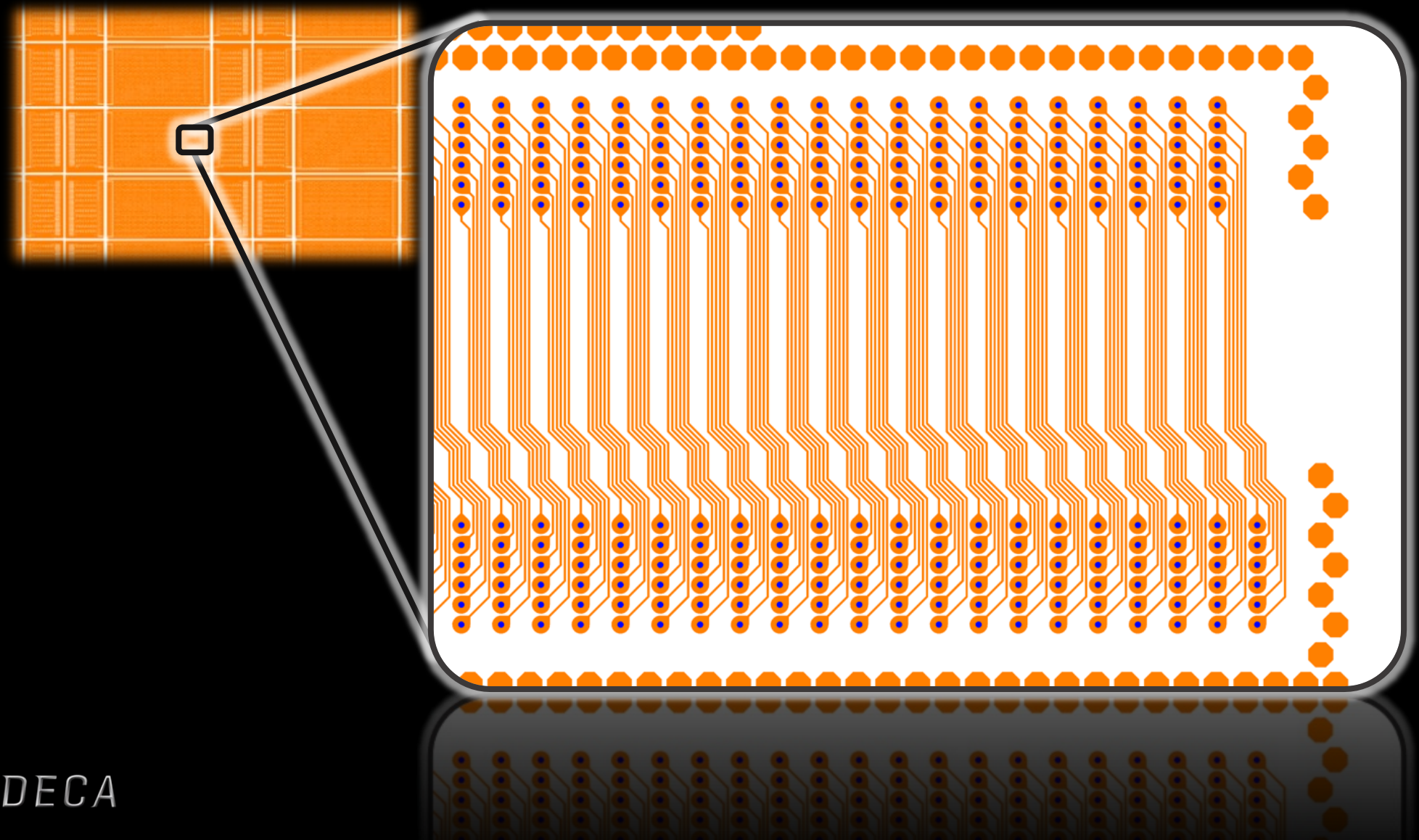




DECA

Actual 600mm large panel distribution of die location reduced to ± 1.2µm at 3 sigma

Multi-mode Adaptive Patterning – Scaled up to more wires

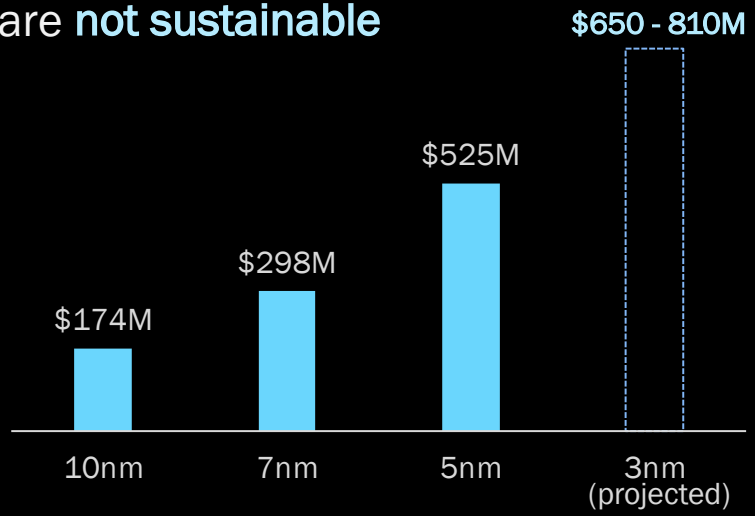


Outline

- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

DECA

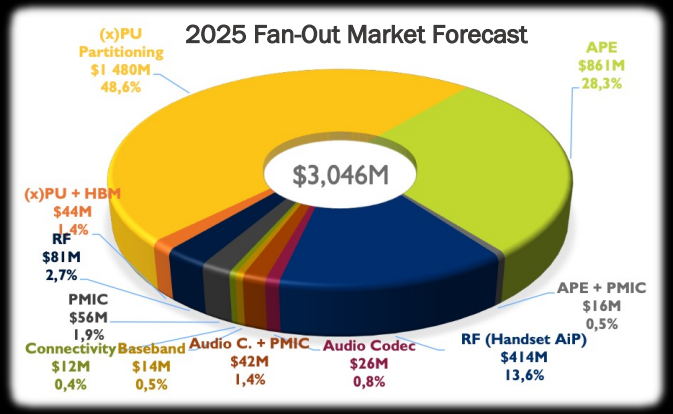
Monolithic SoC design costs are **not sustainable**



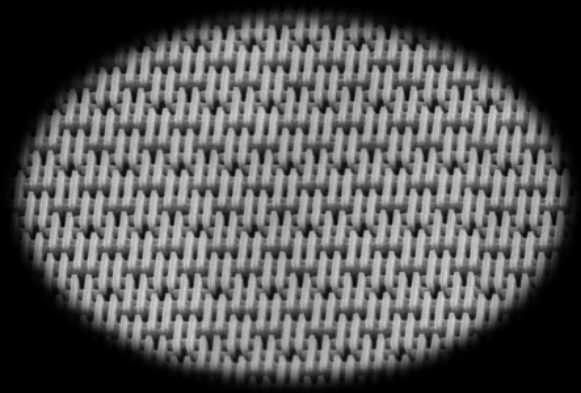
Li, et al. "Chiplet heterogeneous integration technology—status and challenges."

High-end packaging growing quickly

More than 20% CAGR expected for fan-out packaging of advanced SoC, CPU, GPU, & AI silicon

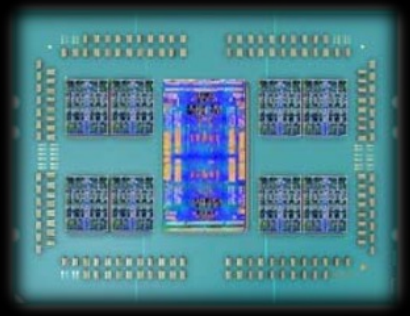


Yole Development,"Fan-Out Packaging 2020"



7nm ⟶ 5nm ⟶ 3nm

Chiplets are not a future technology In production **now**



S. Naffziger, K. Lepak, M. Paraschou and M. Subramony, "AMD chiplet architecture for high-Performance server and desktop products,"

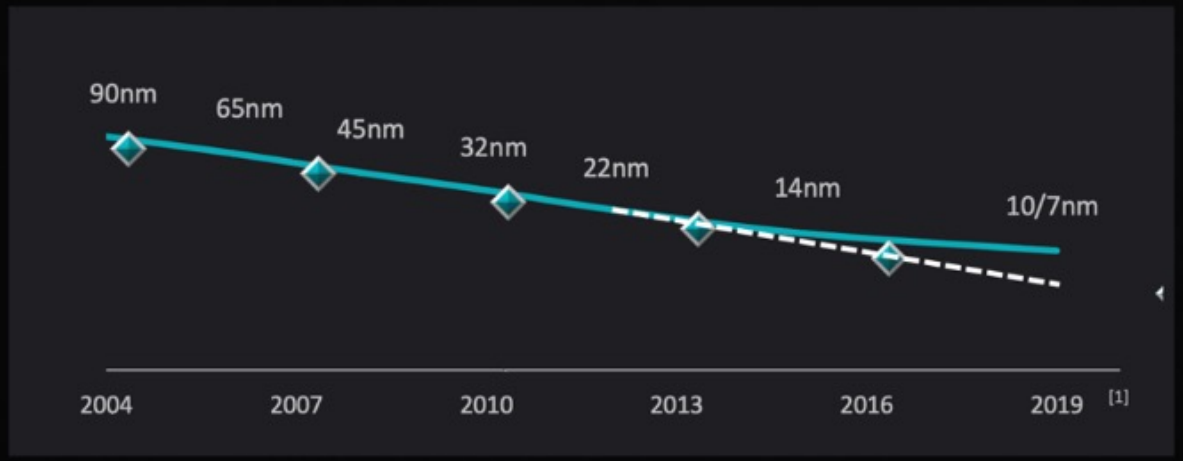
AMD EPYC "Rome"

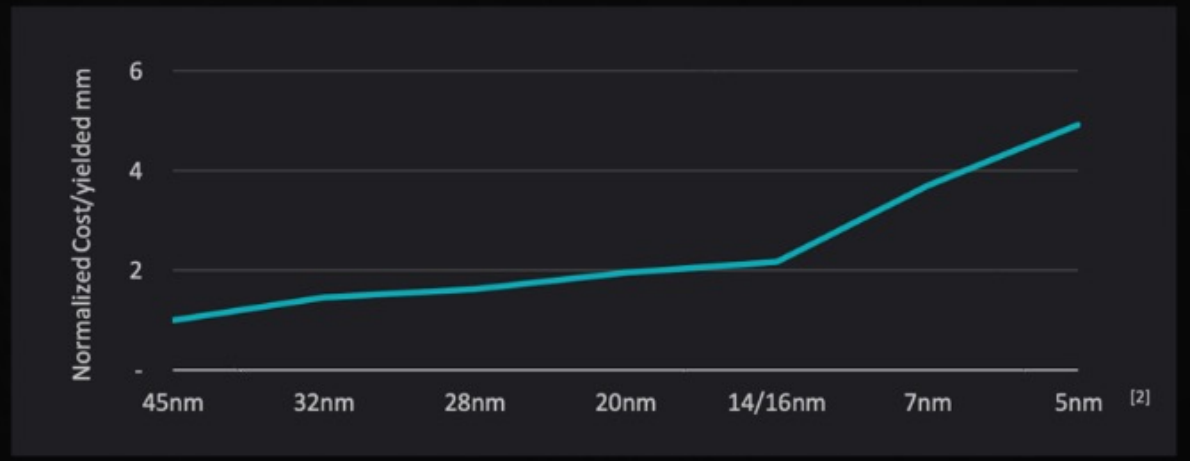
- Up to eight 7nm compute die
- One 12nm IO die
- ≥ 47% cost reduction vs. monolithic die for 48 cores
- At 64 cores, achieved higher max performance than possible in a monolithic die

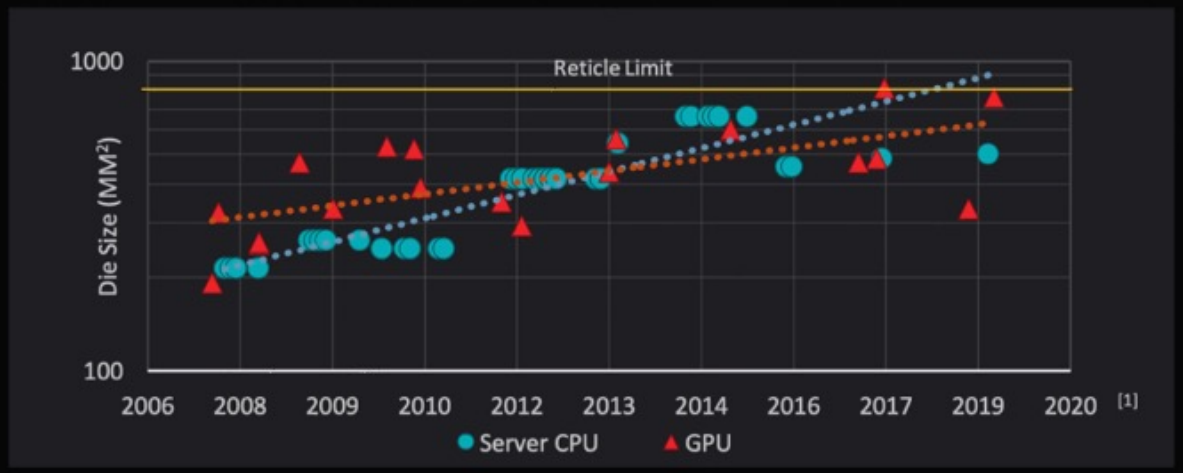
The dynamics are changing.

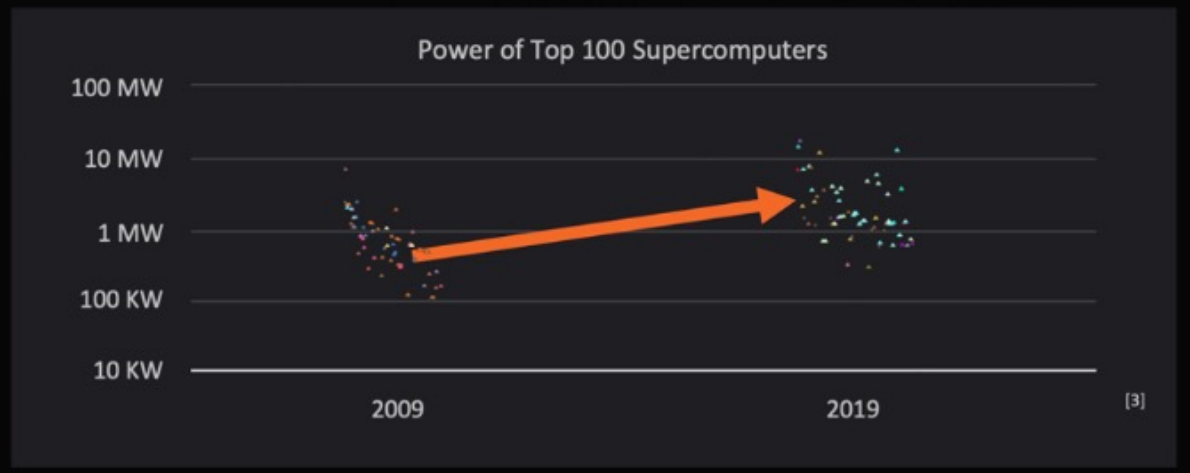
DECA

TECHNOLOGY CHALLENGES









Many Well-known Technology Challenges | Slowing of Moore's Law, Cost Increases, Die-size Limits, Power

ED PACKAGING

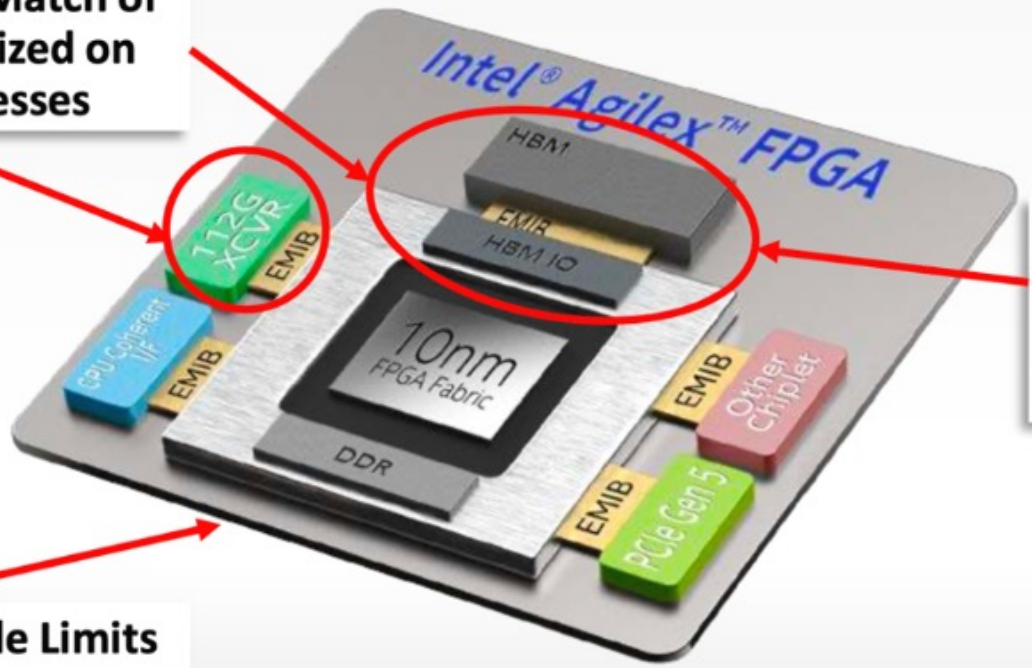
[1] Naffziger, VLSI Short Course, 2020, [2] Cost per yielded mm² for a 250mm² die, [3] Data from top500.org

AMD

Deca released for Chiplet Summit 2023

Increased Interest in HI is Driven by

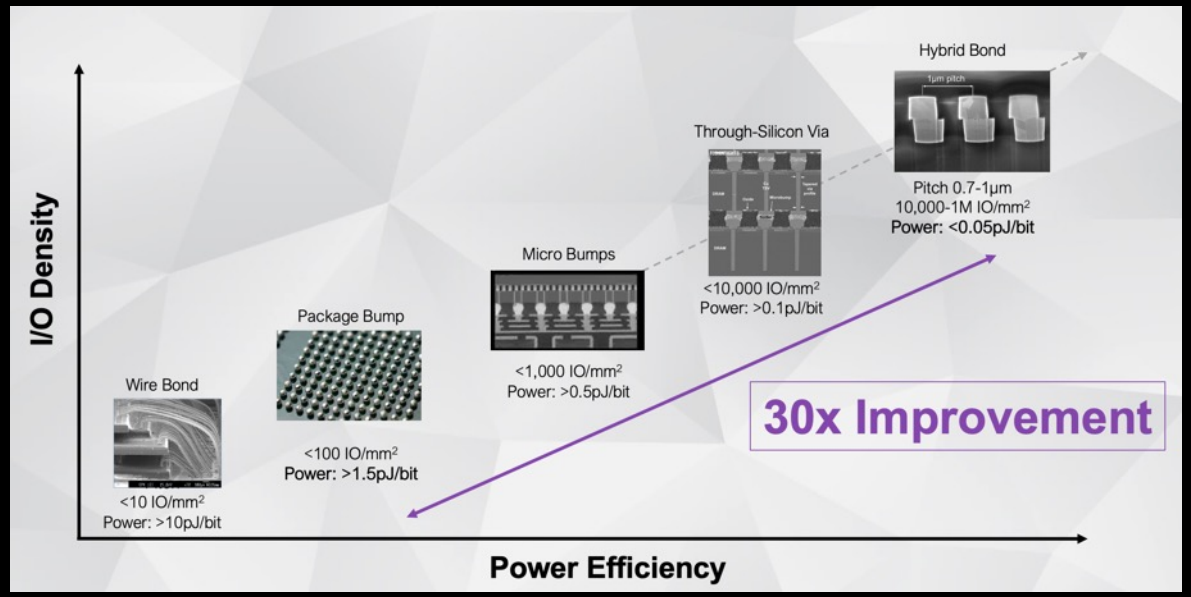
Need to Mix and Match of Diverse IP Optimized on Different processes



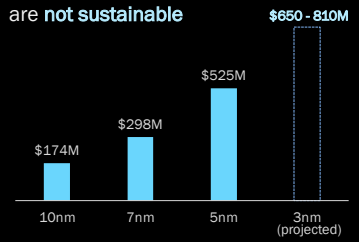
Need for Proximate Memory with a High BW Low Power Interface

Escape from Reticle Limits

Additionally, Yield Resiliency and Time to Market Advantages Make On-Package HI Attractive



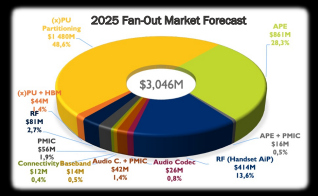
Monolithic SoC design costs are **not sustainable**



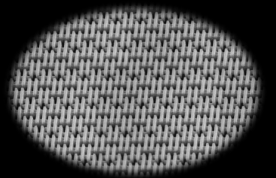
Li, et al. "Chiplet heterogeneous integration technology--status and challenges."

High-end packaging growing quickly

More than 20% CAGR expected for fan-out packaging of advanced SoC, CPU, GPU, & AI silicon

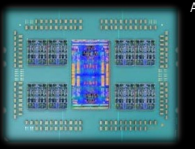


Yole Development "Fan-Out Packaging 2020"



7nm → 5nm → 3nm

Chiplets are not a future technology
In production **now**

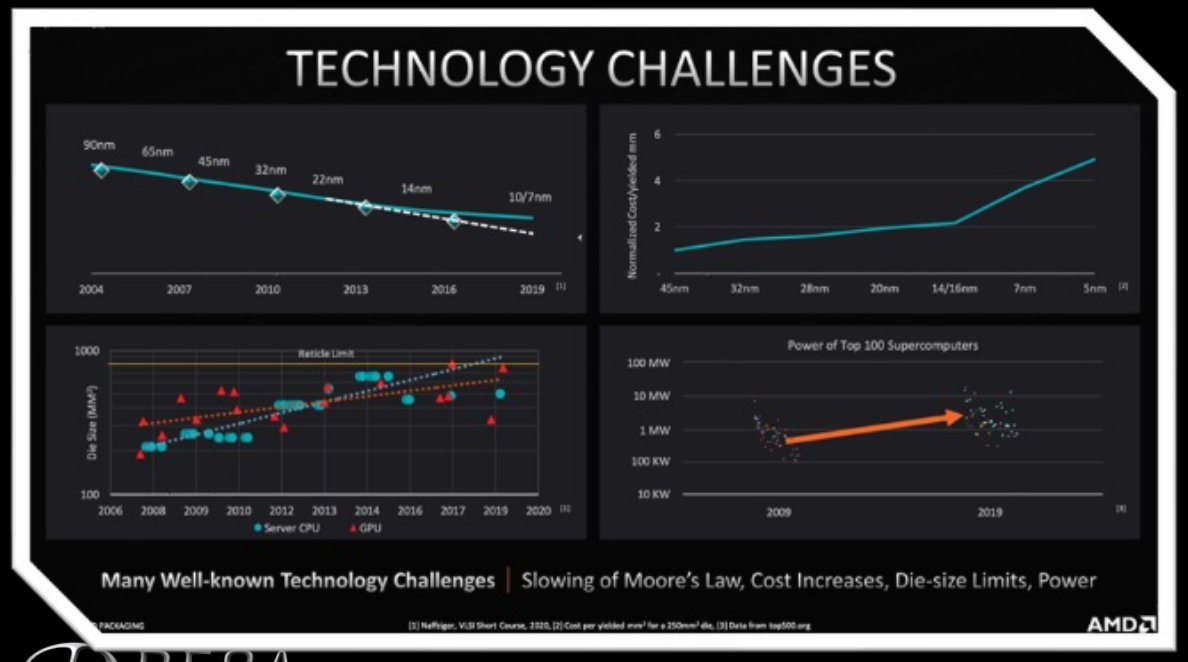


S. Naffziger, K. Lepak, M. Paraschou and M. Subramony, "AMD chiplet architecture for high-Performance server and desktop products,"

AMD EPYC "Rome"

- Up to eight 7nm compute die
- One 12nm IO die
- ≥ 47% cost reduction vs. monolithic die for 48 cores
- At 64 cores, achieved higher max performance than possible in a monolithic die

The dynamics are changing.

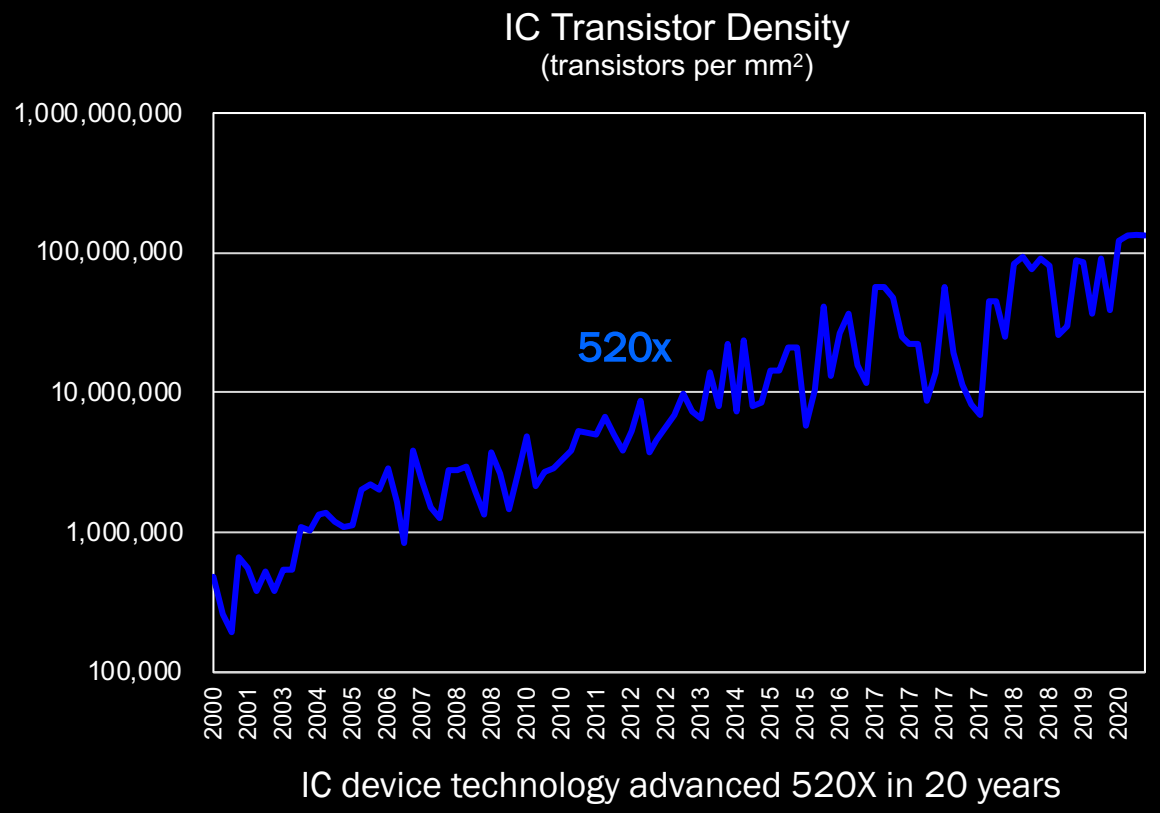


DECA

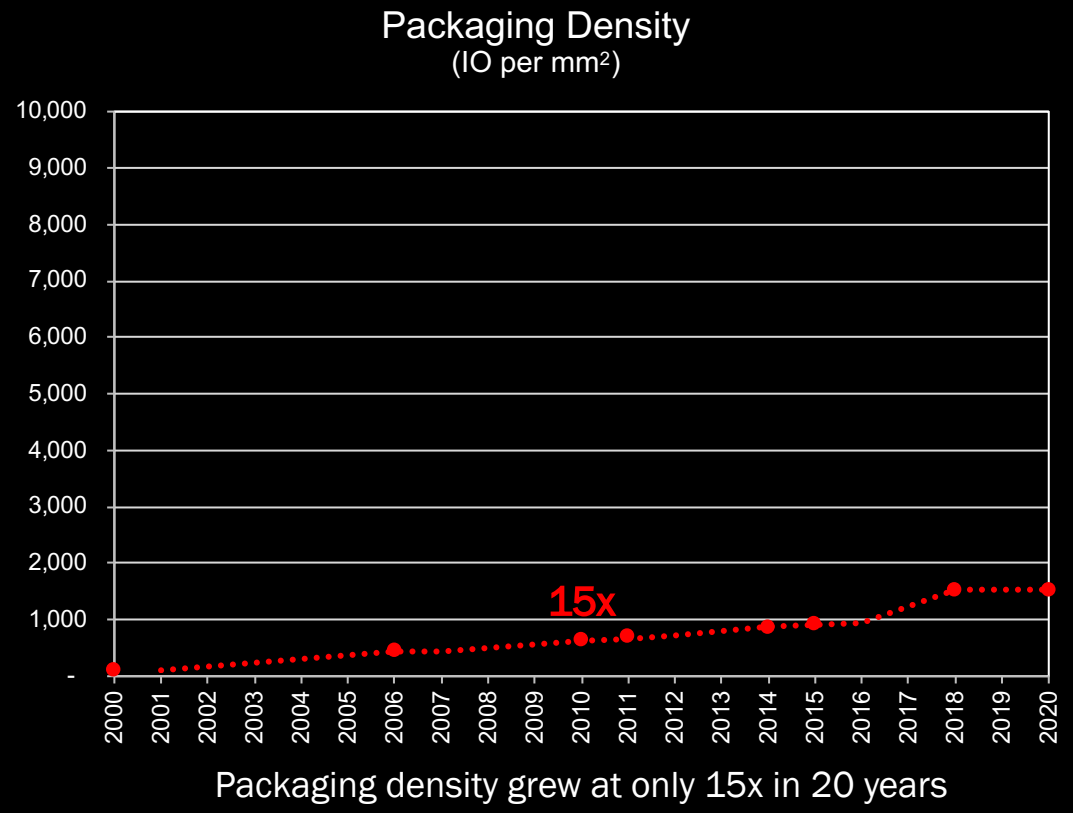
Deca released for Chiplet Summit 2023

Scaling Down for Higher Density

Packaging severely lagging semiconductor device technology (15x vs. 500x density increase in past 20 years)



Source: Multiple industry sources compiled at en.wikipedia.org/wiki/Transistor_Count



Sources: 1. Chip scale Review: March-April 2020, IO/mm² derived from die pad pitch data
2. Tech Search Intl, Advanced Packaging Update, Vol 2, 2020

Packaging interface density orders of magnitude behind ICs

DECA

A simplified picture

Leading-node cost per yielded mm^2 silicon increasing

Demand for more compute & memory per package insatiable

→ More die connected with ~~"packaging"~~ interconnect technologies

→ Need more vertical connections: µBumps, TSVs, hybrid bonding, RDL vias, Cu posts

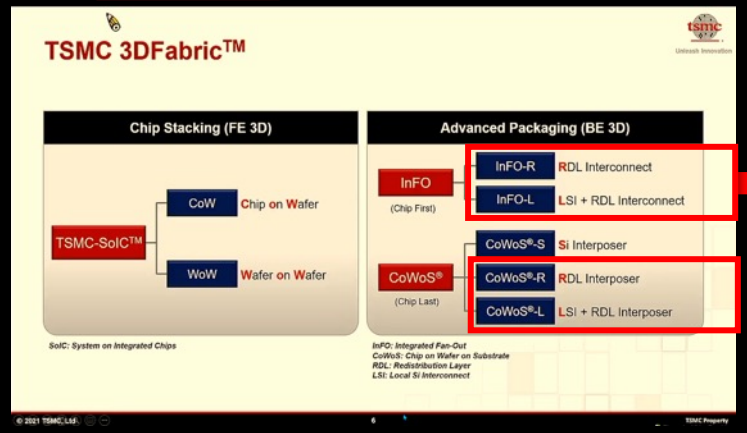
→ Need more wires: Si interposer, embedded bridge, UHD RDLs → fan-out metal layers

Outline

- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

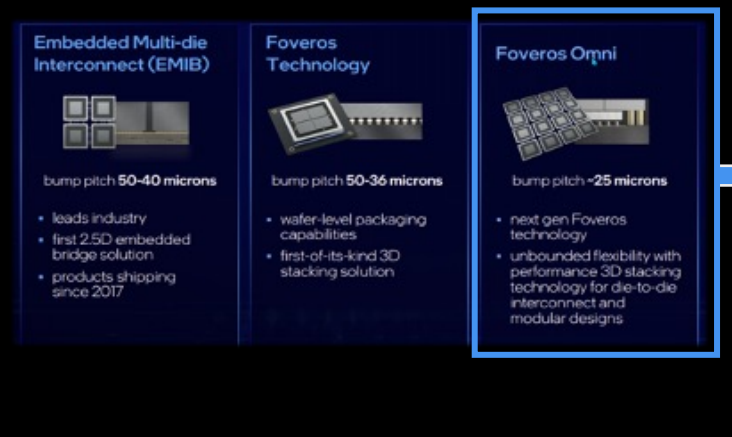
Fan-out RDL is a key element to heterogeneous integration

1. tsmc — Industry leader in advanced packaging

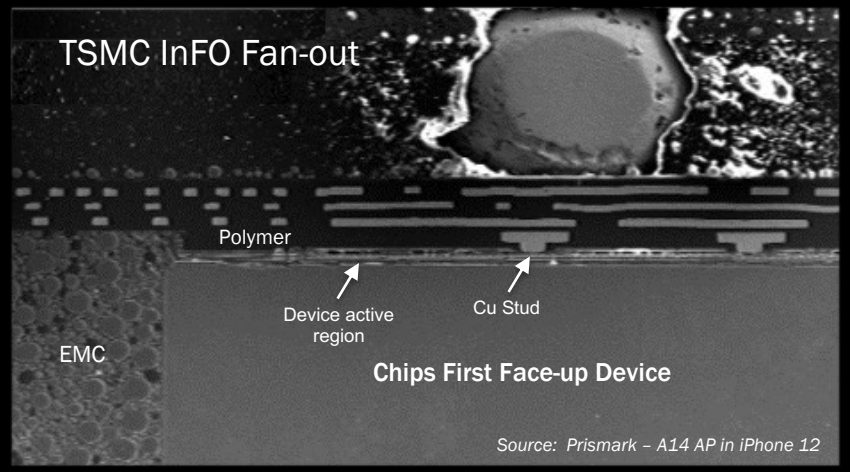


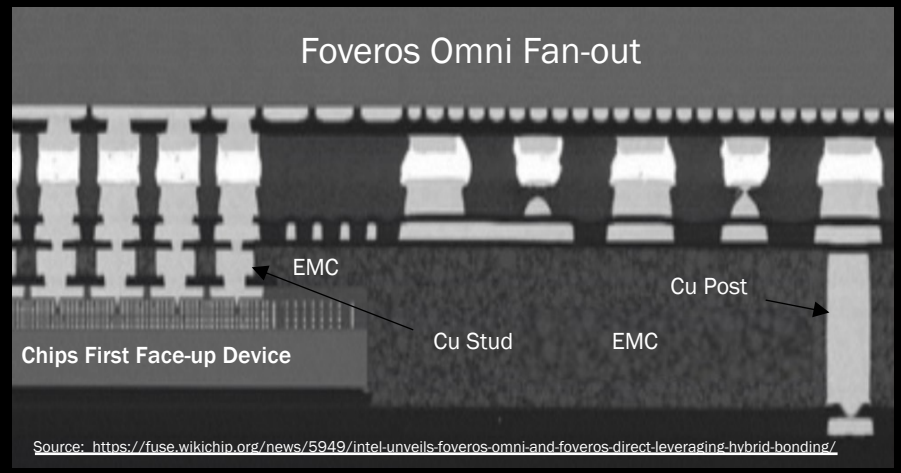
4 out of 5 of TSMC's advanced packaging structures are fan-out based

2. intel



Intel's most advanced packaging structure is fan-out based



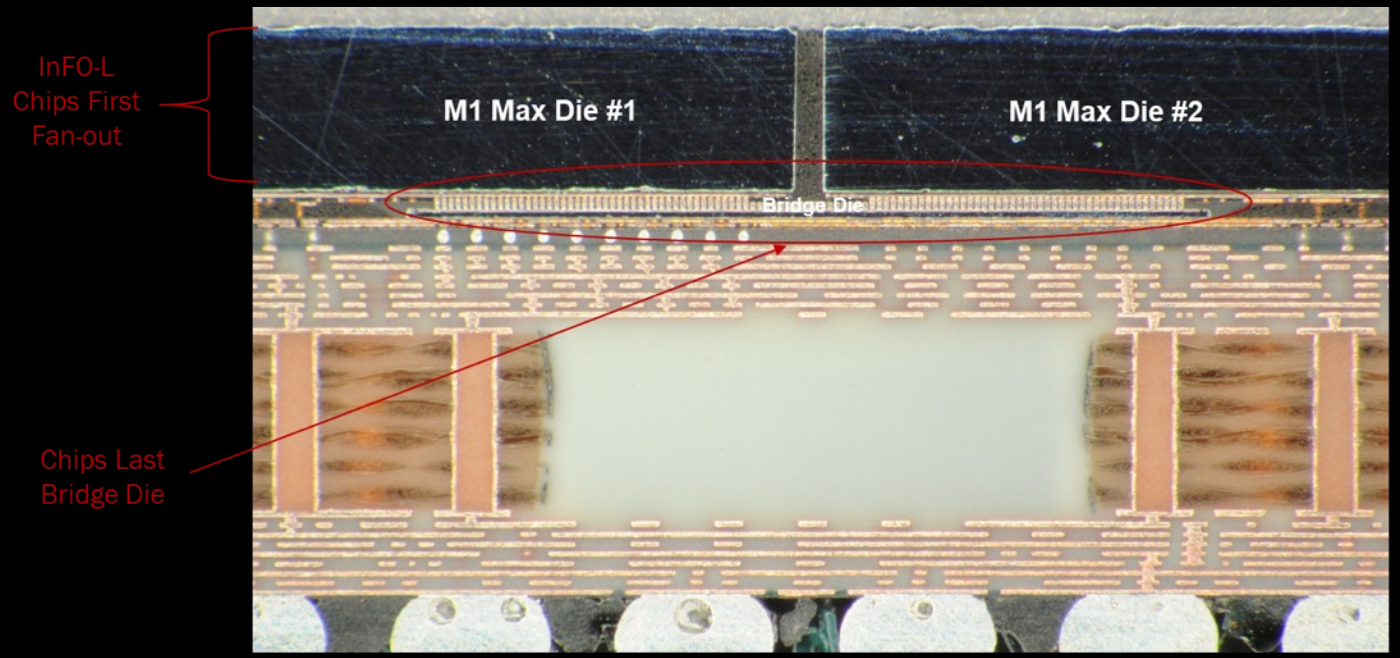


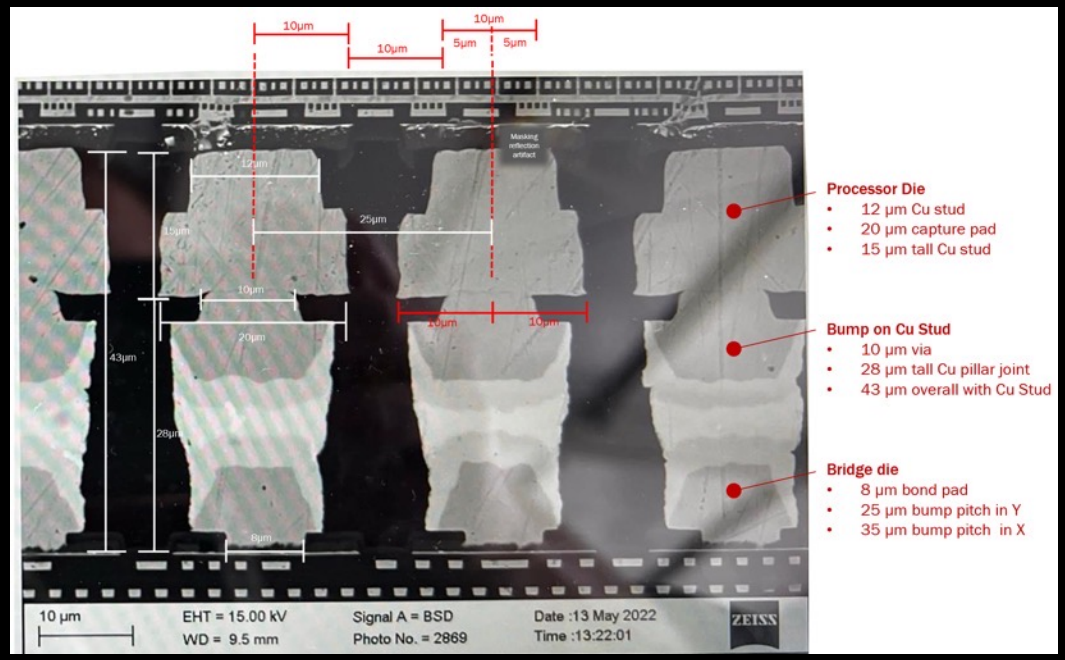
Intel's Foveros ODI is nearly identical to Deca's M-Series

DECA

Fan-out RDL is a key element to heterogeneous integration

Apple M1 Ultra for Mac Studio – Two M1 Max chips first in fan-out + flip chip bridge die

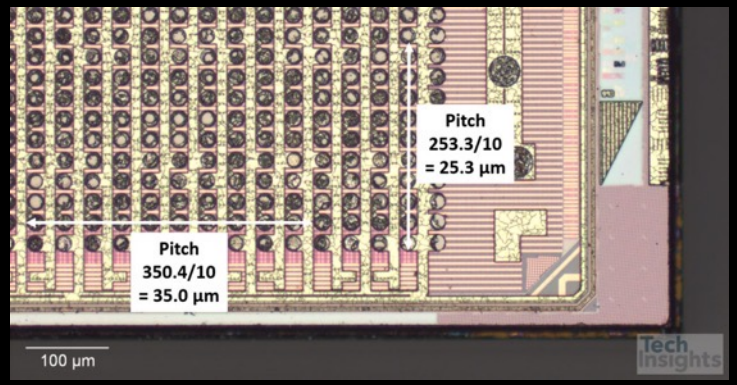




65x72mm TSMC InFO-L fan-out on substrate

- Chips up, chips first M1 Max die (2 die)
- Very fine pitch Cu pillar flip chip bridge die (25µm x 35µm)

2.5 TB/s die-to-die bandwidth

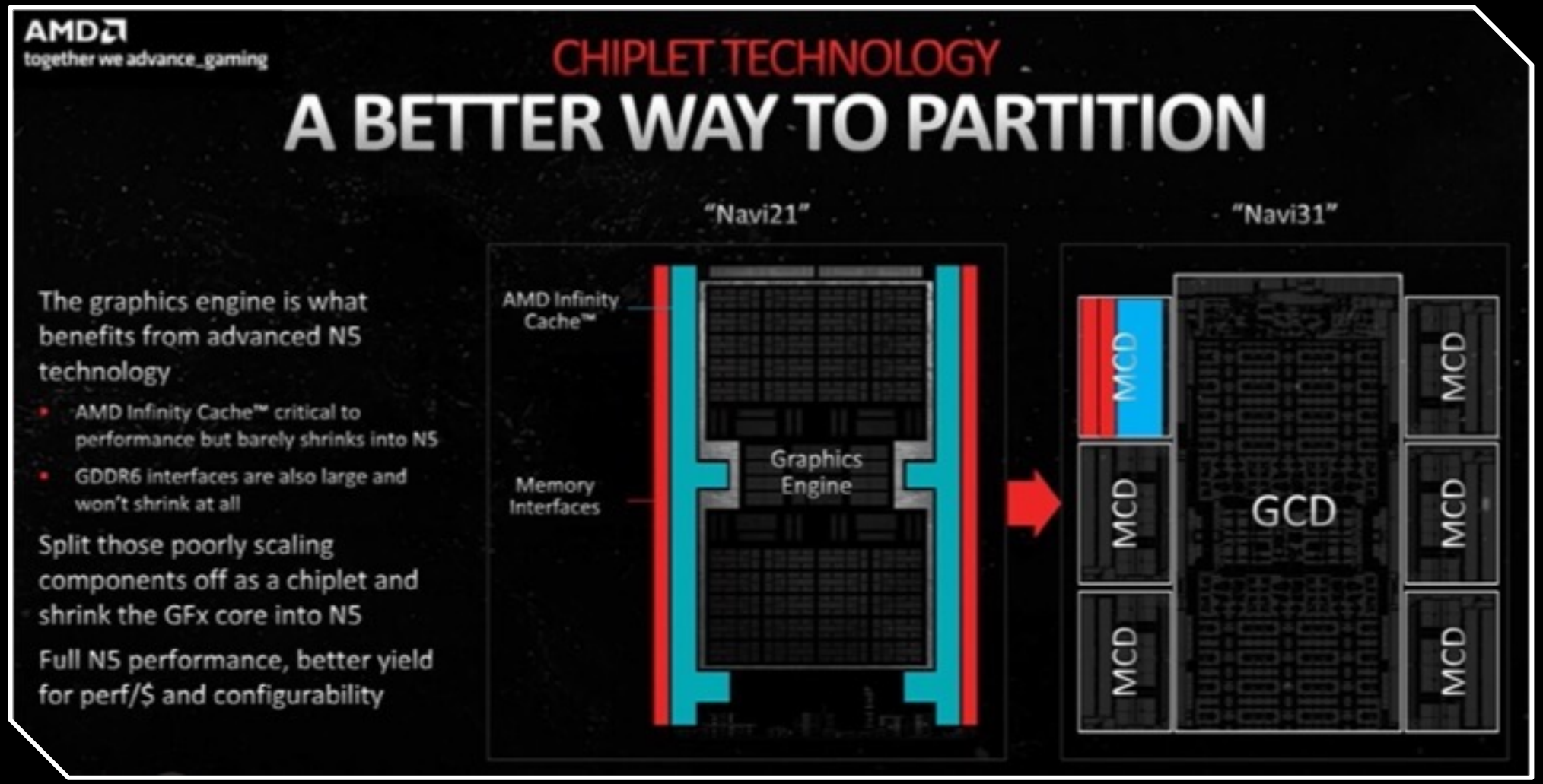


https://www.techinsights.com/blog/apple-joins-3d-fabric-portfolio-m1-ultra

DECA

Fan-out RDL is a key element to heterogeneous integration

AMD RDNA 3 - GPU chiplets with fan-out RDL



Fan-out RDL is a key element to heterogeneous integration

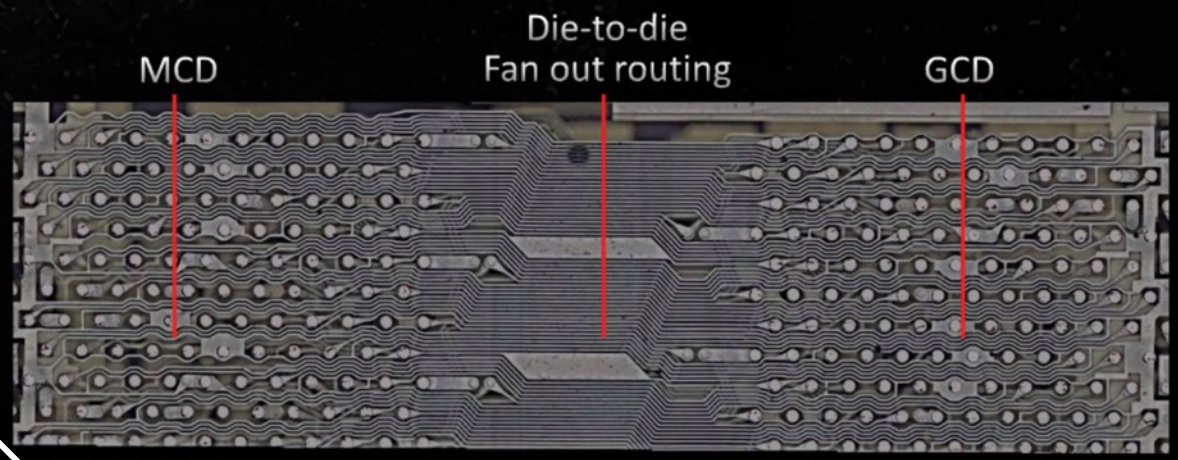
AMD RDNA 3 - GPU chiplets with fan-out RDL

CHIPLET TECHNOLOGY

INFINITY FANOUT LINKS

BANDWIDTH DENSITY

- Infinity Links, operating at 9.2Gb/s with High Performance Fanout provide almost 10X the BW density of the IFOP links used in Ryzen and EPYC
- Enables industry-leading peak bandwidth of 5.3TB/s



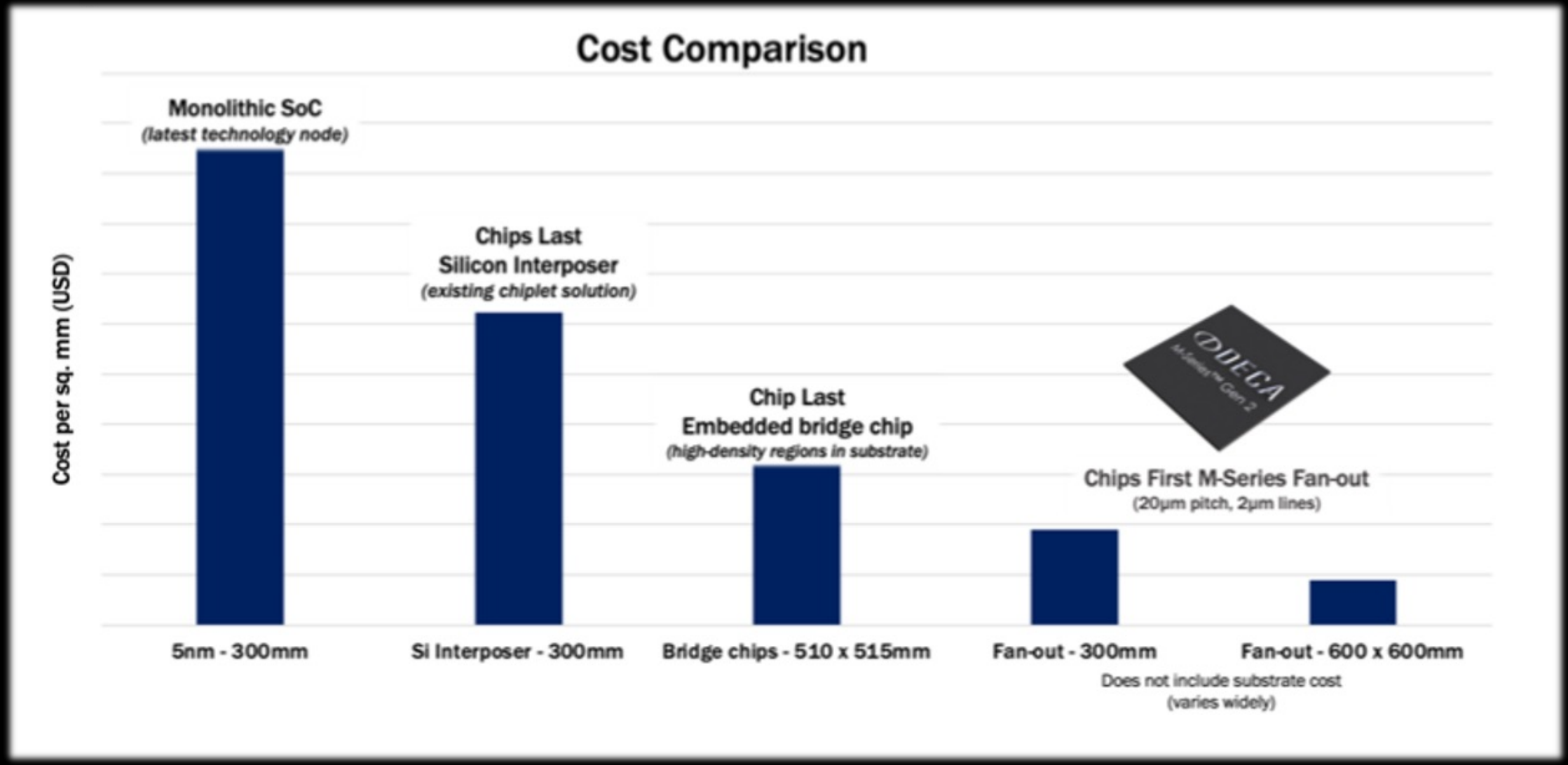
AMD's High Performance Fanout Interconnect

https://www.tomshardware.com/news/amd-rdna-3-gpu-architecture-deep-dive-the-ryzen-moment-for-gpus

Interconnect	Picojoules per Bit (pJ/b)
On-die	0.1
Foveros	0.2
EMIB	0.3
UCIe	0.25-0.5
Infinity Fabric (Navi 31)	0.4
TSMC CoWoS	0.56
Bunch of Wires (BoW)	0.5-0.7
Infinity Fabric (Zen 4)	???
NVLink-C2C	1.3
Infinity Fabric (Zen 3)	1.5 (?)

DECA

Why fan-out is on the rise everywhere? → Cost



Sources: Yole Advanced Substrates 2018, Customer feedback, Deca estimates

DECA

Outline

- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

M-Series™ & Adaptive Patterning® Technology Roadmap

M-Series Gen 1

2016 →

Codec

RF

IoT Device

PMIC

Dual PMIC

Single-die

- Protected fan-in
- Fan-out

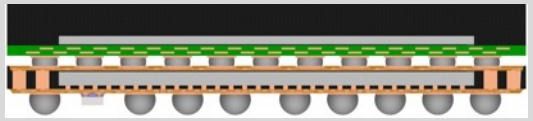
Multi-die

- RF & IoT modules
- Integrated PMICs

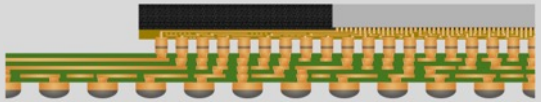
55 µm bond pad pitch
8 µm lines & spaces
Up to 2 layers of RDL

M-Series Gen 1.5

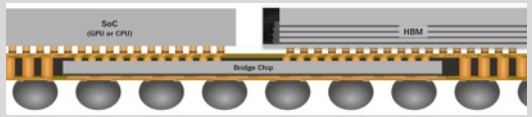
(High Density Integration)
2021 →



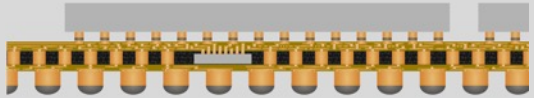
1. 3D PoP - Mobile Applications Processor



2. Fan-out SoC – Expanding bond pad pitch on advanced node Si



3. Embedded Bridge Die Interposer – Replacing Si interposers for SoC to HBM integration

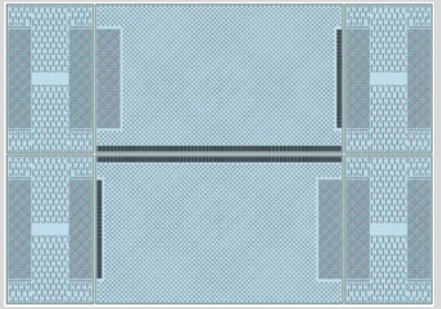


4. Passive & Active Interposers – Power mgmt., memory integration, etc. for CPU, GPU, AI & Networking

45 µm bond pad pitch
5 µm lines & spaces
Up to 5 layers of RDL

M-Series Gen 2

(Ultra-High-Density Integration)
2022 →



- 20µm die pad pitch
- 2µm lines & space

Ultra-high-density chiplet integration

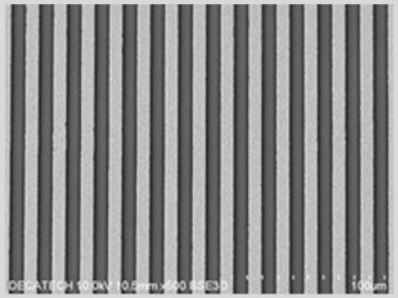
No reticle = No package size limitation

20 µm bond pad pitch
2 µm lines & spaces
> 5 layers of RDL

DECA

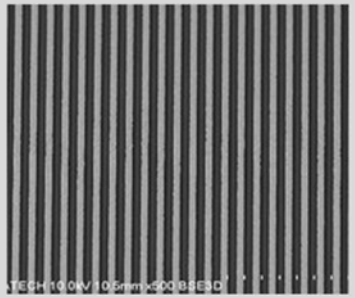
Scaling Roadmap

Gen 1
2016 →



Attribute	Units	Gen 1
RDL lines & spaces	µm	10
RDL layers (per side)	#	2
RDL line density	Lines / mm / layer	50
Minimum via*	µm	20
Enclosure	µm	7.5
Bond pad pitch	µm	55
Cu stud diameter	µm	35

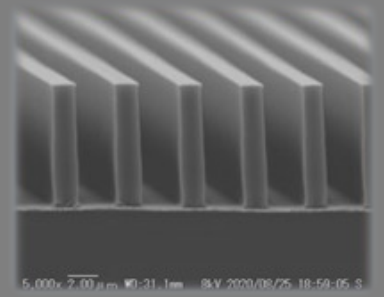
Gen 1.5
2021 →



Gen 1.5
5
5
100
10
7.5
45
30

Original Equipment Set

Gen 2
2022 →



Gen 2	Gen 2.1	Gen 2.2
2	1.75	1.5
5	6	8
250	Under NDA	
5		
3		
20		
12		

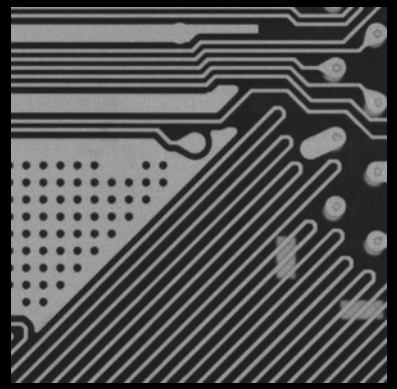
Gen 2 Lithography & AOI

Gen 3

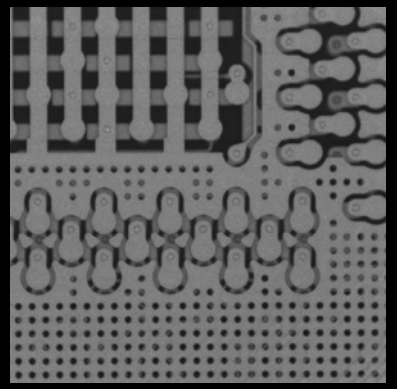
Gen 3 MDx
0.8
Under NDA

DECA

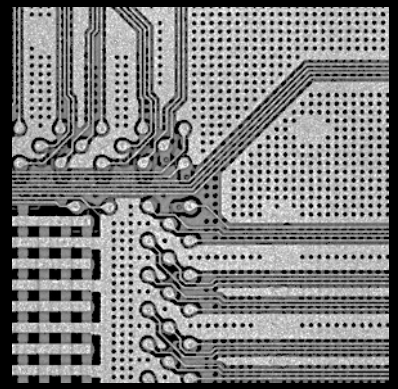
Five layer RDL fan-out for CPU



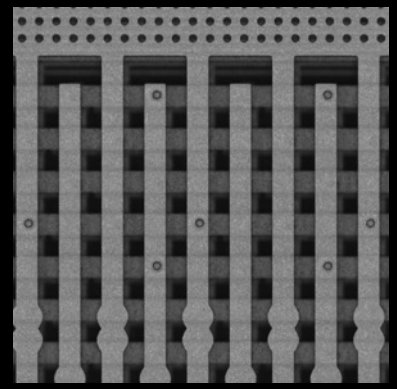
RDL 1



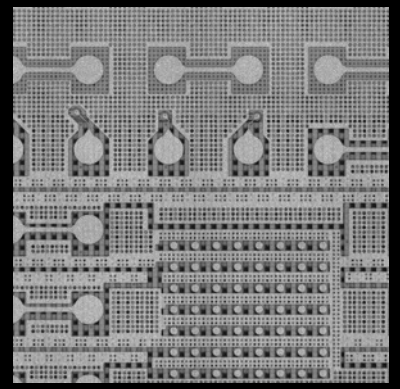
RDL 2



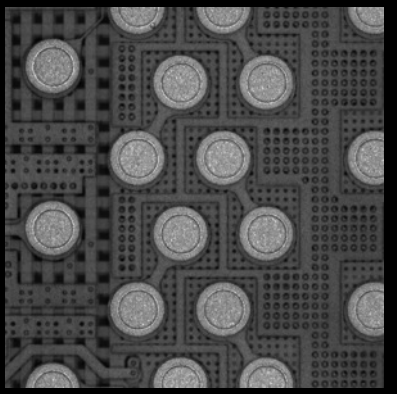
RDL 3



RDL 4



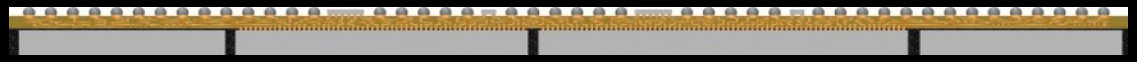
RDL 5

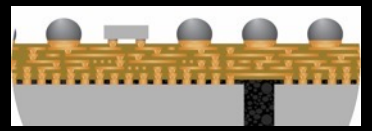


UBM

Phase 1
Monolithic SoC

Phase 2
Chiplet-based SoC



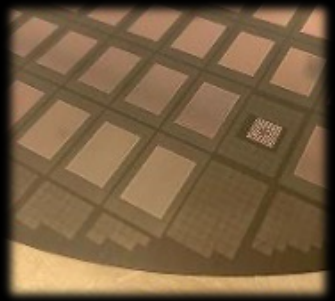


CPU **device split into chiplets**

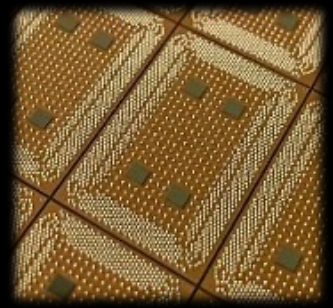
- 5-layer RDL
- 20 µm device bond pad pitch
- 60 µm die to die spacing
- Structural silicon added
- IPDs on UBM layer
- No bridge die required

Phase 1 device

- After panelization



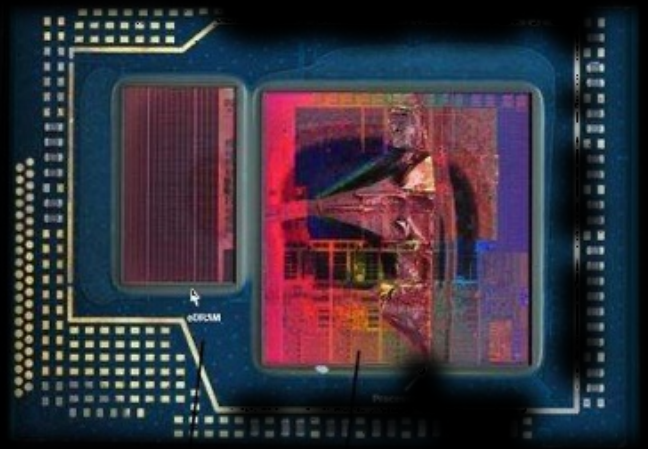
- After IPD & ball attach

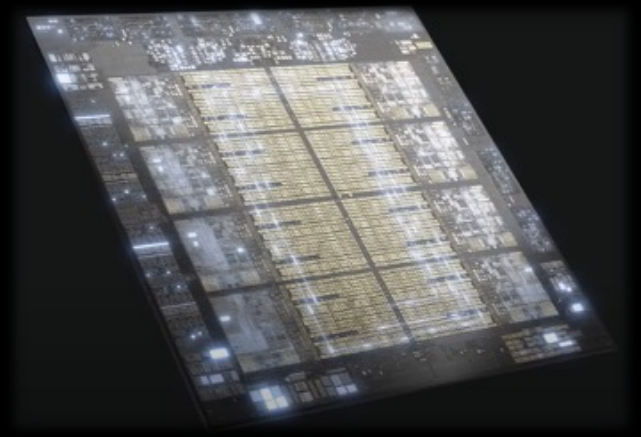


DECA & nepes

Traditional cache memory integration

Package substrate level cache integration





Benefits (vs. monolithic)

- Increased L3-L4 cache size
- Potential for heterogenous integration
- Reduced CPU die area
  - Lower cost
  - Higher yield
  - Higher performance

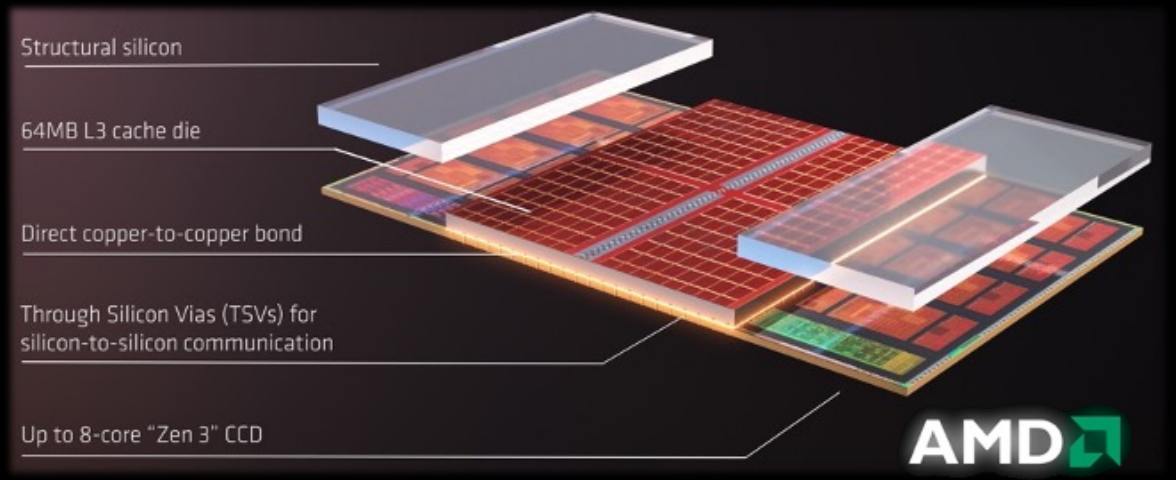
Challenges

- Power consumption
  - Long wire length
  - High frequency SERDES
- Limited bandwidth
  - Coarse IO pitch (90-180 µm)
  - Constrained wire density
- High latency

DECA

Leading-edge cache memory integration

3D silicon cache integration



Leading the industry in Cu-Cu bonding

Benefits (vs. monolithic)

- 50% larger L3 cache with high performance
  - Extremely high bandwidth (> 2 TB/s)
  - Low latency

Challenges

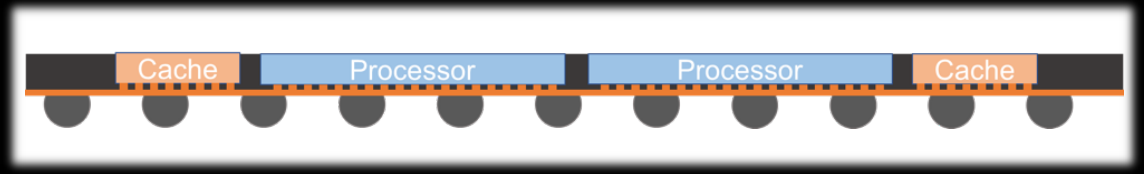
- Cache and structural silicon in thermal path
- Power delivery through CPU die
- Expensive
  - Die-to-wafer Cu-to-Cu hybrid bonding
  - TSVs

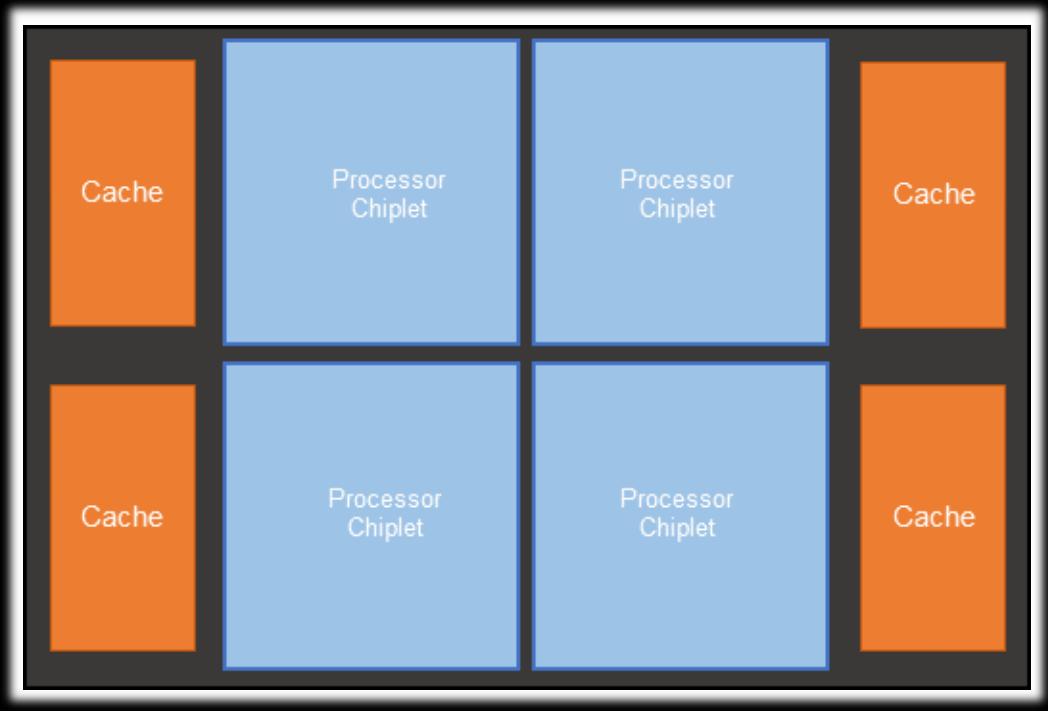
DECA

Fan-out Applications – Lateral Processor to Cache(1)

- Processor and cache are embedded
- RDL interconnect between processor & cache
  - All Cu, no solder flip chip
  - Multi-layer RDL – up to 5 proven
  - 2 µm line & space
  - 20 µm bond pad pitch
- Dense chiplet integration
  - 65 µm die to die spacing
  - < 1.5 mm channel length
- C4 or Cu pillar bumps to substrate

  or
- Directly mount to PCB, no substrate





DECA

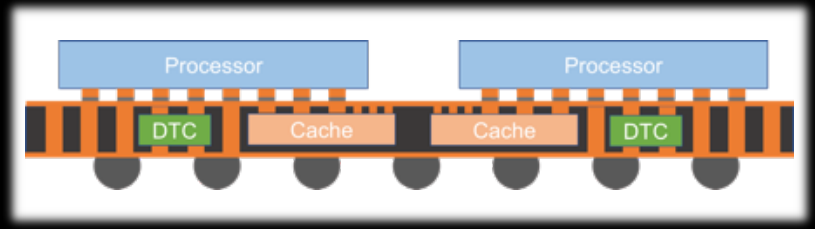
Fan-out Applications – Vertical Chips Last (2)

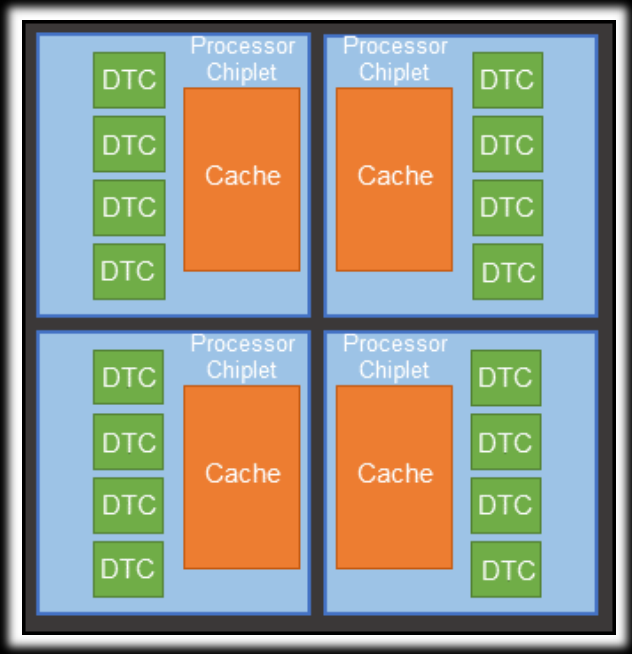
- Processor chiplets flip chip mounted (chips last)
- Cache embedded

- High bandwidth, low latency from processor to cache
  - Minimized channel length, directly vertical
  - Standard C4 or Cu pillar attach
  - Microbumps for advanced applications

- Dense lateral interconnect between cache die for coherency
  - 2 µm line & space
  - 20 µm bond pad pitch

- Low impedance power distribution network (PDN)
  - Embedded deep trench capacitors (DTCs)
  - Power and ground planes in thick RDL
  - Vertical Cu posts from BGA to processor





DECA

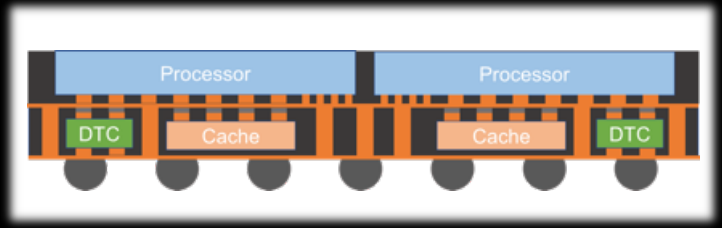
Fan-out Applications – Vertical Chips First (3)

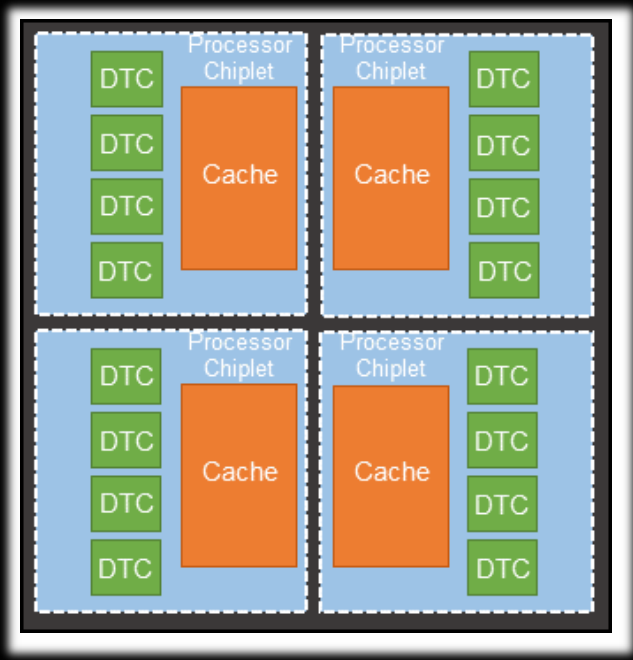
- Processor chiplets embedded (chips first)
- Cache flip chip mounted

- Dense lateral interconnect between processor chiplets
  (vs. between cache on previous slide)
  - 2 µm line & space
  - 20 µm bond pad pitch

- High bandwidth, low latency from processor to cache

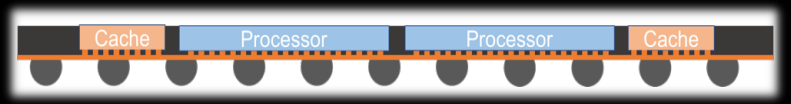
- Low impedance power distribution network (PDN)



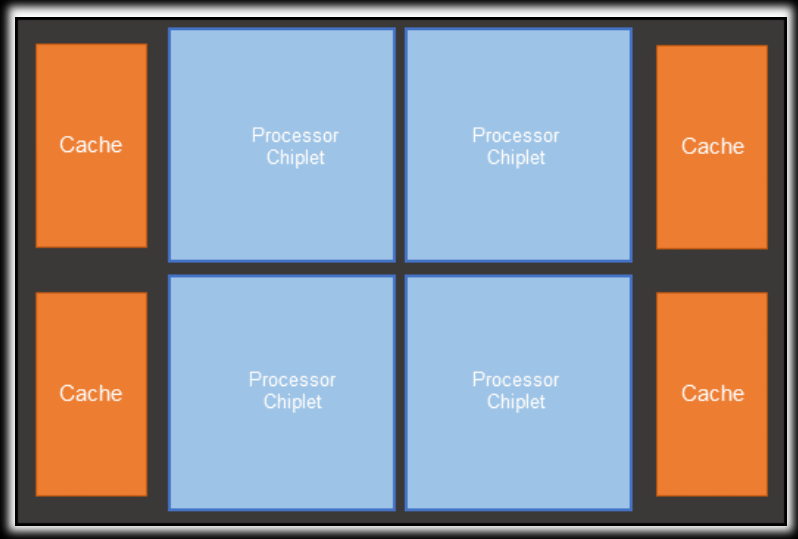


DECA

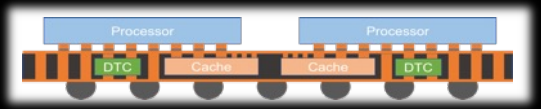
Fan-out Applications – Lateral vs. Vertical



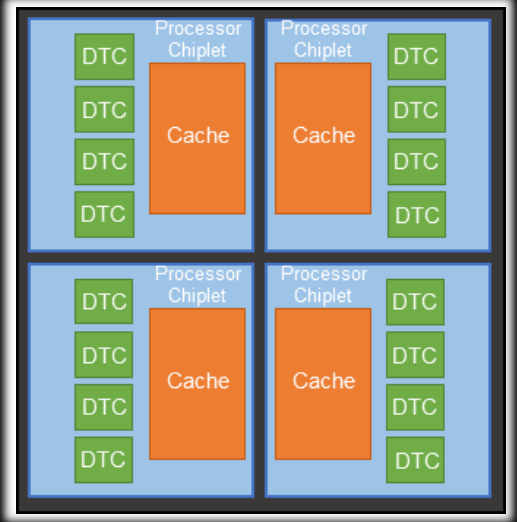
1. Lateral



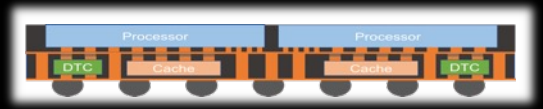
Lateral Chiplets Integration
Chips first cache & processor chiplets



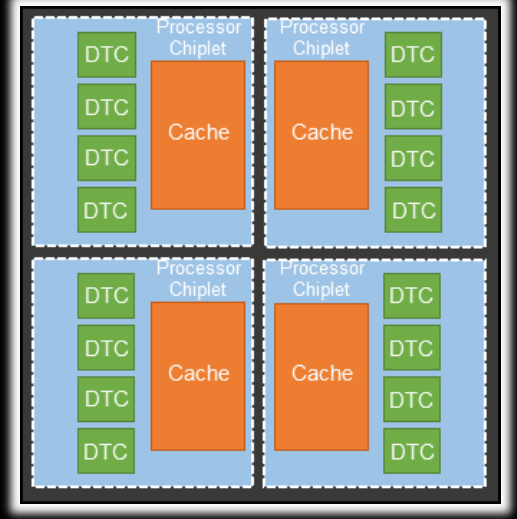
2. Vertical - CL



Face-to-Face Chips Last
Chips first cache & DTCs
Chips last processor chiplets



3. Vertical - CF

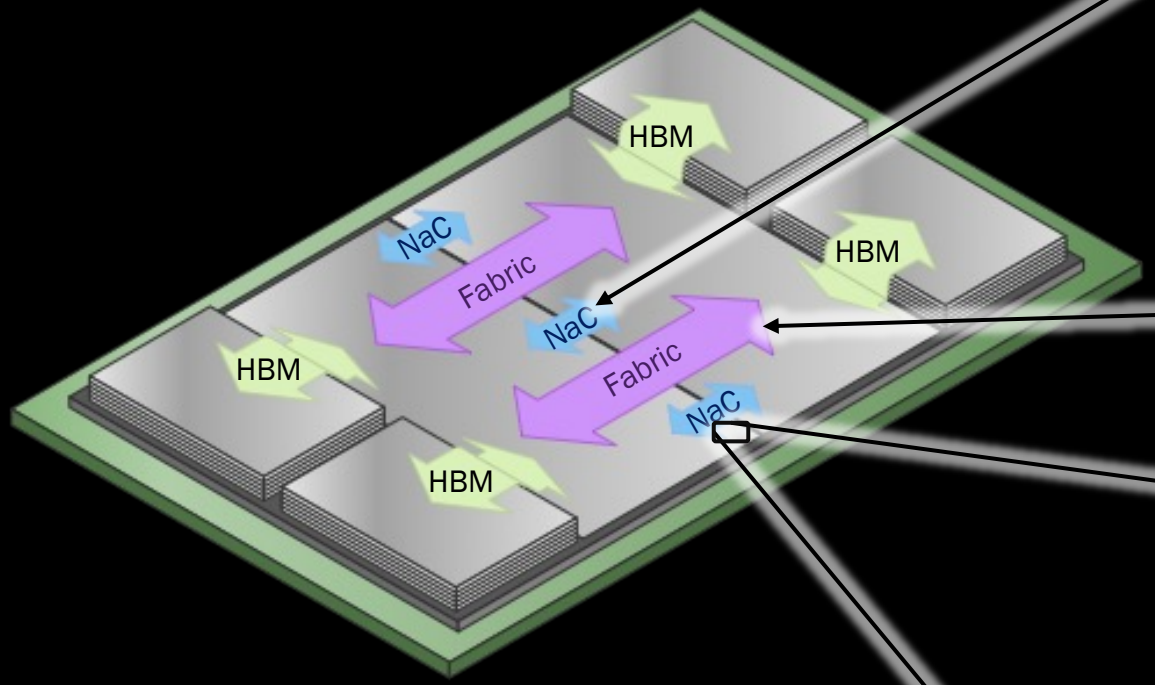


Face-to-Face Chips First
Chips first processor chiplets
Chips last cache & DTCs

DECA

HPC, AI & FPGA – without Si interposer

Fan-out RDLs become part of the chip itself

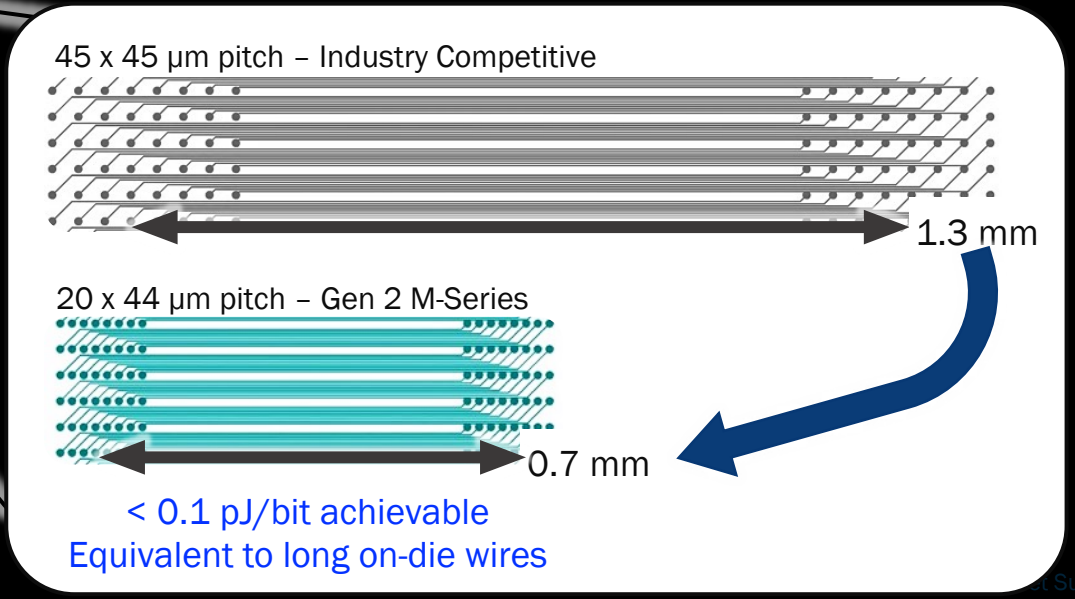


High bandwidth & efficient network across chiplets – NaC

- Extends network on chip (NoC) to multi-die
- Multiple links for 1-5 TB/s **@ < 0.1 pJ/bit**
- Synchronous flop-top-flop channel with 3rd-party clock IP offers low area and power overhead

Die-to-die FPGA fabric routing resources

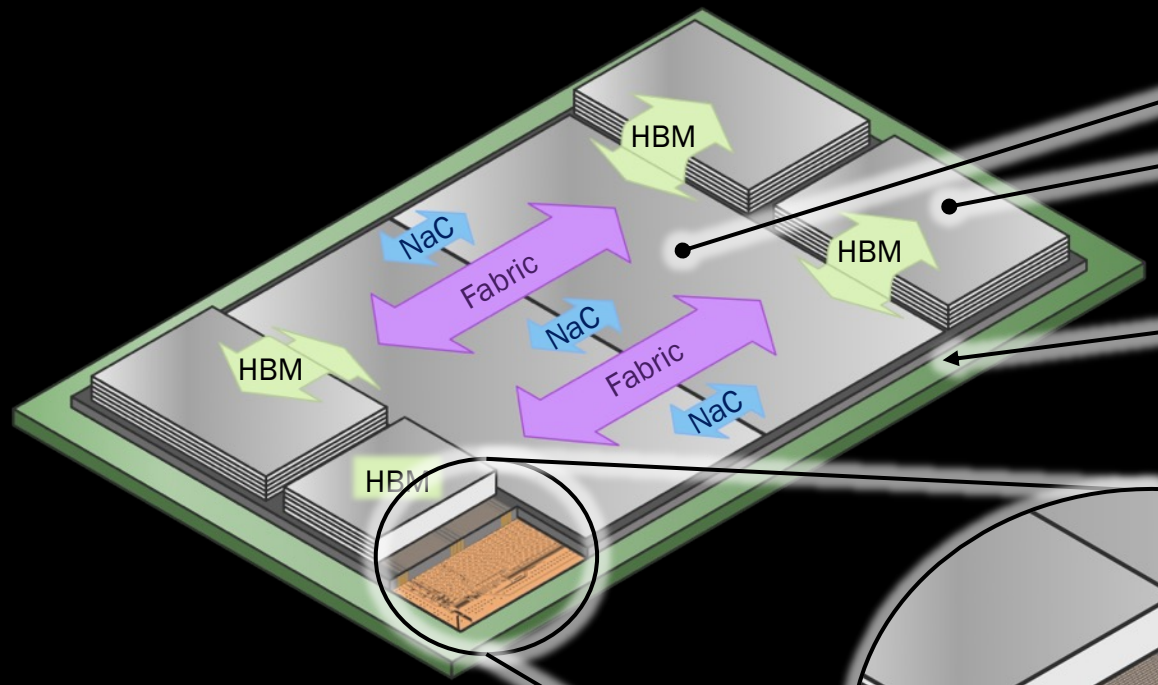
Ultra-short die-to-die channel length for high efficiency



DECA

HPC, AI & FPGA – without Si interposer

Combine the benefits of chips-first & chips-last for 3D integration



High bandwidth memory (HBM) integration

- Chips-first processor die
- Chips-last HBM stacks

Larger-than-reticle fan-out module

- No reticle limit with Adaptive Patterning
- Balanced structure to minimize warpage

3D through-mold interconnects

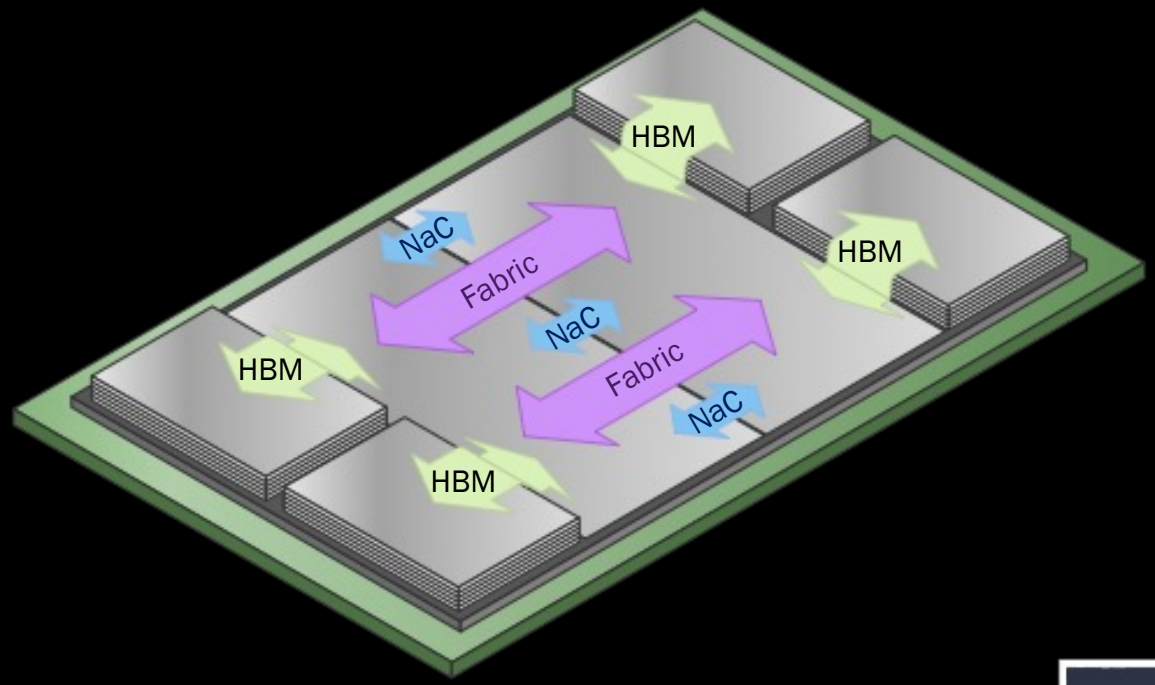
- 20 µm pitch 3D interconnect
- Polymer dielectric for excellent signal integrity

Backside RDL routing to HBM footprint

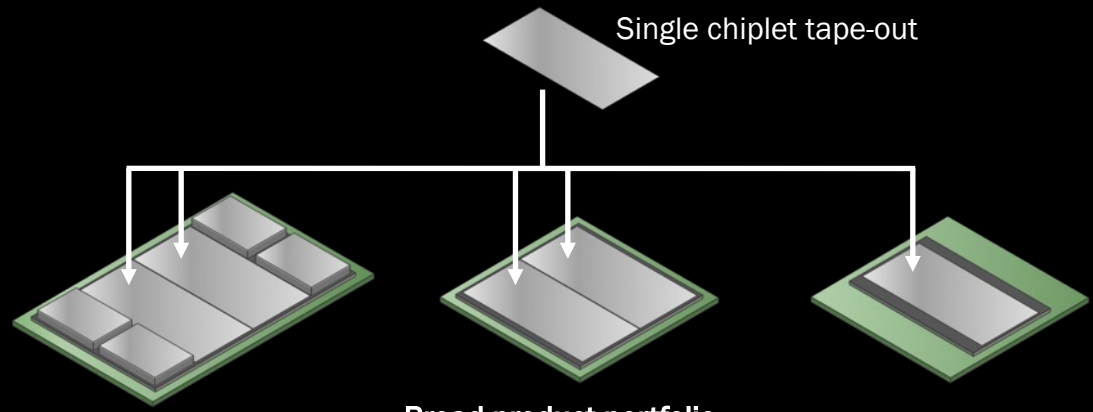
DECA

HPC, AI & FPGA – without Si interposer

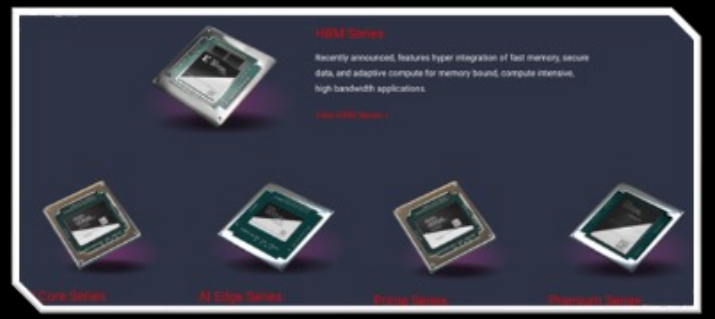
Fan-out RDLs become part of the chip itself



Scalable to create a product portfolio



Broad product portfolio
with a single silicon tape-out



For example:
FPGA vendors offer wide portfolios to address varying applications

For example, the AMD Versal family alone has **> 35 SKUs** [3]

[3] "Versal Architecture and Product Data Sheet: Overview". AMD. https://docs.xilinx.com/v/u/en-US/ds950-versal-overview

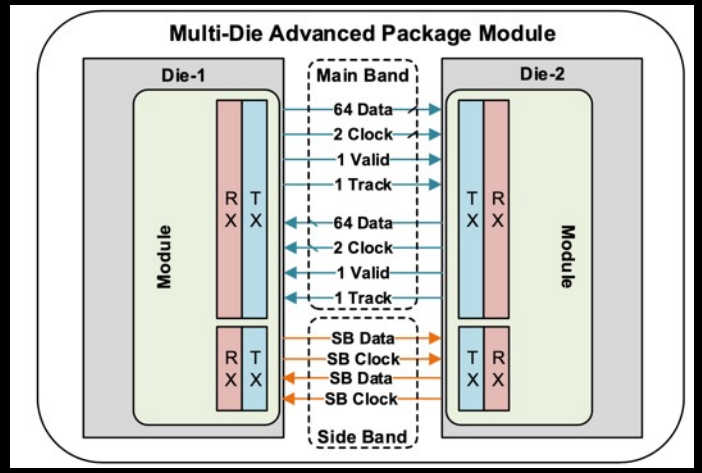
DECA

Outline

- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

Die-to-die interface standards are solidifying

Major die-to-die standards so far (e.g. UCIe, BoW, AIB) use SerDes and clock-forwarded architectures

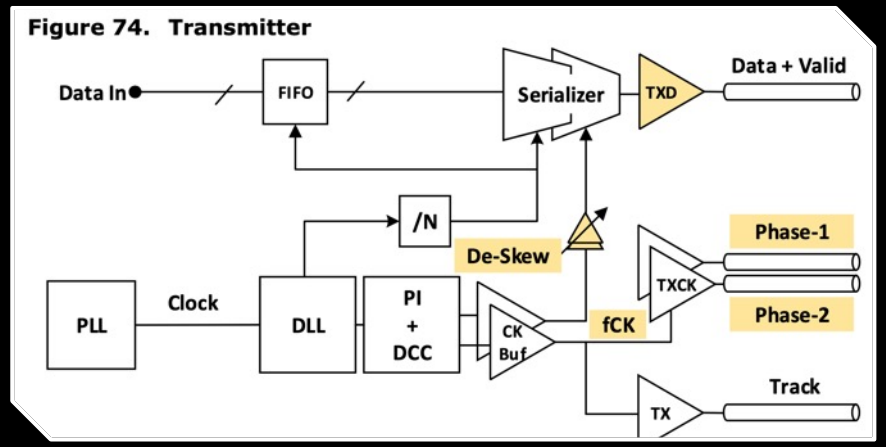


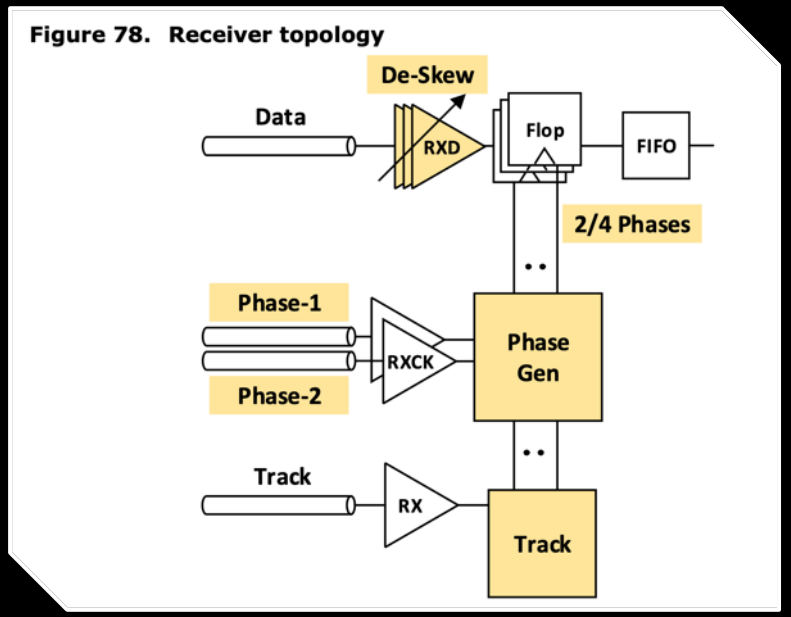
Pros:

- Interoperability between different chiplet vendors
- High bandwidth – 658 GB/s/mm @ 16 Gbit/s UCIe
- Minimizes PVT matching challenges

Cons:

- Power consumption, 0.25–0.6 pJ/bit, IO+PHY)
- Latency, ≥ 12 cycles (UCIe)
- Area & complexity – 3rd party IP, protocol layer, IO, PLL, DLL





PLLs, DLLs, de-skew, tracking, Pi, DCC all affect efficiency (pJ/bit)

DECA

Deca released for Chiplet Summit 2023

Can't die-to-die wires look just like chip wires?

Yes, with a little help for clock distribution

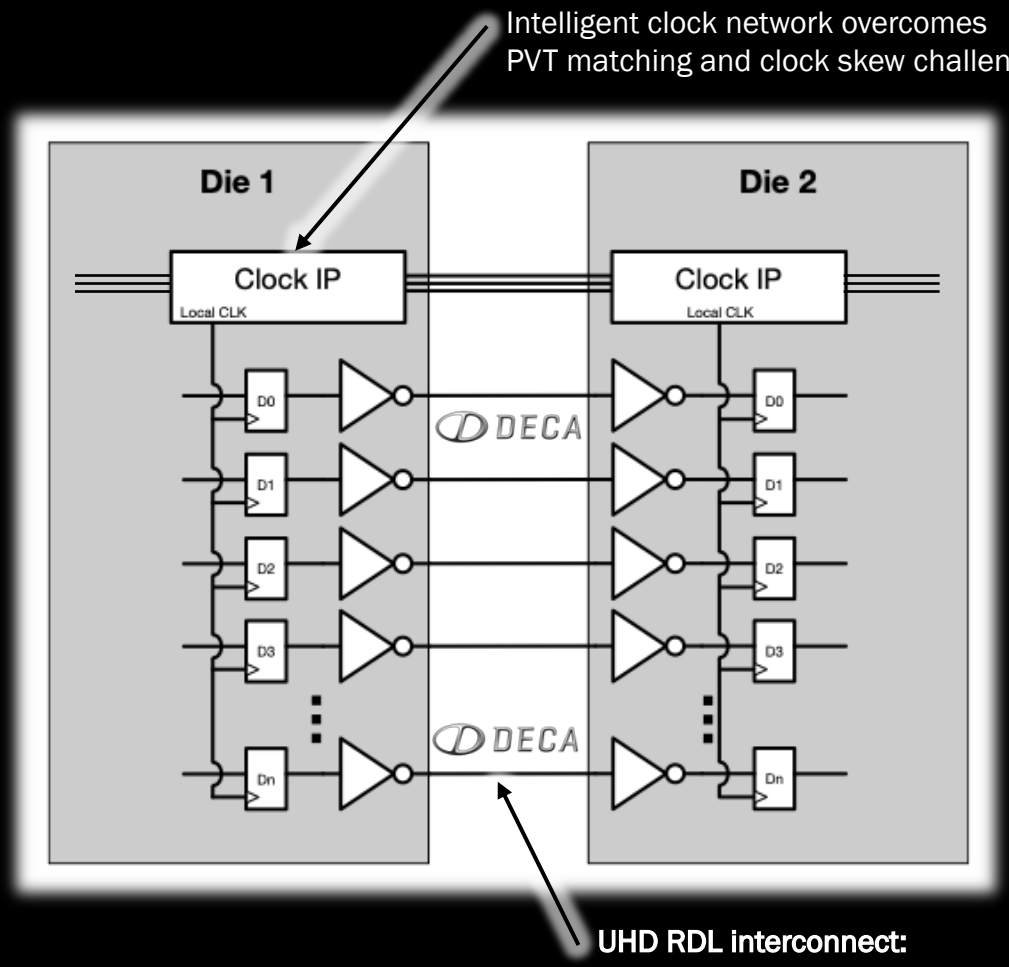
With 3rd-party intelligent clock IP, each die generates a local clock compensated for skew & PVT

Pros:

- Energy efficiency, **< 0.1 pJ/bit**
- Lowest latency
- Minimal area & complexity
- High bandwidth
  - 288 GB/s/mm – Gen 2 M-Series
  - > 768 GB/s/mm – Gen 3 MDx
- Extends network-on-chip (NoC) into a network-across-chiplets (NaC)

Cons:

- Short link length, < 1mm
- Non-standard

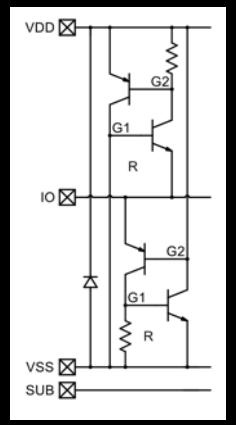


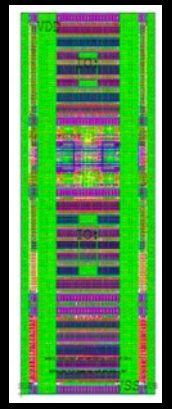
DECA

ESD protection has large impact on efficiency

Capacitance from ESD protection is a significant factor for energy efficiency

ESD capacitance on both die can be larger than wire capacitance

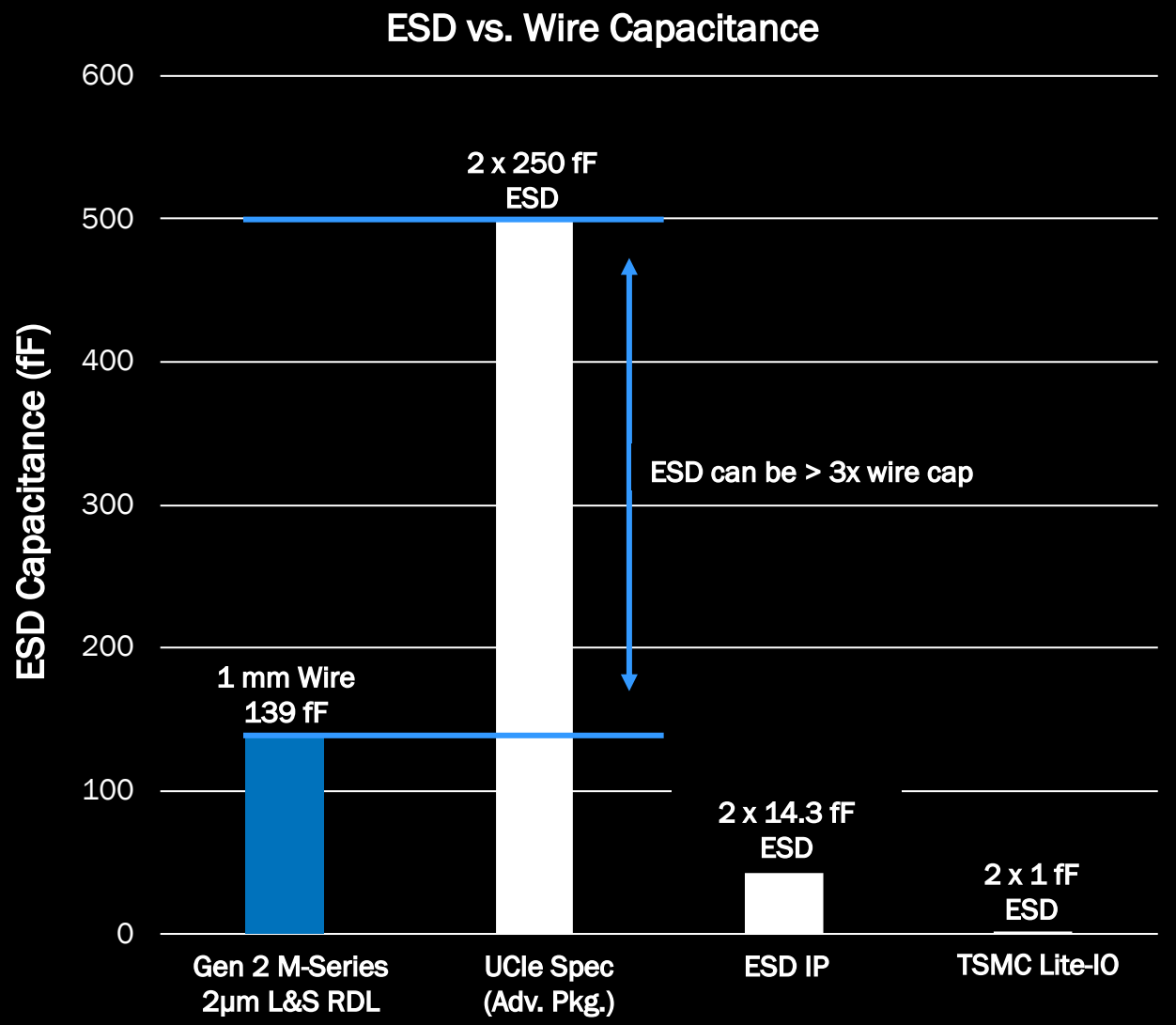




SOFICS
SOLUTIONS FOR ICS

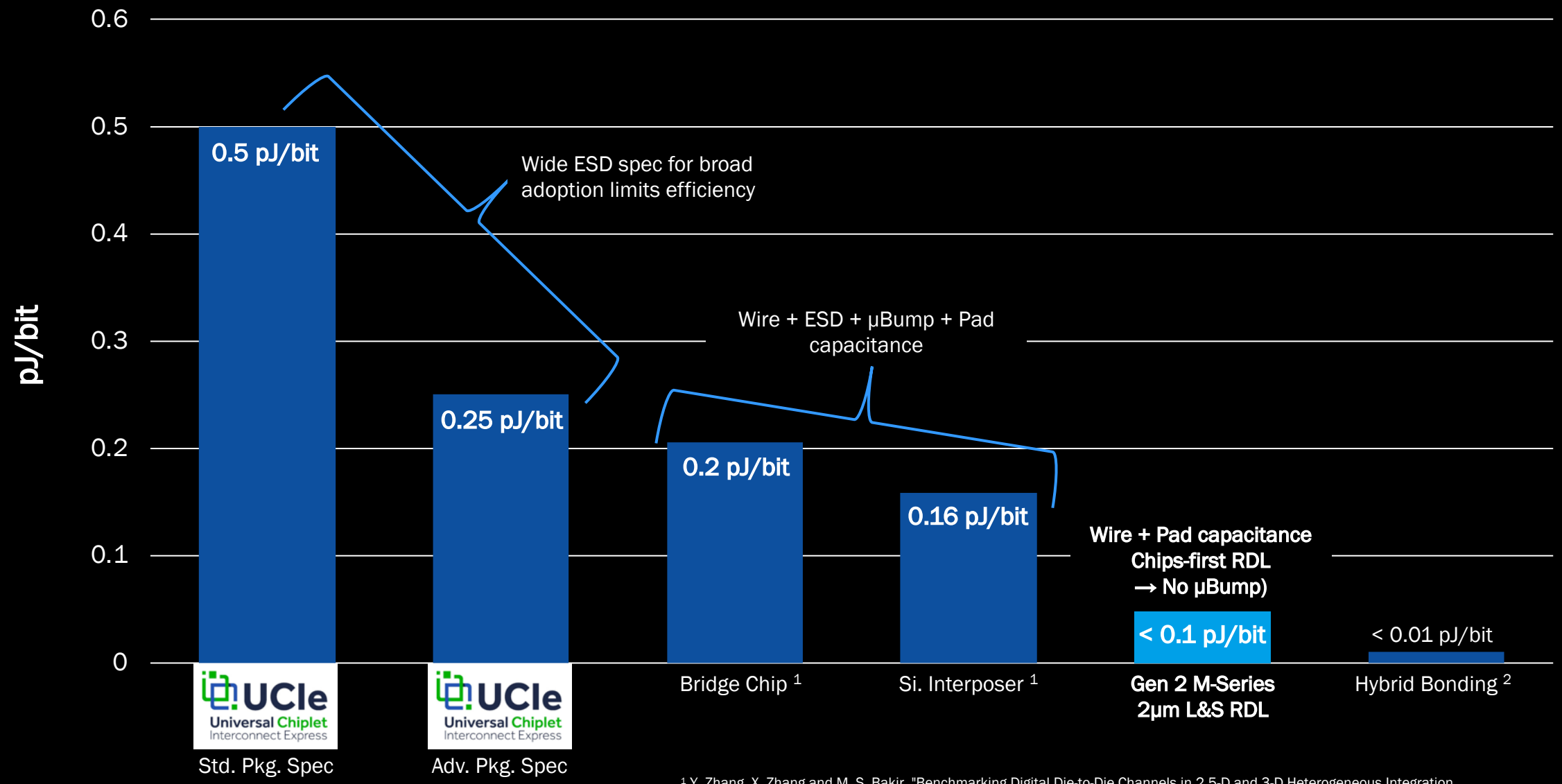
Process: TSMC N7 FF – GOX2 = 1.8V
Used Metals: 7 metals
Special Layer required: Deep Nwell
Area: 156.62µm² (7.426µm x 21.09µm)

Example ESD IP for TSMC N7 from Sofics



DECA

What kind of energy efficiency is possible?



[1] Y. Zhang, X. Zhang and M. S. Bakir, "Benchmarking Digital Die-to-Die Channels in 2.5-D and 3-D Heterogeneous Integration Platforms," in IEEE Transactions on Electron Devices, vol. 65, no. 12, pp. 5460-5467, Dec. 2018,

[2] Y. . -K. Cheng et al., "Next-Generation Design and Technology Co-optimization (DTCO) of System on Integrated Chip (SoIC) for Mobile and HPC Applications," 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2020, pp. 41.3.1-41.3.4.

DECA

Outline

- Introduction
  - Fan-out fundamentals
  - Traditional applications
  - Process overview
  - Adaptive Patterning
- Next-gen applications
  - Motivations
  - Fan-out for heterogenous integration
  - Examples
  - Beyond “packaging”
- Summary

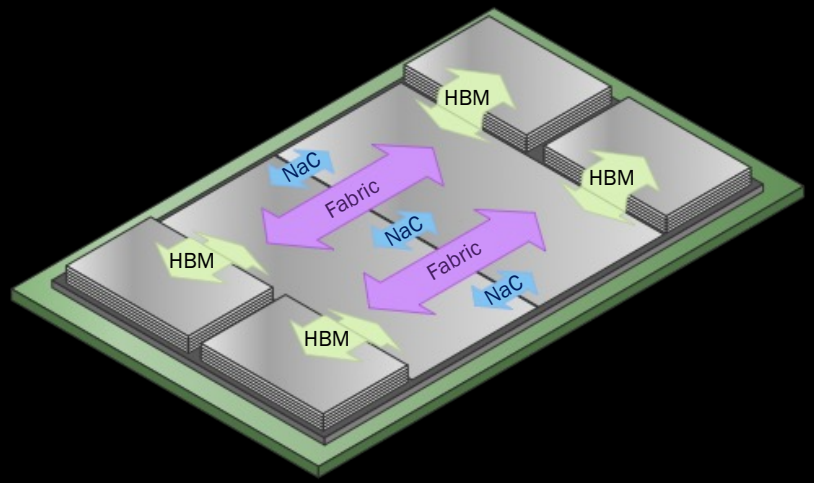
Summary

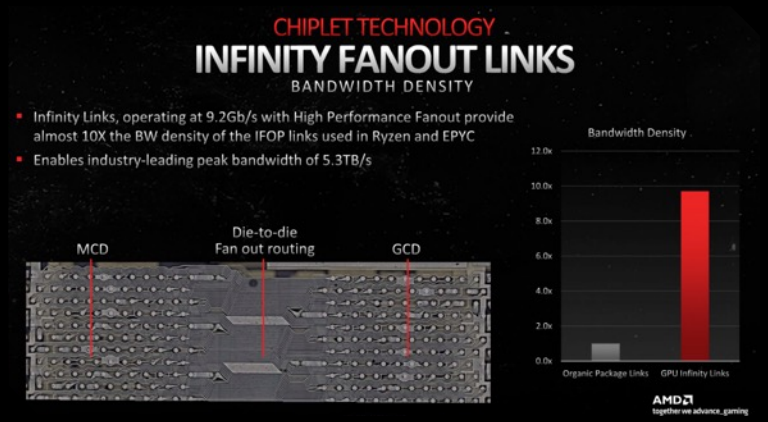
Leading-node cost per yielded mm^2 silicon increasing

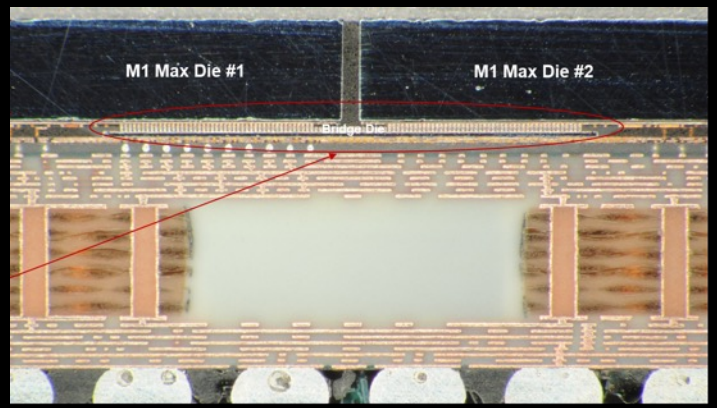
Competing interests

Demand for more compute & memory per package insatiable

→ More die connected with ~~"packaging"~~ interconnect technologies







DECA

Thank you from