Heterogenous Package Thermal Characterization and Modeling

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Agenda

Introduction

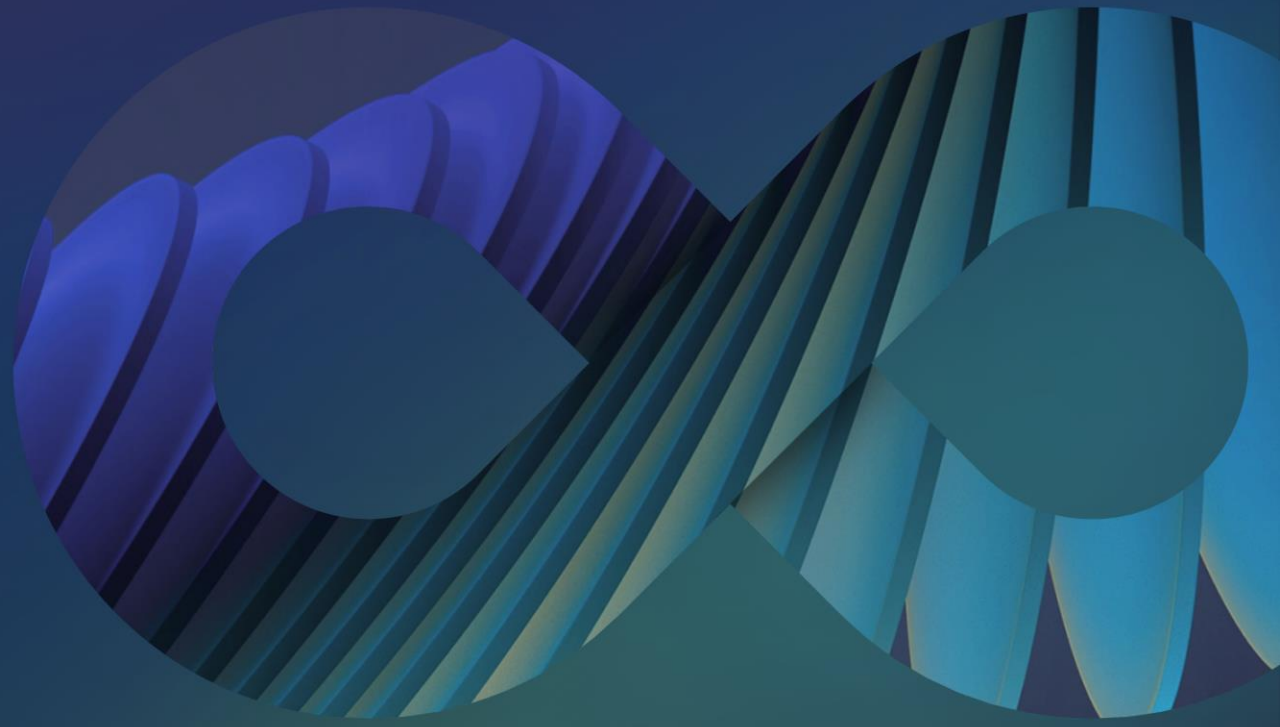
Thermal Transient Test approach

- Body diode
- I/O Pin
- TTV

Structure Functions

Application examples

Potential next steps



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Introduction

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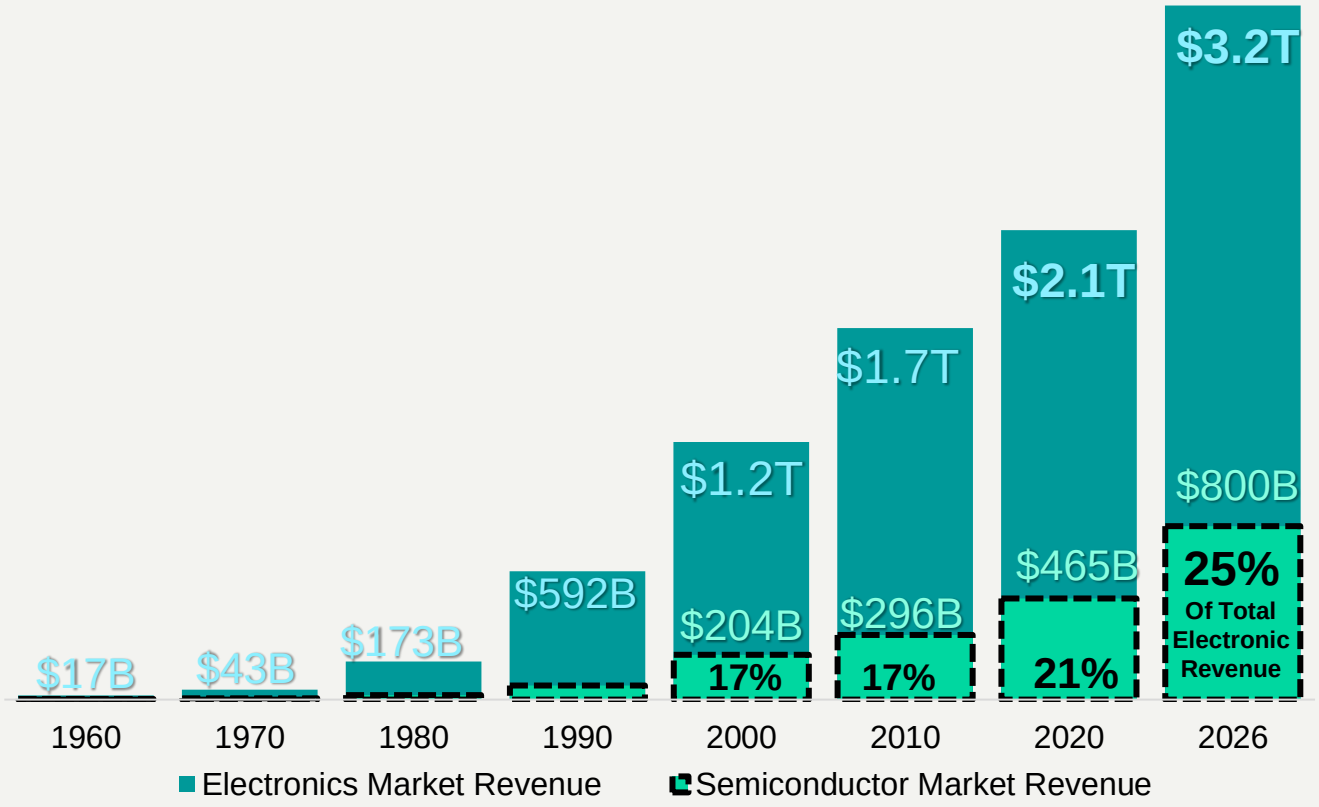
Increasing Semiconductor Content in Electronics Systems

Tightly linked to future Electronics growth areas



Source: VLSI Research, September 2021

The increasing amount of semiconductor content in electronic systems is enabling innovation and driving system value growth

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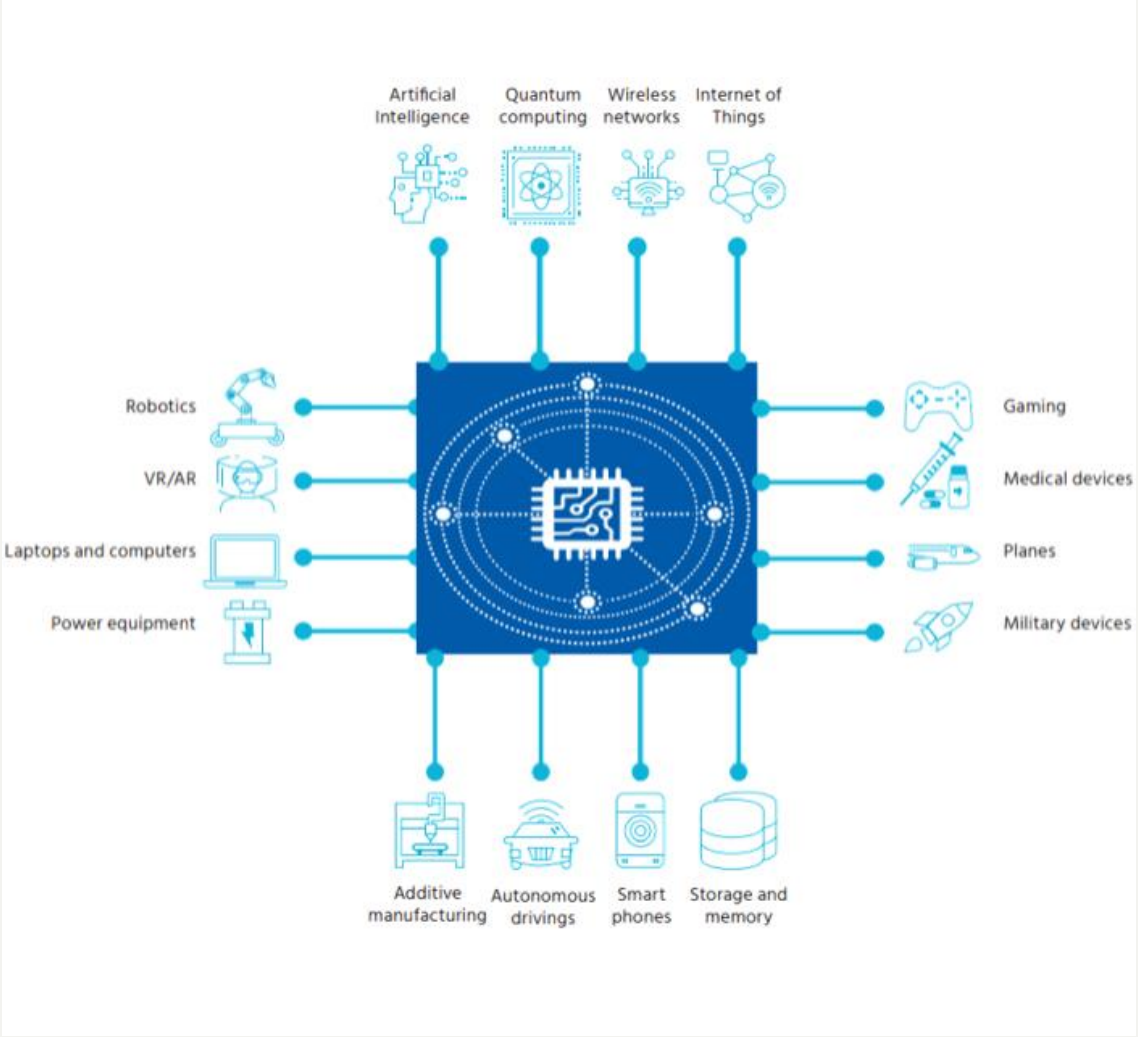
Current Market Drivers in Electronics

- 5G wireless network deployment will see major footprint in cars´ connectivity
- Renewables faces governments´ focus with the new climate agreements
- The slow adoption of electric vehicles is facing a turnaround
- Businesses using IoT technologies from 13 % in 2014 to 25 % in 2020
- AI/ML applications are increasing needs for HPC



Consumption of semiconductors per person in China:
$16.72 per person in 2010
$85.22 in 2020 (+5.10X) (IBS)

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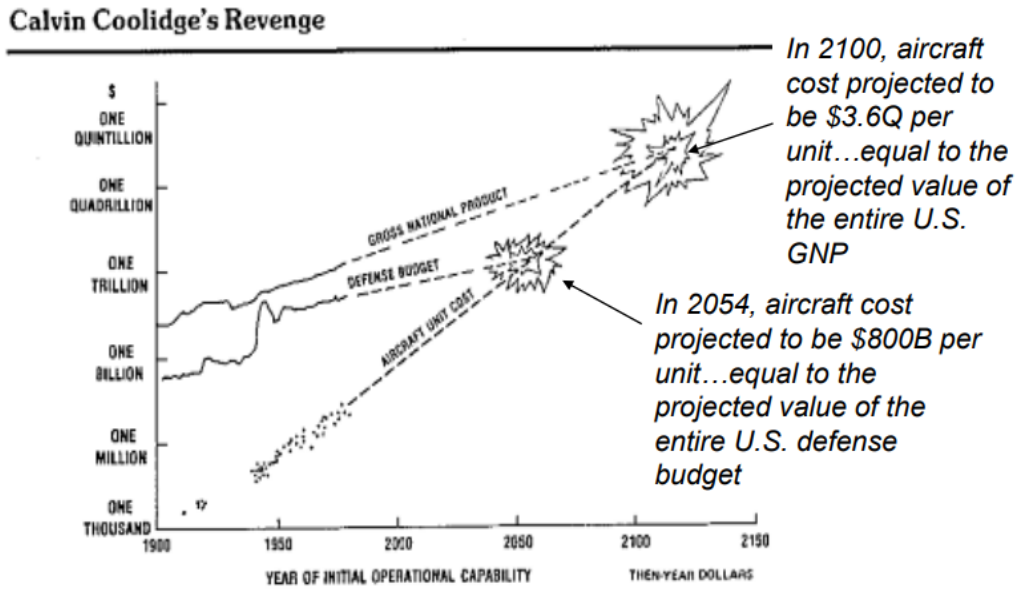
Learning from other industries

"In the year 2054, the entire defence budget will purchase just one aircraft."

- If the U.S. defense budget grows by 2.5% per year…
- If nominal gross national product grows by 5.5% per year….



Integrate, then build!

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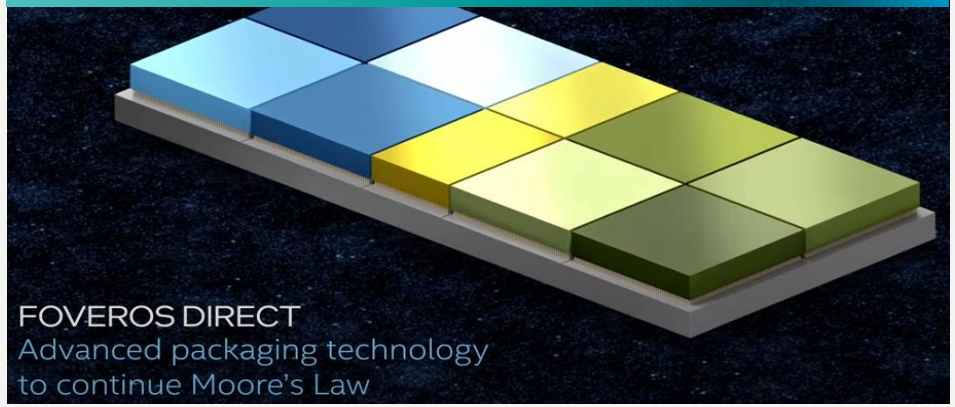
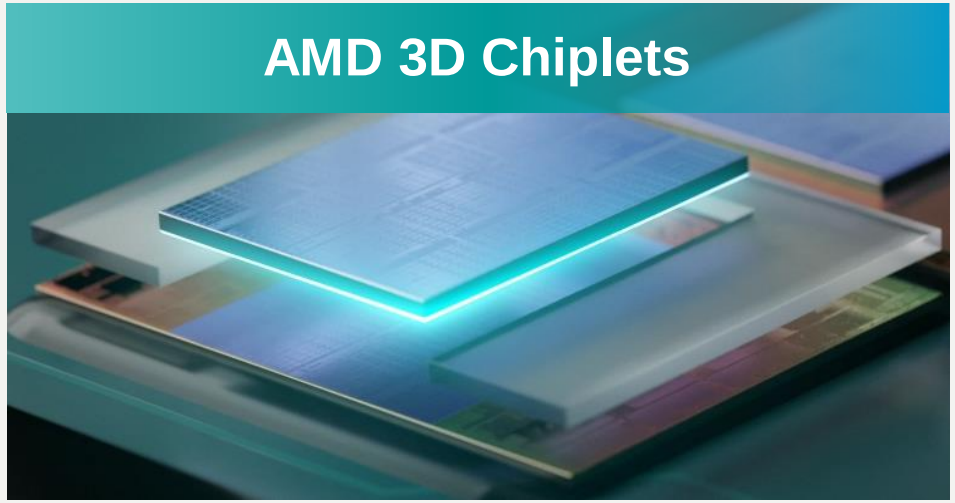
Getting More out of Moore's Law
with High Density Advanced Packaging

Intel Foveros Direct



TSMC 3D Fabric

AMD 3D Chiplets



New Protocols

Universal Chiplet Interconnect Express

Building an open ecosystem of chiplets for on-package innovations

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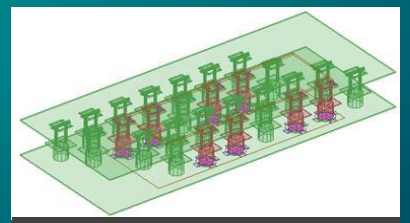
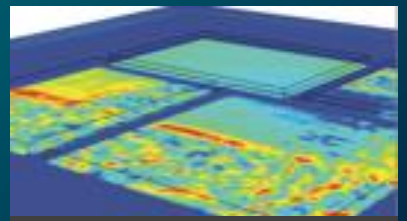
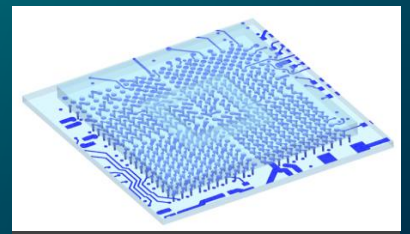
New Challenges Presented by New Frontiers



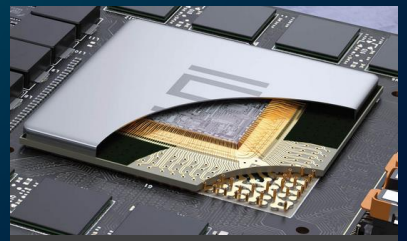
Power Delivery



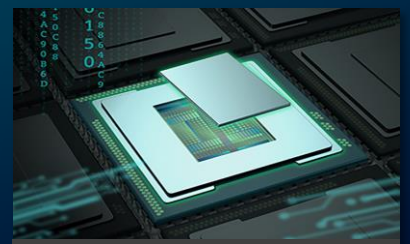
Thermals



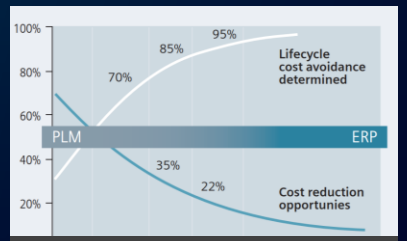
Mechanical Stress



Material Characterization



System Integration



Lifecycle Management

Semiconductor Lifecycle Management

- Electrical Design
- Mechanical Design
- Analyze
- Optimize
- Test/Calibrate

End to end toolchain

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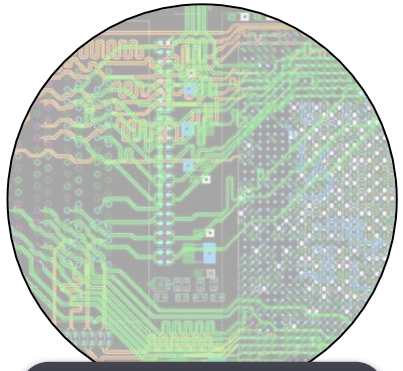
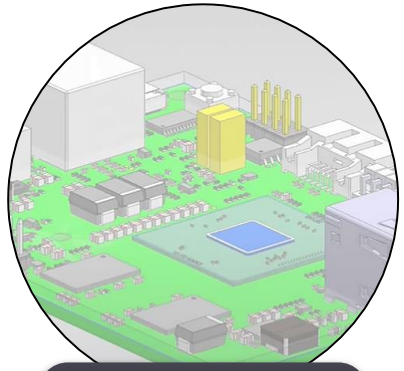
Integrated Advanced Packaging Design Workflow



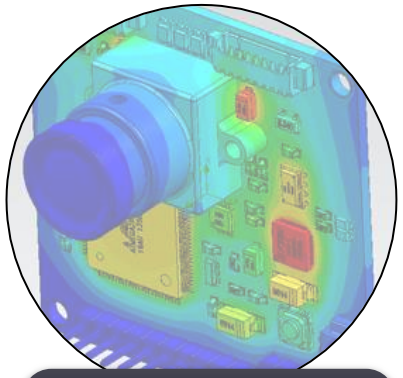
Electrical Design

(Xpedition / XSI /XPD)



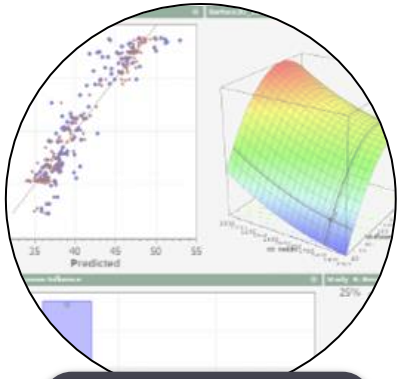
Mechanical Design

(NX Platform)



Analysis
Electrical, Thermal, & Mechanical Analysis

(NX - Simcenter)



Optimization

(HEEDS)

Testing & Calibration

(T3ster, MicReD, TeraLED)

Product Lifecycle Management

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Thermal Measurements

Basics

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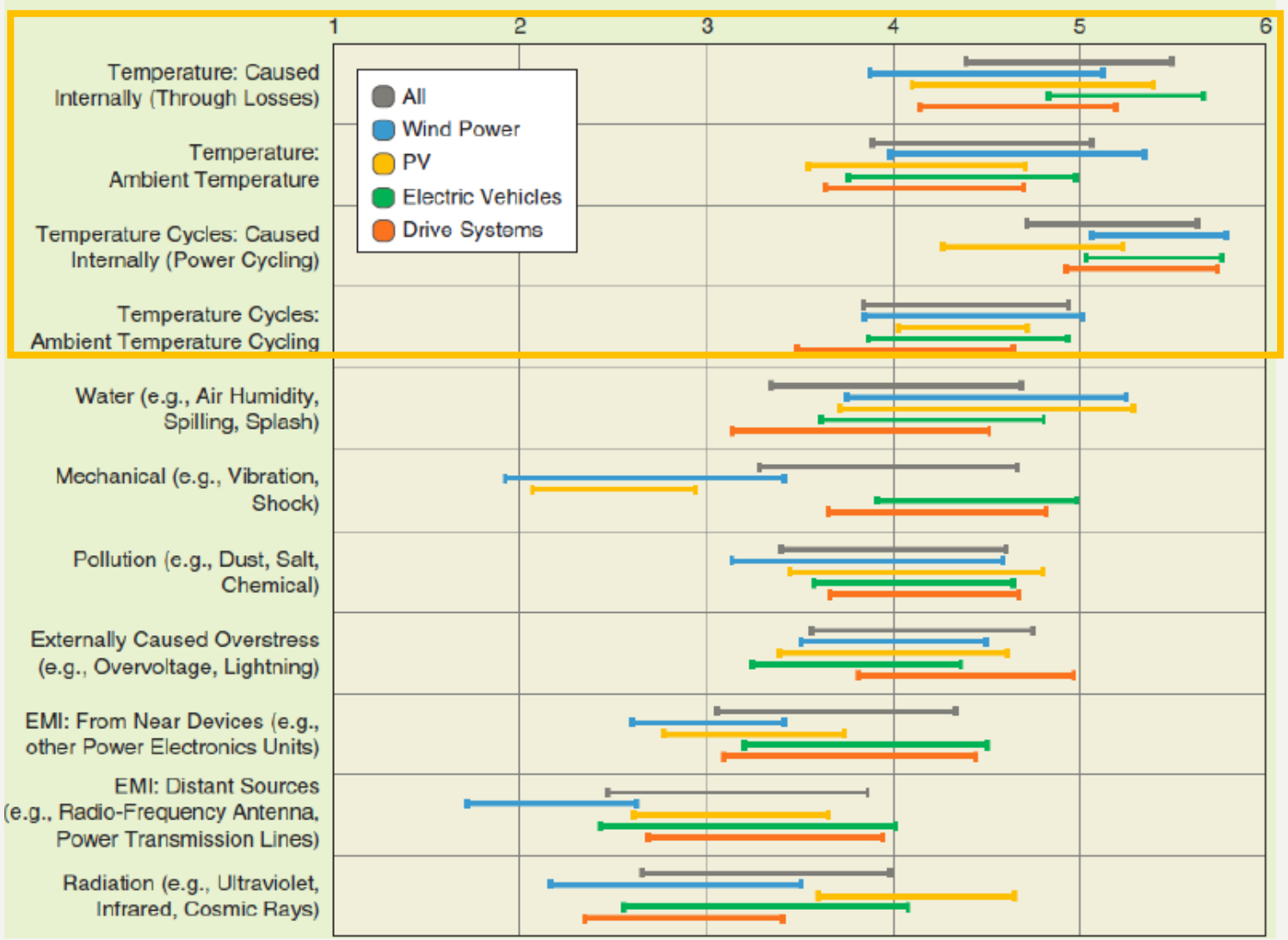
Temperature Factors - Main Threat to Reliable Operation



Temperature related issues have highest votes

Source: J. Falck, C. Felgemacher, A. Rojko, M. Liserre and P. Zacharias, "Reliability of Power Electronic Systems: An Industry Perspective," in IEEE Industrial Electronics Magazine, vol. 12, no. 2, pp. 24-35, June 2018.

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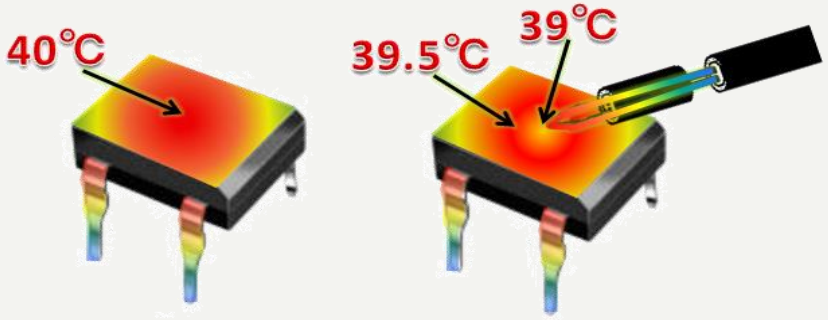
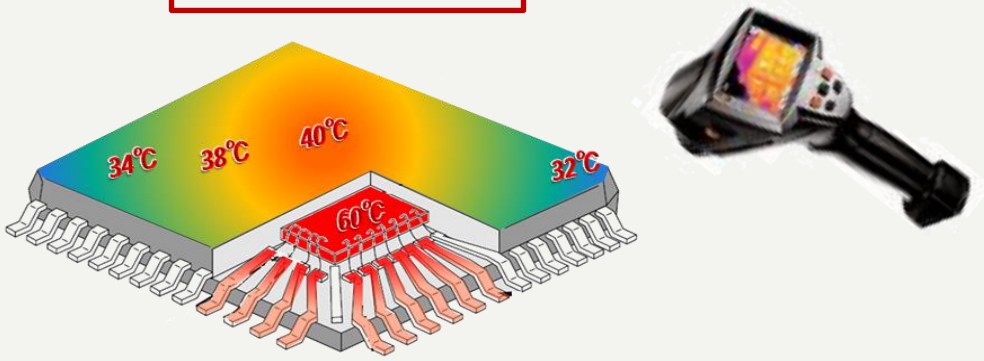
Traditional Measurement Solutions

Thermocouples



IR camera



- Simple and generally available methods
- Only surface temperature (Thermocouples, IR camera)
- Effect by thermocouple itself or surface, emissivity and absorptivity
- Require access to the die to measure junction temperatures

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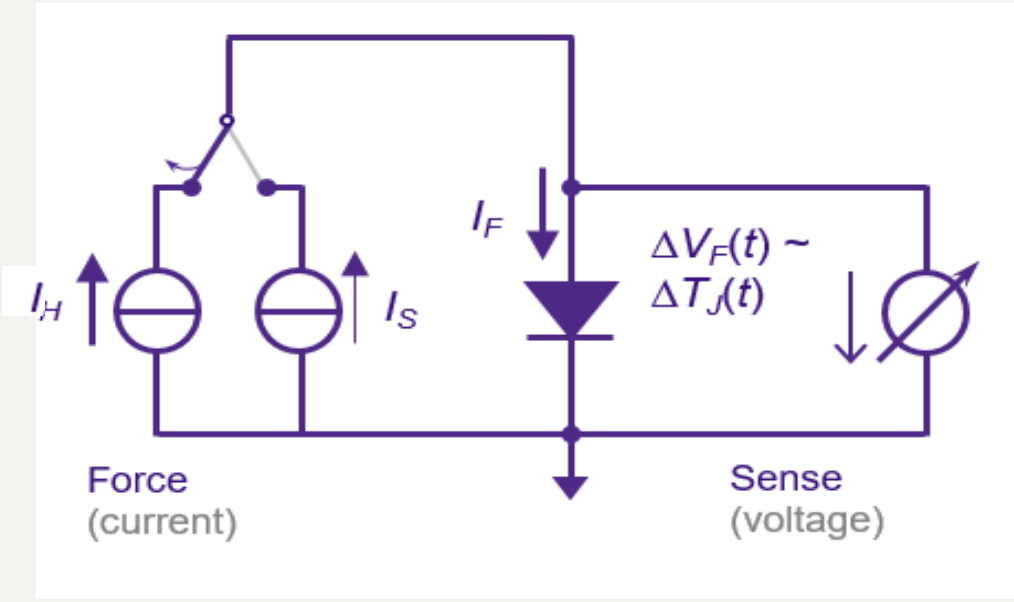
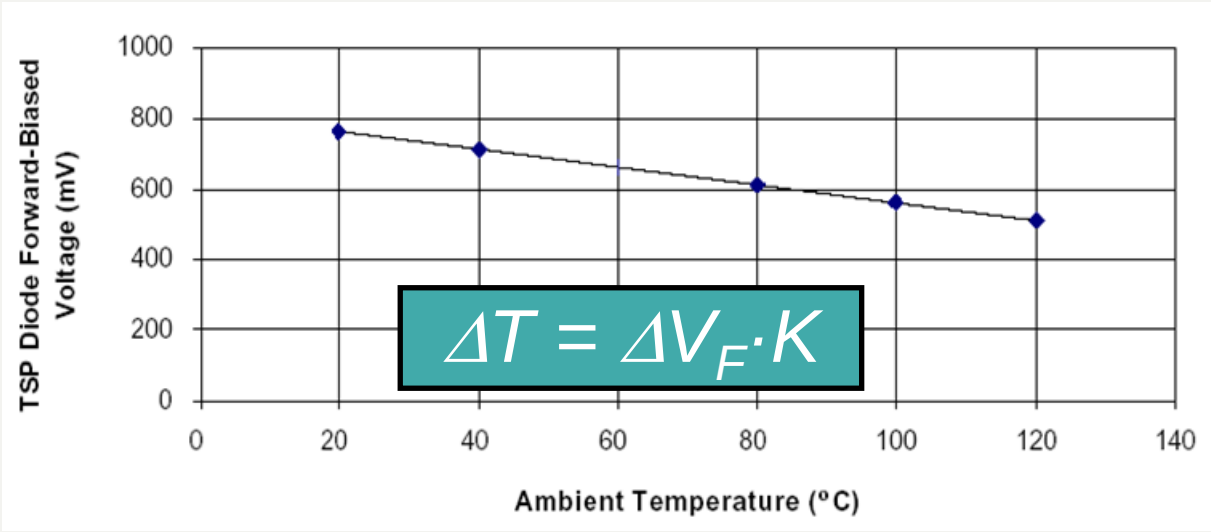
Accurate Junction Temperature Measurement

- The forward voltage of a PN junction under forced current condition can be used as a very accurate thermometer

- The change of the forward voltage (TSP – temperature sensitive parameter) should be carefully calibrated against the change of the temperature (see JEDEC JESD51-1 and MIL-STD-750D)
  - In the calibration process the S_{VF} temperature sensitivity of the forward voltage is obtained





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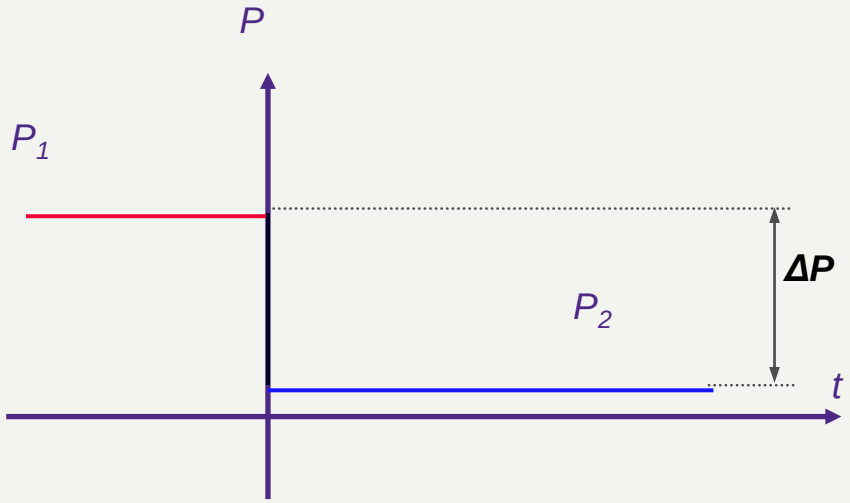
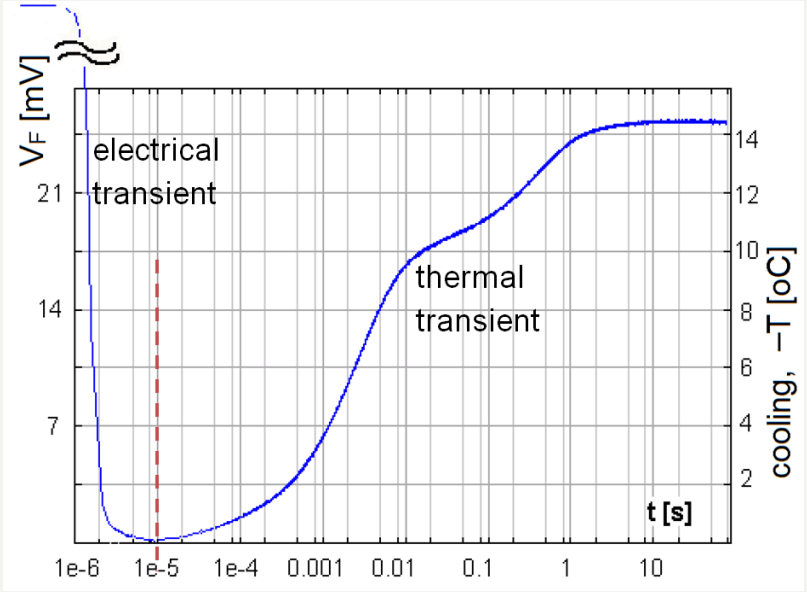
How is the Measurement Done?

- Static test method (JEDEC JESD 51-1 standard)
  Very fast switching between heating and sensing states
- Fast measurement at “junction” to capture time constants
- High temperature resolution: 0.01°C in practice
- 4-wire setup (Kelvin setup) for better power accuracy





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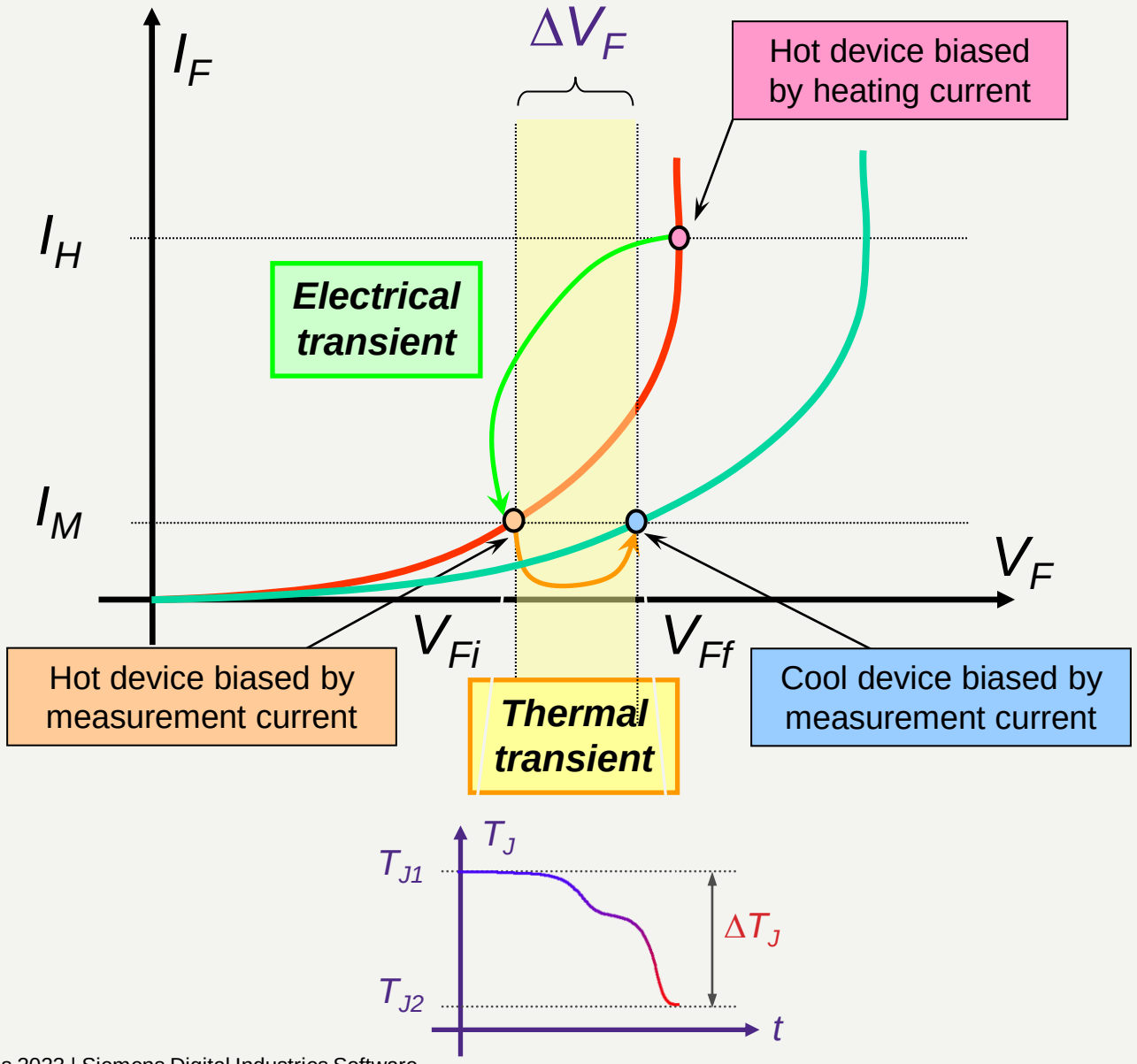
How is the Measurement Done?



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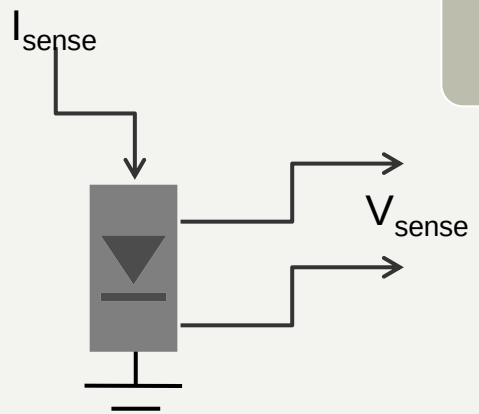
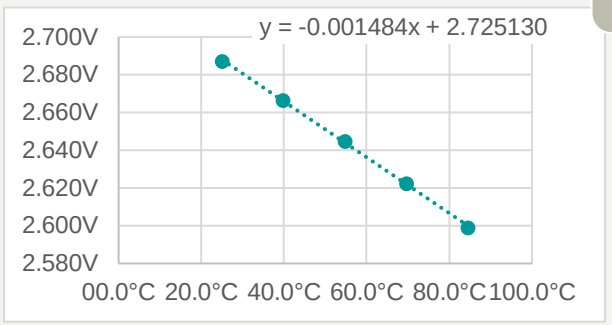
What preparations are necessary for a test?

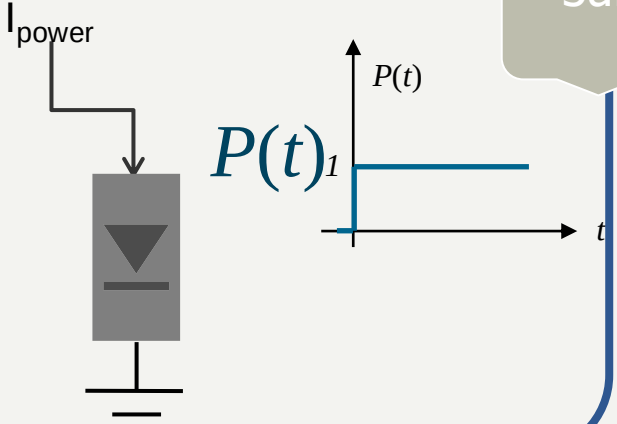
1. Find the TSP



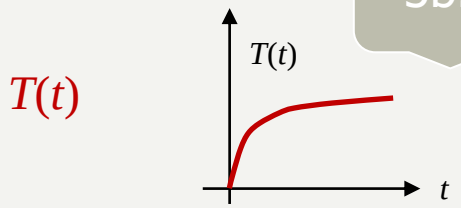
2. Calibrate



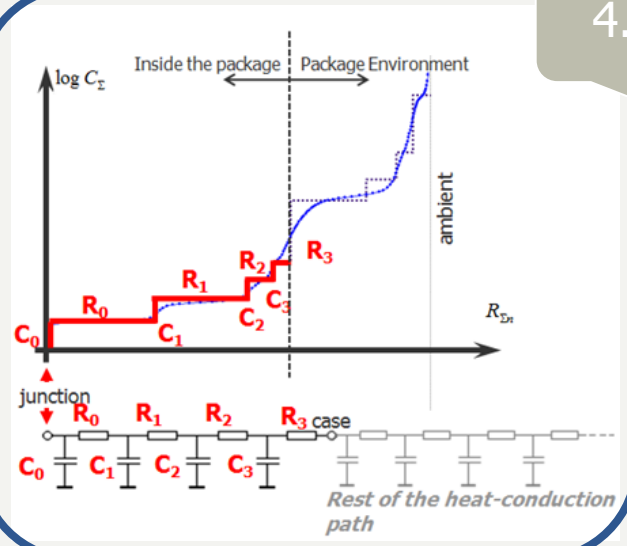
3a. Power Step



3b. Record



4. Analyze



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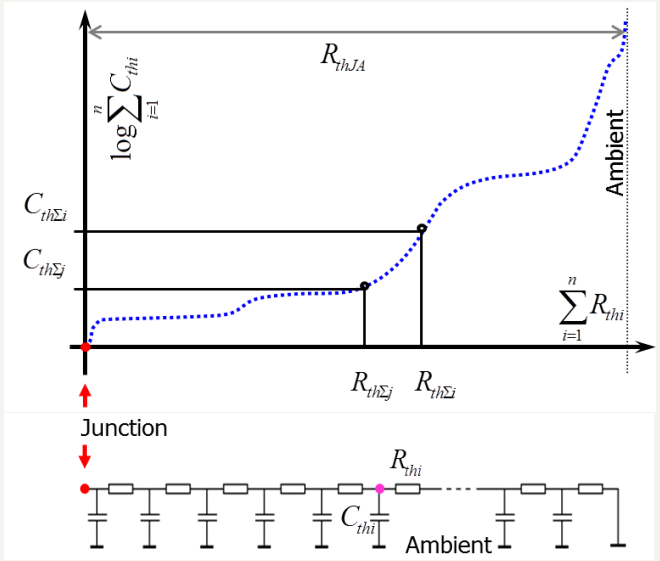
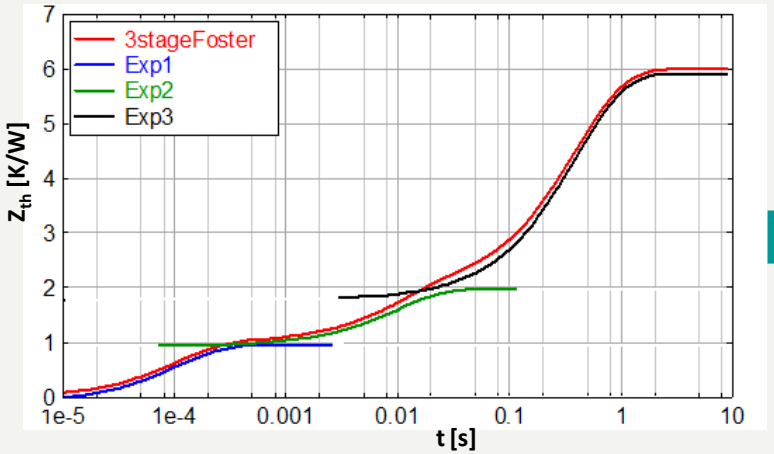
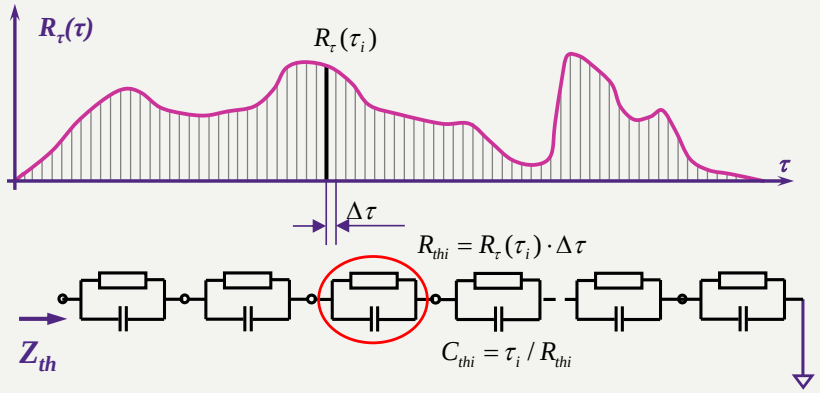
Analyzing the Structure

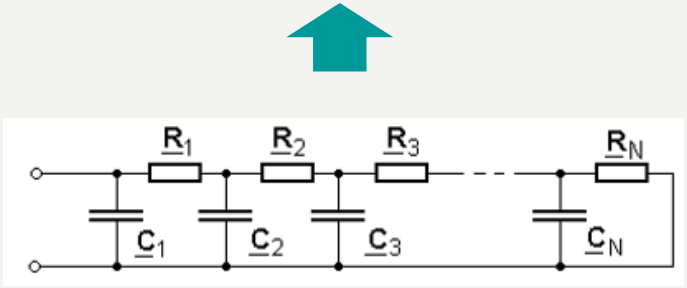




Measure thermal impedance



Time constant spectrum



Foster-Cauer Transformation

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Thermal Measurements

Test environments

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JEDEC standard test conditions

Besides test equipment, standard test conditions need to be provided

test environments

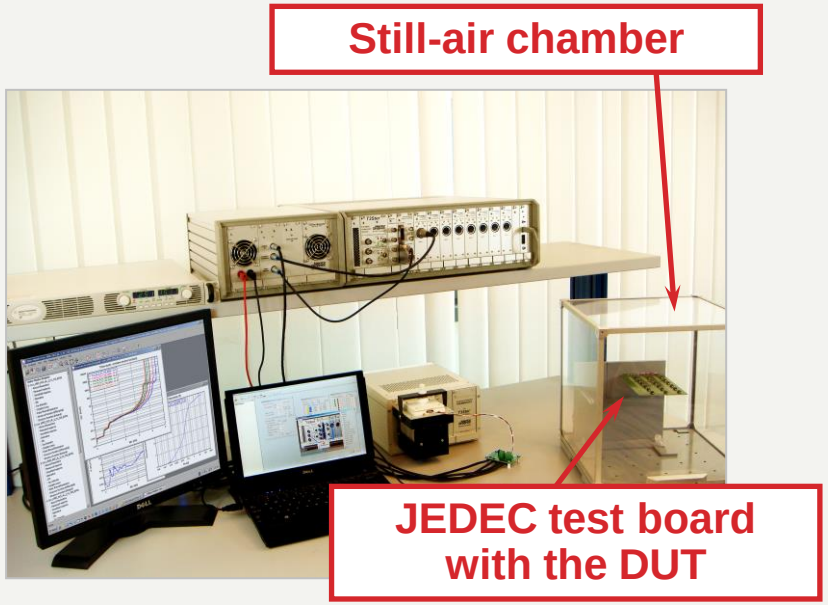
- natural convection
- forced convection
- cold plate

device fixtures / test boards

Natural convection: JEDEC JESD51-2A standard

Forced convection: JEDEC JESD51-6 standard

Different test boards: JEDEC JESD51-3, 5, 7, 10, 11



Source of image
http://www.utacgroup.com/technology_contents_analysis2.html

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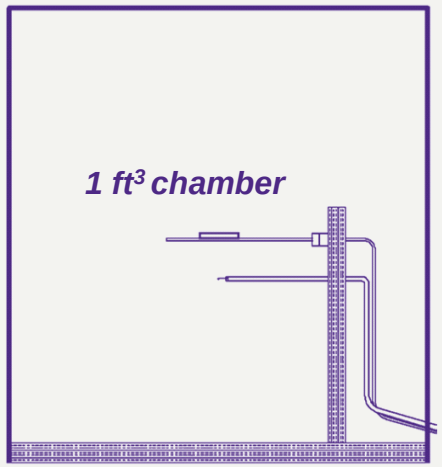
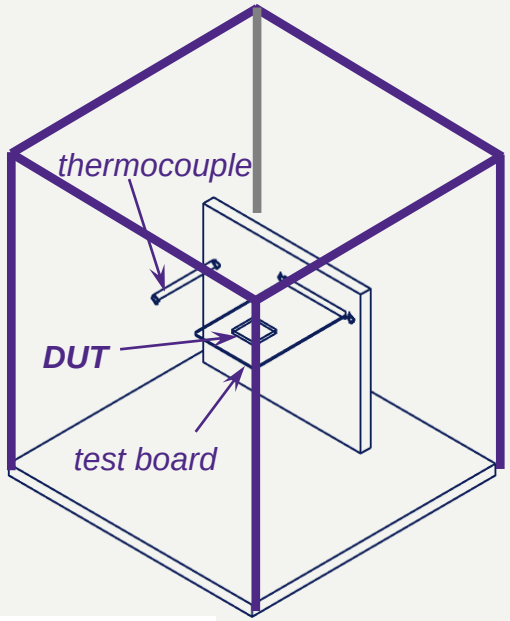
Still-air chamber / test board definitions examples

JEDEC JESD51-2A standard

Low conductivity chamber material (e.g. polycarbonat)





JEDEC JESD51-11 standard

Figure 1a — Cross section of 1s PCB showing trace and dielectric thicknesses in package placement and trace fan-out regions

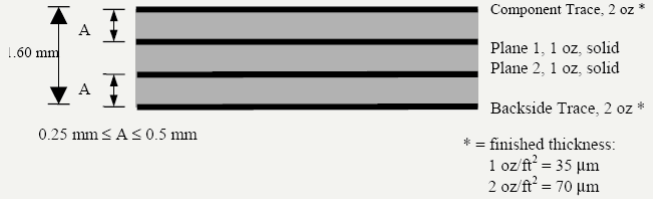


Figure 1b — Cross section of 2s2p PCB showing trace and dielectric thicknesses

Table 1 — PCB sizes for packages

Package Length	PCB Size (+/- 0.25 mm)
Pkg. Length ≤ 40 mm	101.5 mm x 114.5 mm (4.0 in x 4.5 in)
40 mm < Pkg. Length ≤ 65 mm	127.0 mm x 139.5 mm (5.0 in x 5.5 in)
65 mm < Pkg. Length ≤ 90 mm	152.5 mm x 165.0 mm (6.0 in x 6.5 in)

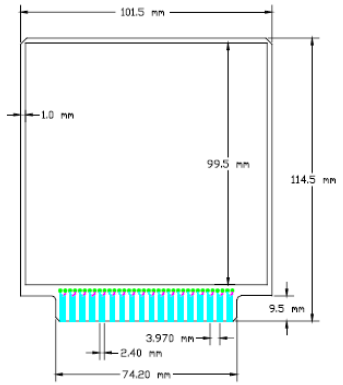


Figure 2 — Example test board outer dimensions and edge connector design

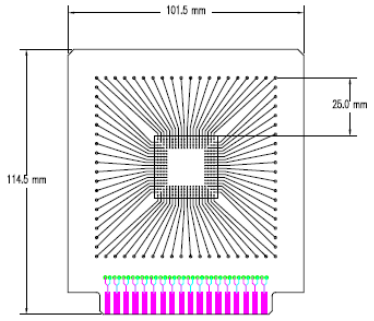


Figure 3 — Traces to outer pin row flared to perimeter 25 mm from package body.

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JEDEC standard test conditions

Test environments

natural convection: 1 ft^3 still-air chamber: **JESD51-2A** (2008)

forced convection: wind tunnel **JESD51-6** (1999)

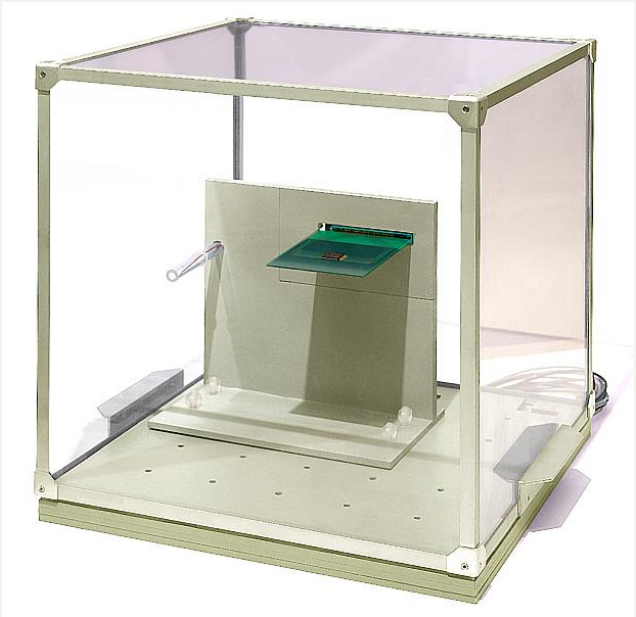
Test boards

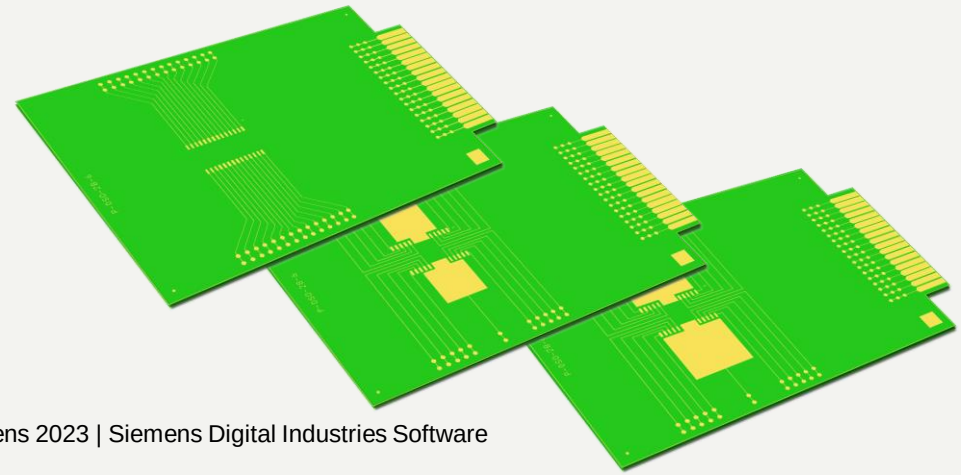
copper coverage / number of layers

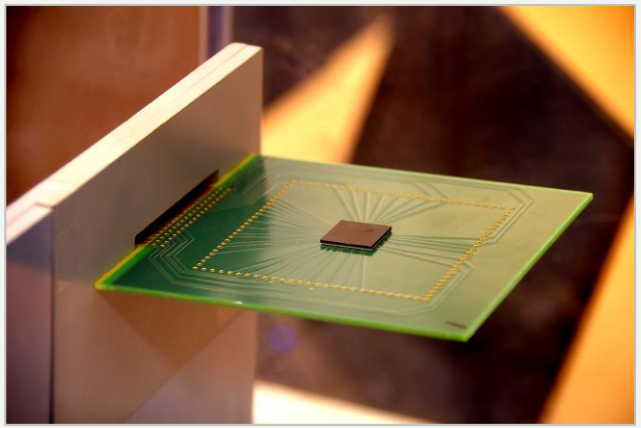
- high / low conductivity, 1s / 2s

different designs mathching different package styles

design / orientation counts a lot, as shown by structure functions







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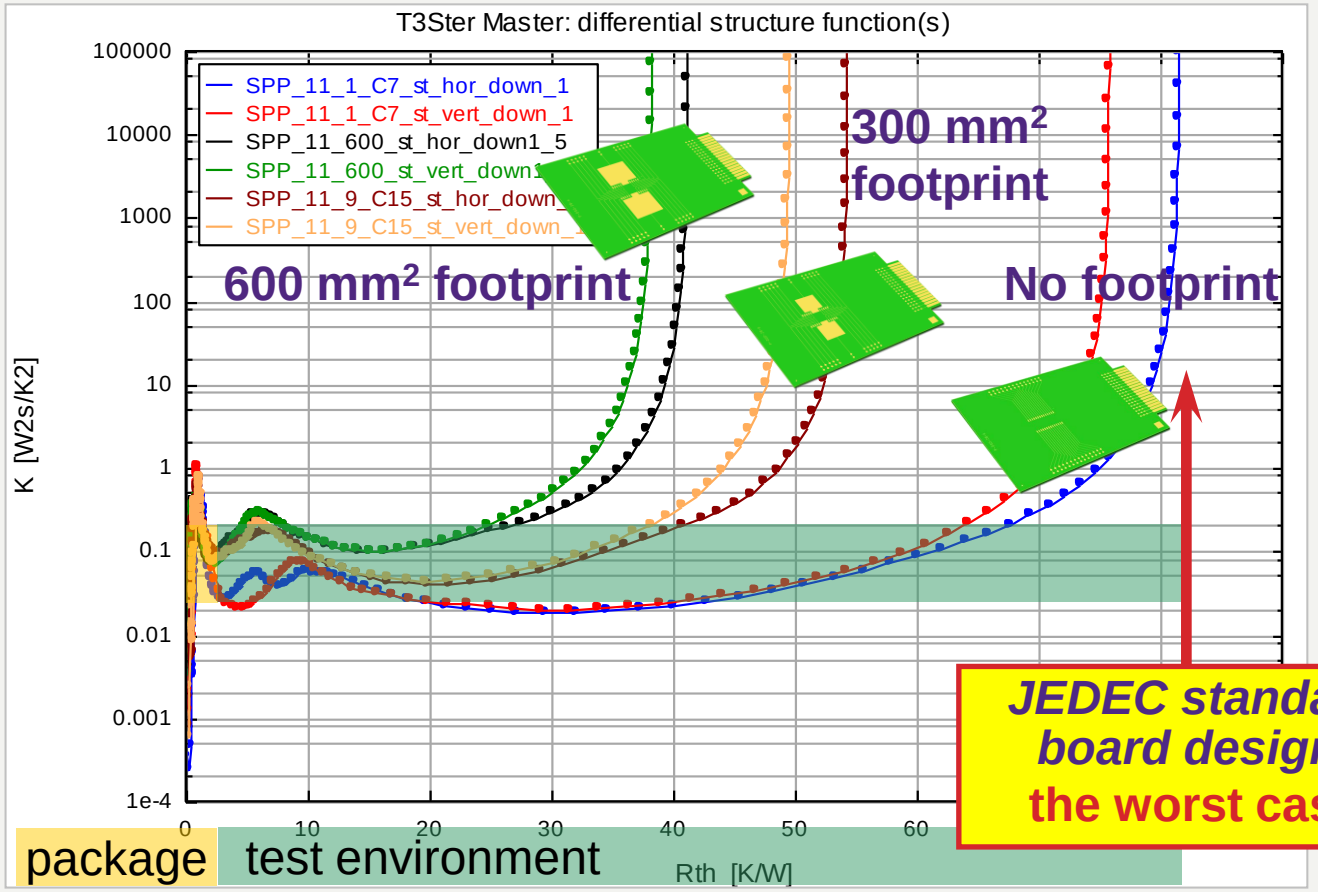
Effect of test board design / orientation

Tests performed in a JEDEC standard still-air chamber

Measured transients converted to structure functions



Board design (Cu area of footprint region) and board position (vertical or horizontal) strongly effects the ultimate R_{thja} value

JEDEC standard board design:
the worst case

- Measured R_{th} is mostly due to the test environment

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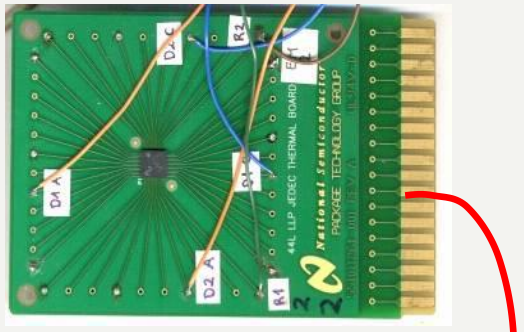
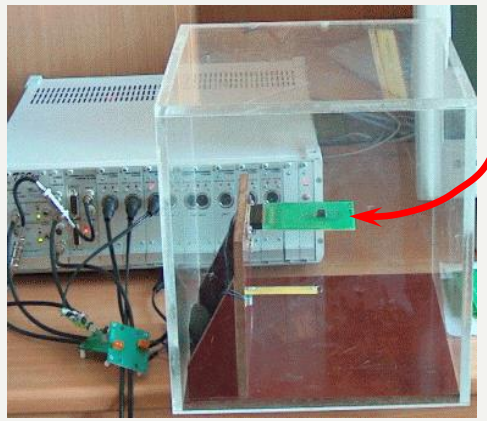
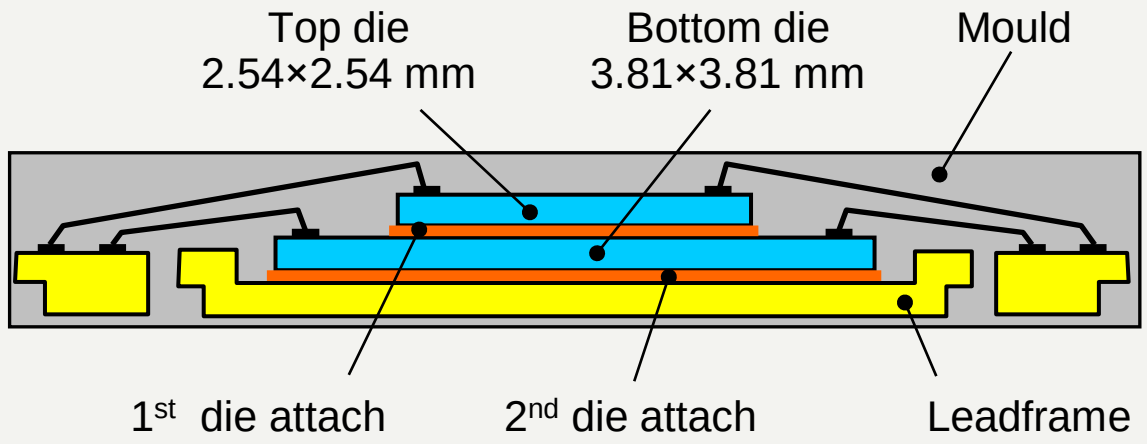
Example: Two live chips stacked in a 44L LLP package

Stacked die package tested in JEDEC standard test environment

Transient extension of the JESD51-1 static test method was used, followed by structure function analysis







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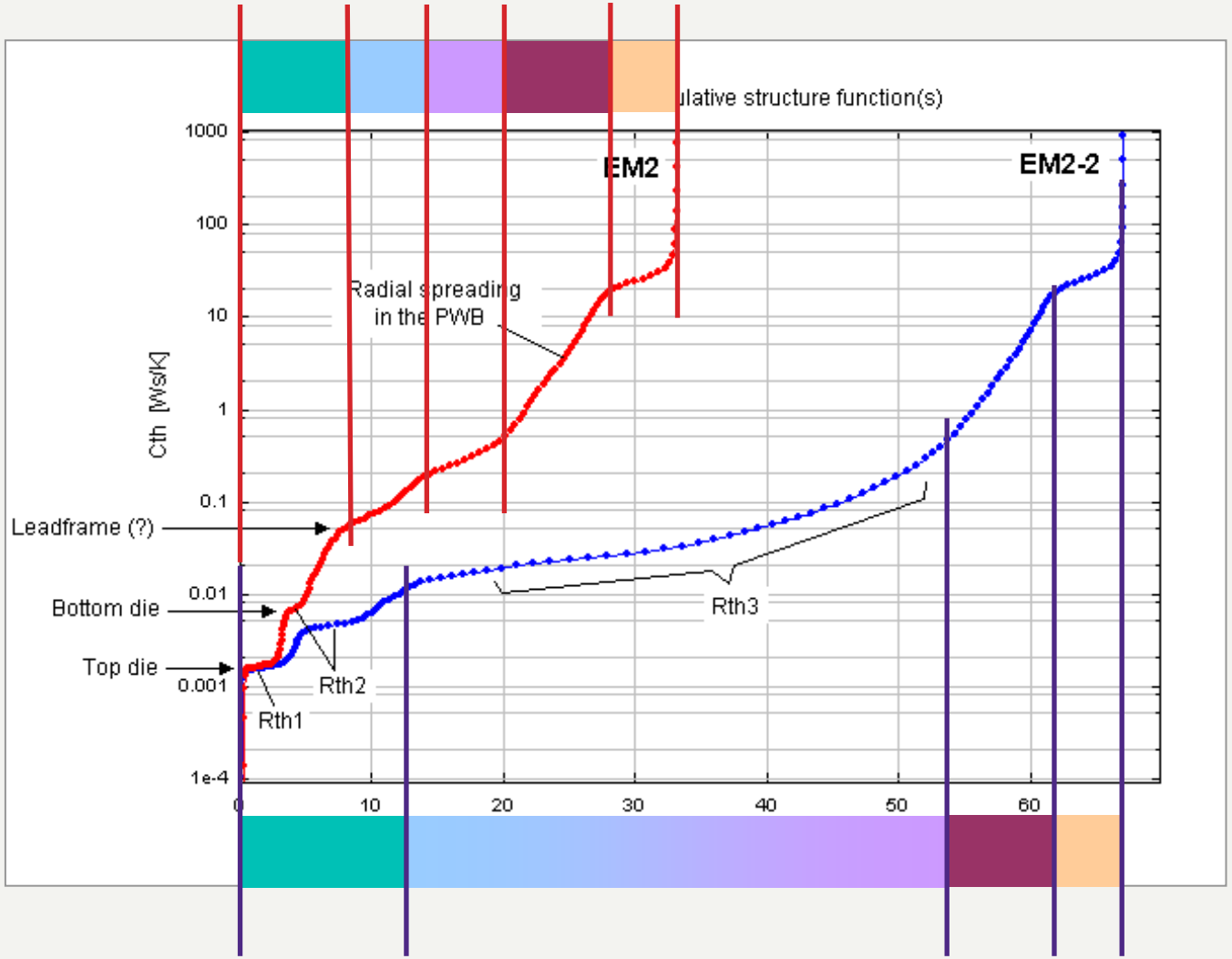
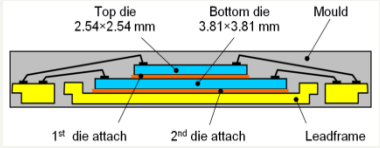
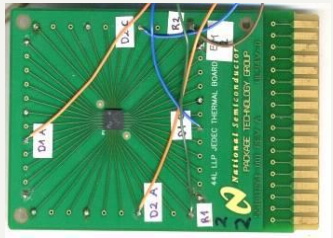
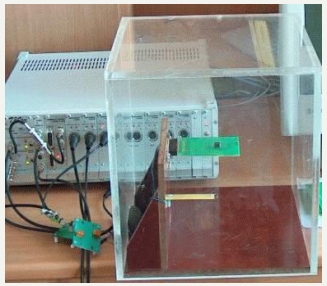
Results in terms of structure functions









Majority of the R_{thja} is caused by the JEDEC standard test environment.

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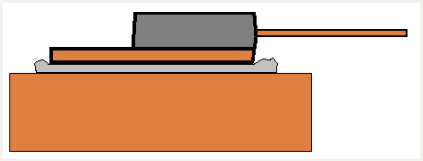
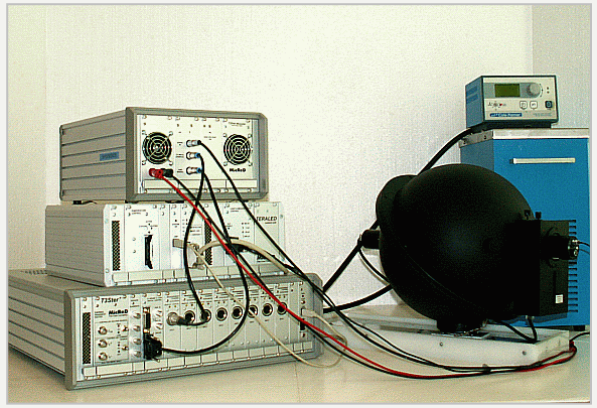
Cold plate as a test environment

Single cold plate setups for R_{thJC} measurements

also, test based models of power packages (transient extended JEDEC 2R models)

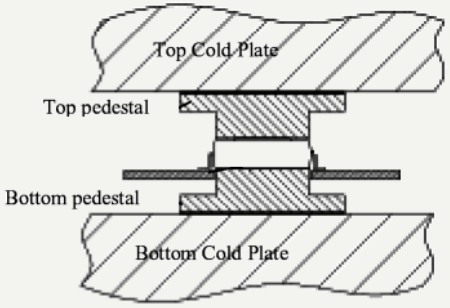
Quicker test, shorter heat-flow path, results characteristic to the package

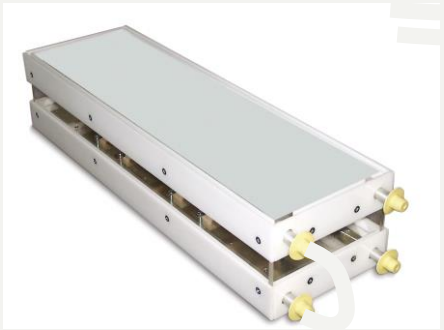




Dual cold plate setups for DELPHI boundary conditions

- validation of detailed models of test set of boundary conditions
- DCP1, DCP2, DCP3, DCP4 setups





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Thermal Measurements

Different ways to get the TSP

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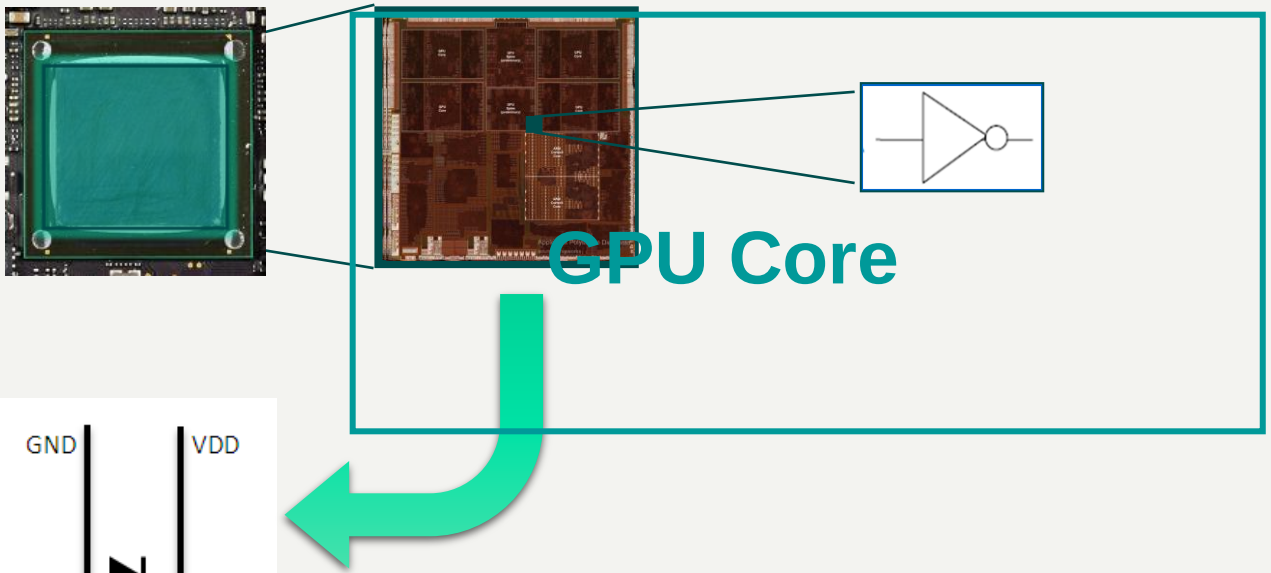
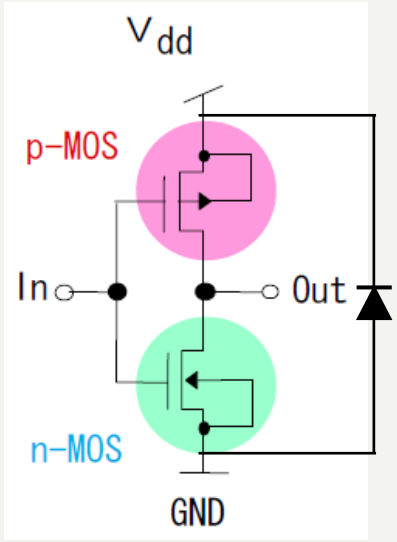
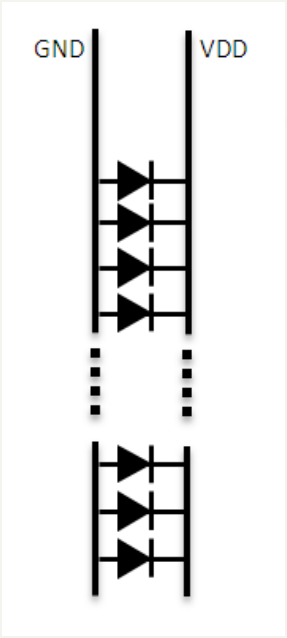
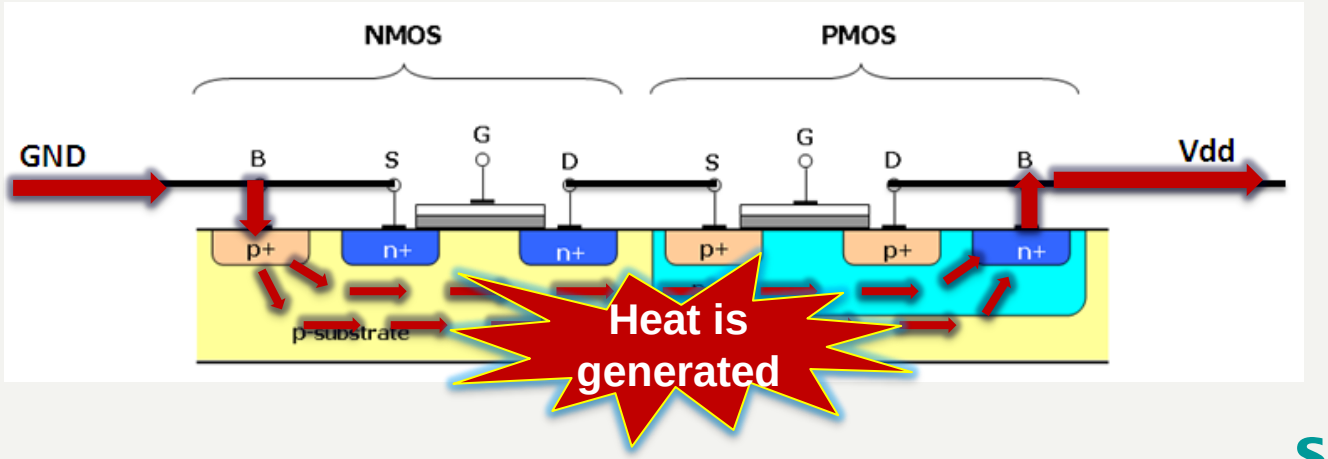
The ‘body diode’ method









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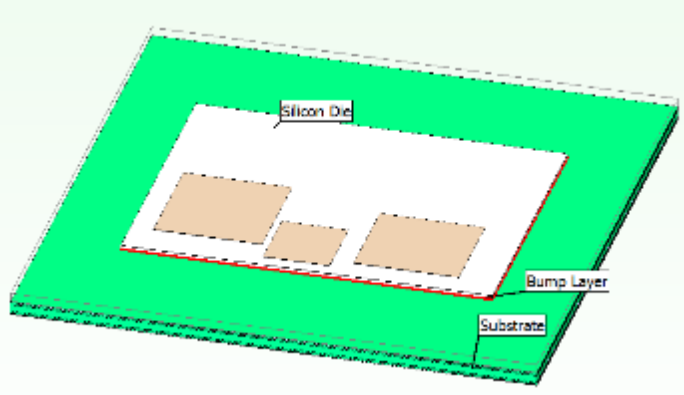
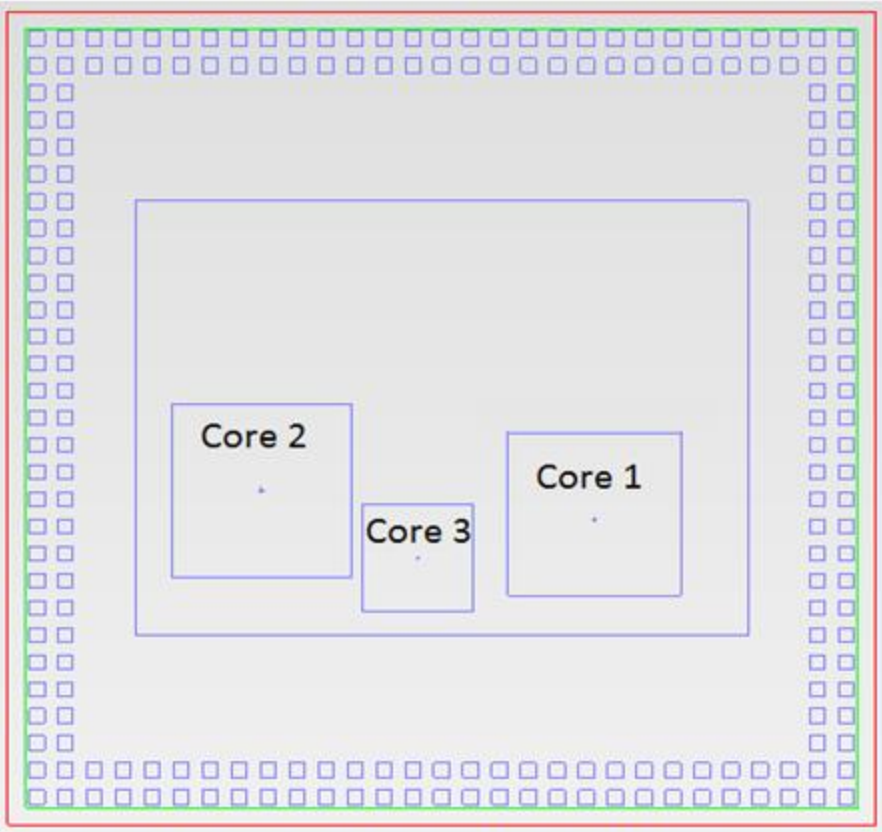
Body diode method example

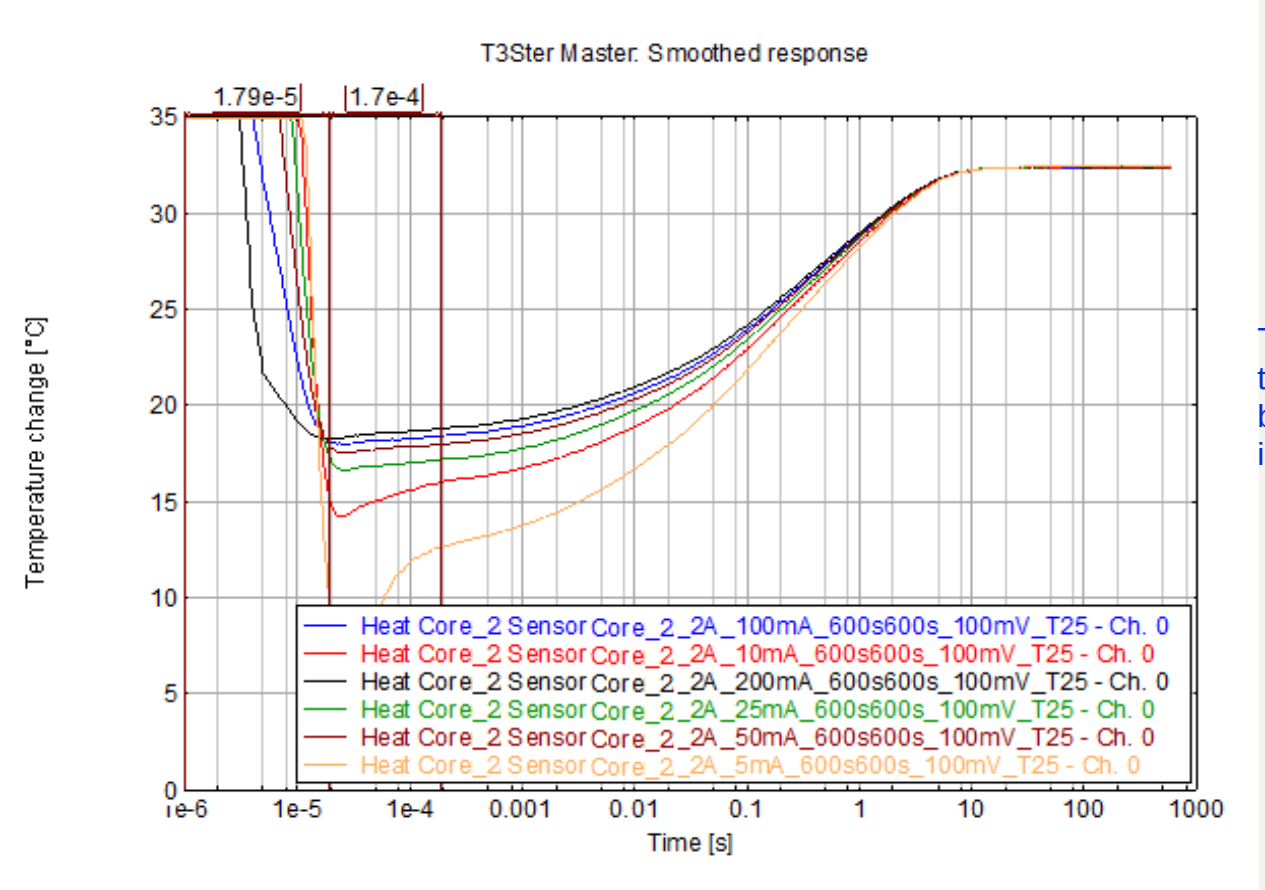
The SoC sample has three cores, ‘Core 1 to 3’ embedded onto one silicon die. Core 2 also contains an embedded capacitance which requires us to select to corresponding sensor current carefully.





Selection of sensor current

Thermal transient measurement were performed on Core 2 with different sensor current values, starting from 5mA and going up to 200mA. The heating current was 2A in each case.



The sensor current is 200mA, the electric transient ends below 20 microseconds, which is a significant gain.

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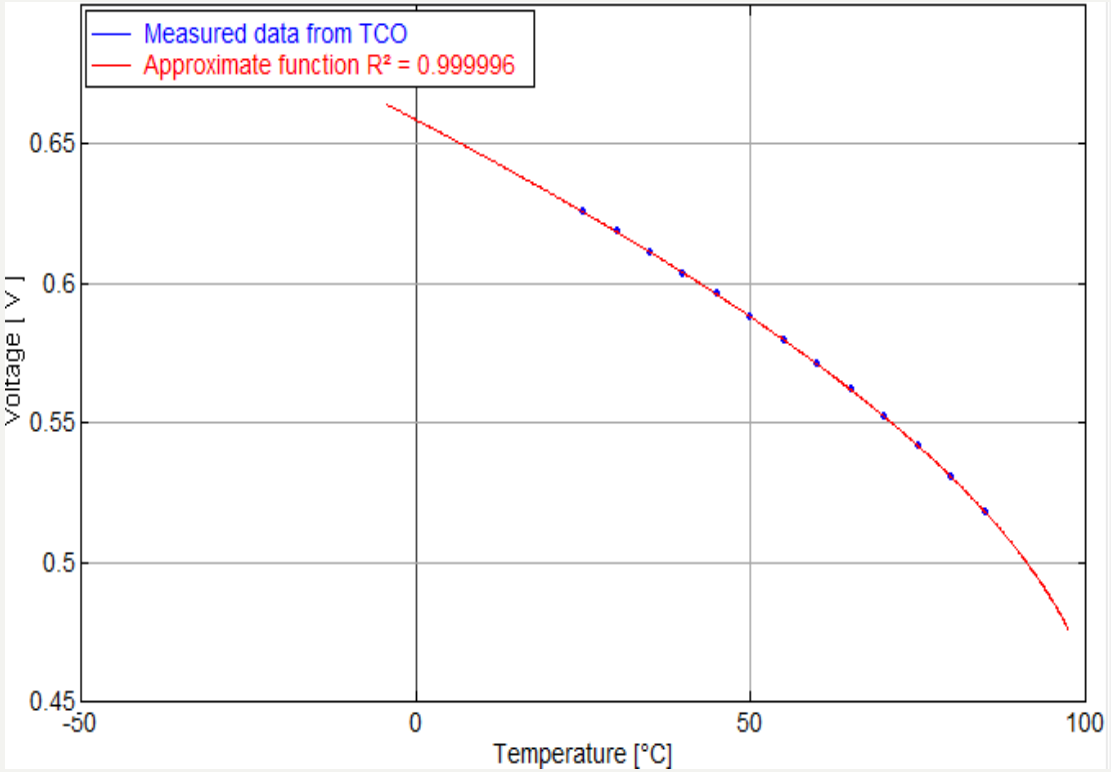
K-factor calibration results

K-factor on Core 2 is non-linear due to the capacitance, however it is highly repeatable.

3rd order polynomial fit was applied on the measured point instead of a linear approximation.



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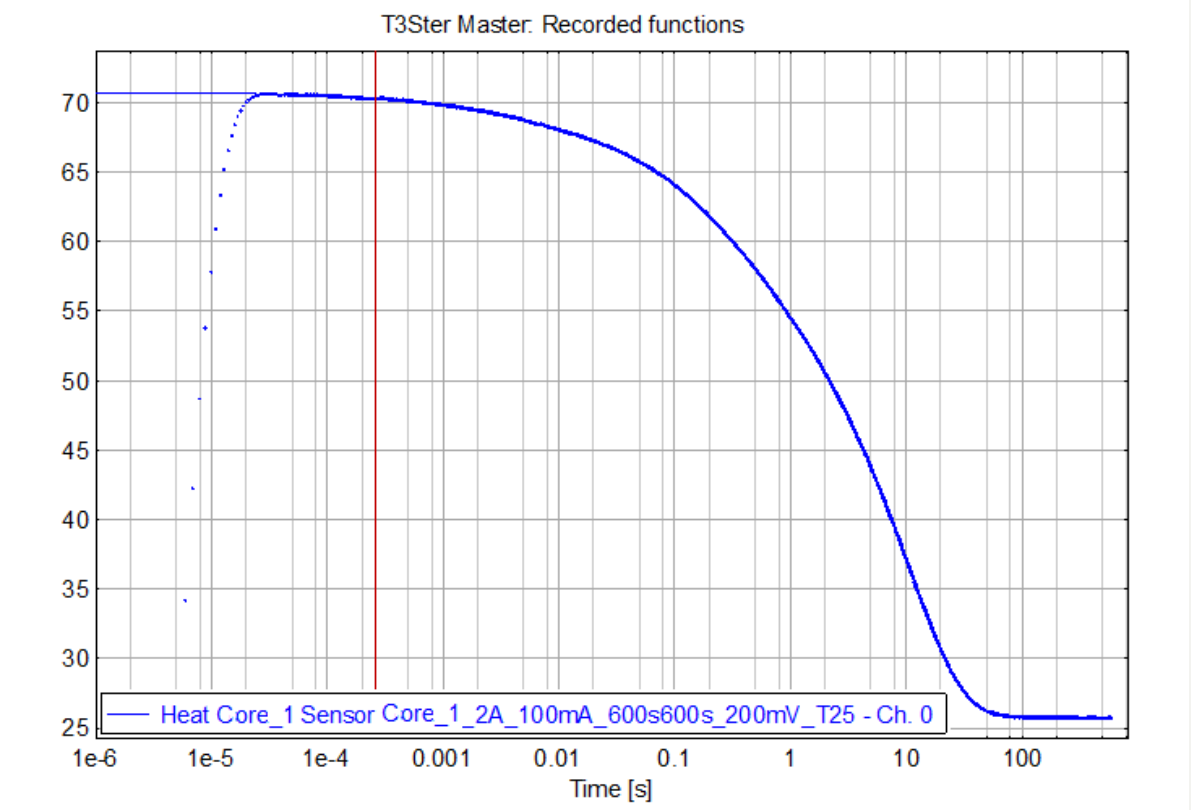
Thermal transient data

After successful calibration of each core, thermal transient tests were performed, two tests on each core.



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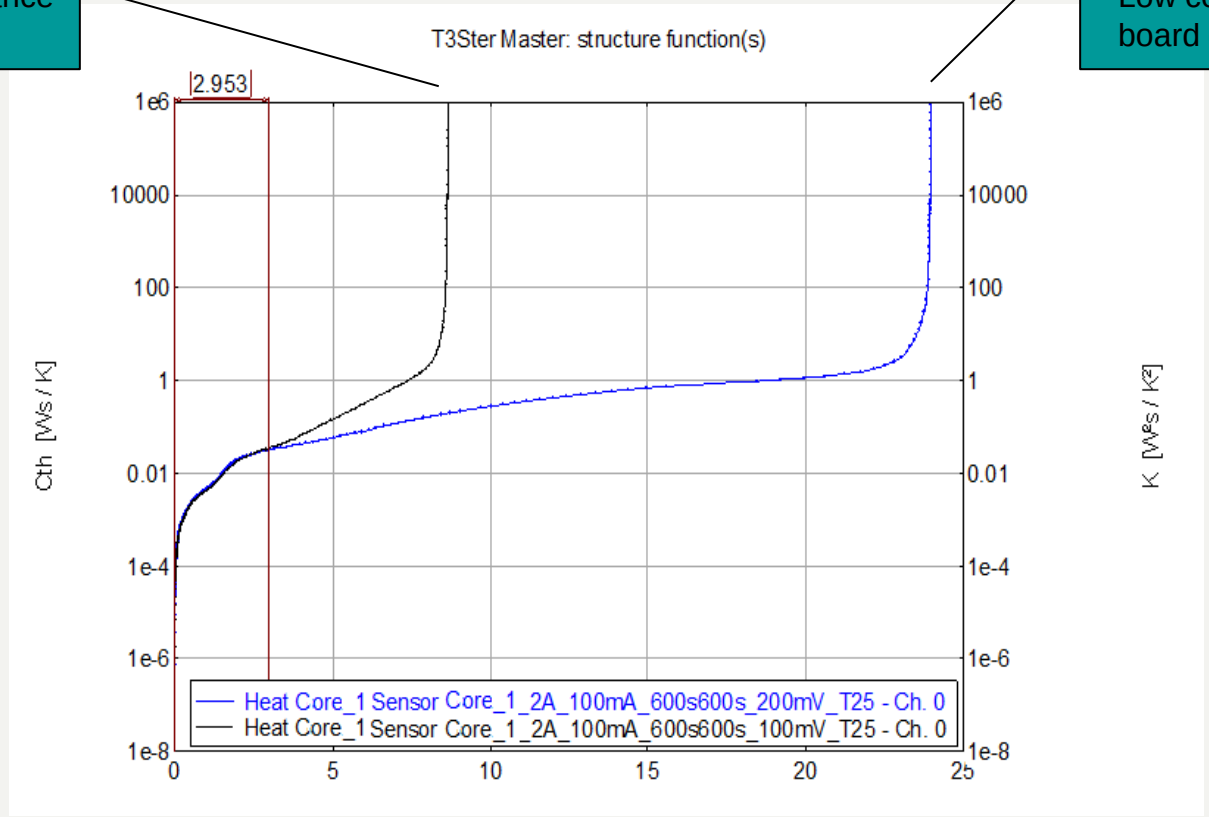
Measurement results

The structure functions corresponding to the device mounted on high conductance board and low conductance board overlap until the R_{thJB} value.

High conductance board data

Low conductance board data



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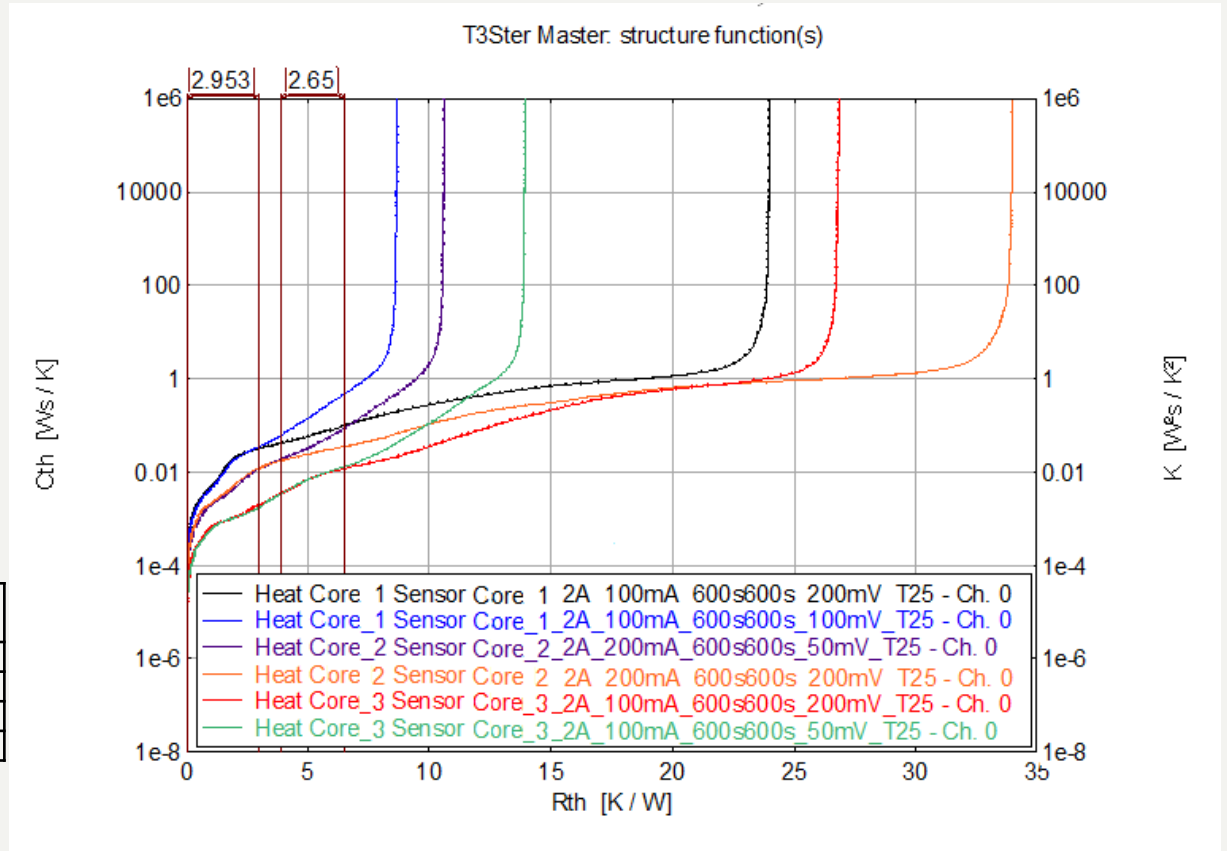
Measurement results

Depending on the heat source area, both the initial thermal capacitance resolved by the structure functions and the calculated Rth_{JB} values will be different.

	Summary of each core's characteristics	
	Area [mm²]	Rth_{JB} [K/W]
Core 1	21	2.95
Core 2	15.5	3.53
Core 3	9.5	6.26



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Alternate option – Use of ESD protection diode

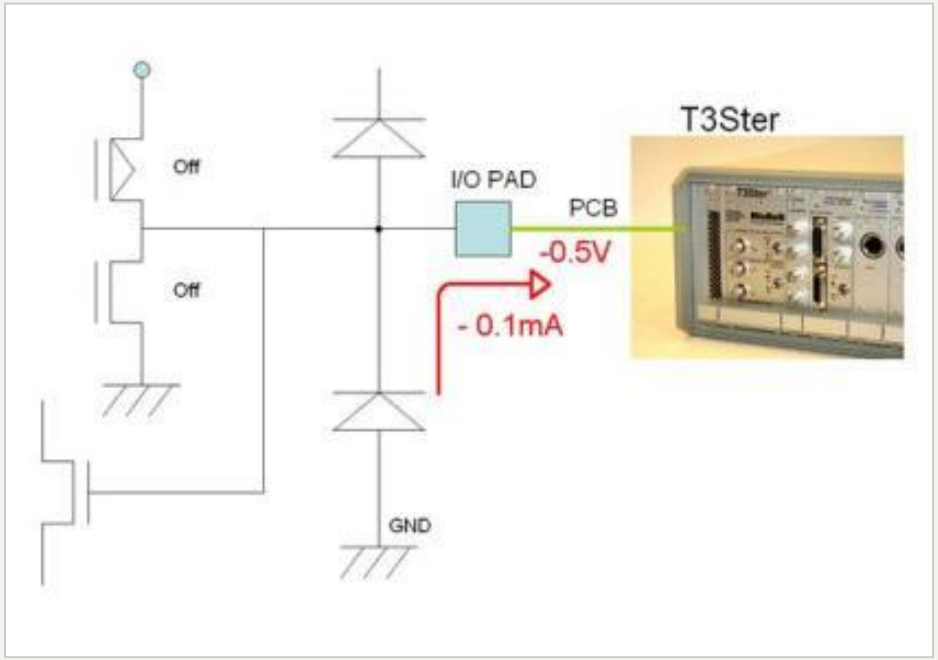
Measuring one of the ESD protection diodes at a non-used I/O pad

Advantages:

- Enables real time measurements while the system is operating

Disadvantages:

- Point like sensor, typically on the I/O ring
- Heated region is different
- Requires additional means to measure power

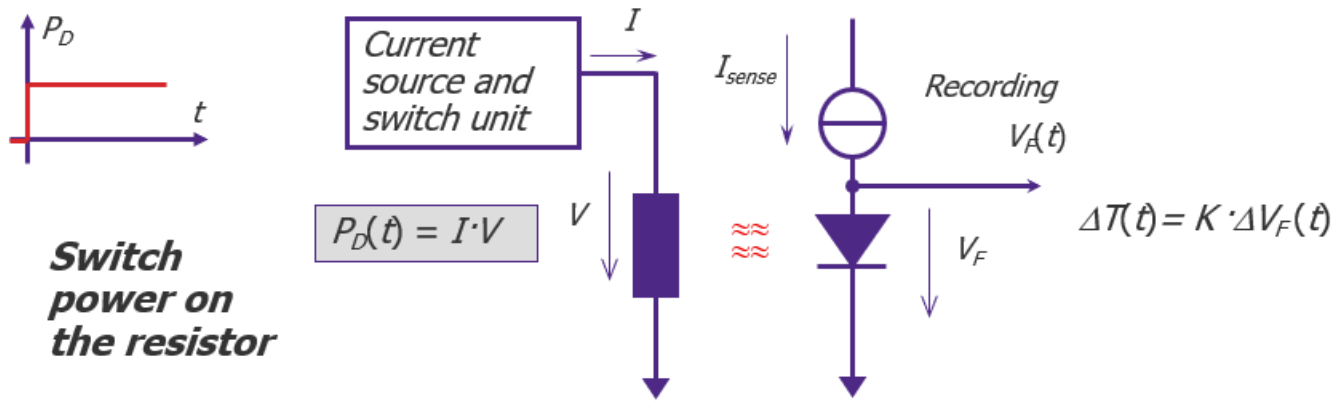


Using TTV-s

Resistive heater – diode like sensor

The distance between the heating resistor and the sensor diode must be small otherwise a transfer impedance is measured.

Constant P_D must be assured – if the resistance depends on temperature, cooling curve must be recorded.



Stacked Test Dies in 144LQFP

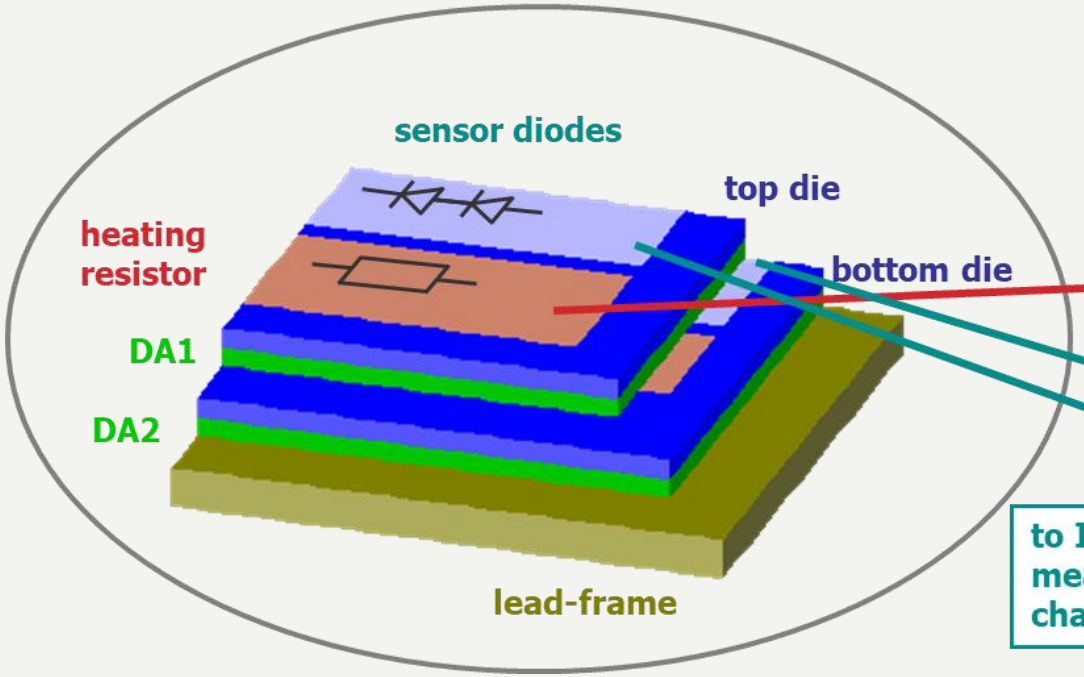
Set measurement parameters

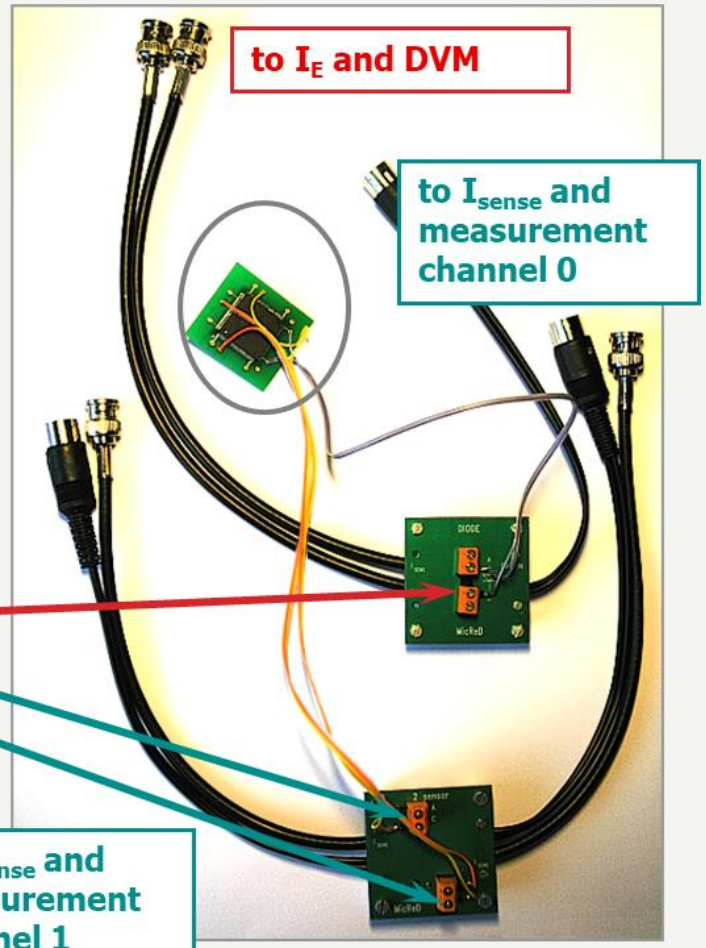
R=19Ω I_E = 150 mA

5 diodes in series S = 10 mV/K, I_{sense}=1mA

Drive (heat) top resistor, **measure** both dies

Evaluate; x-talk transient ends @ 3 µs





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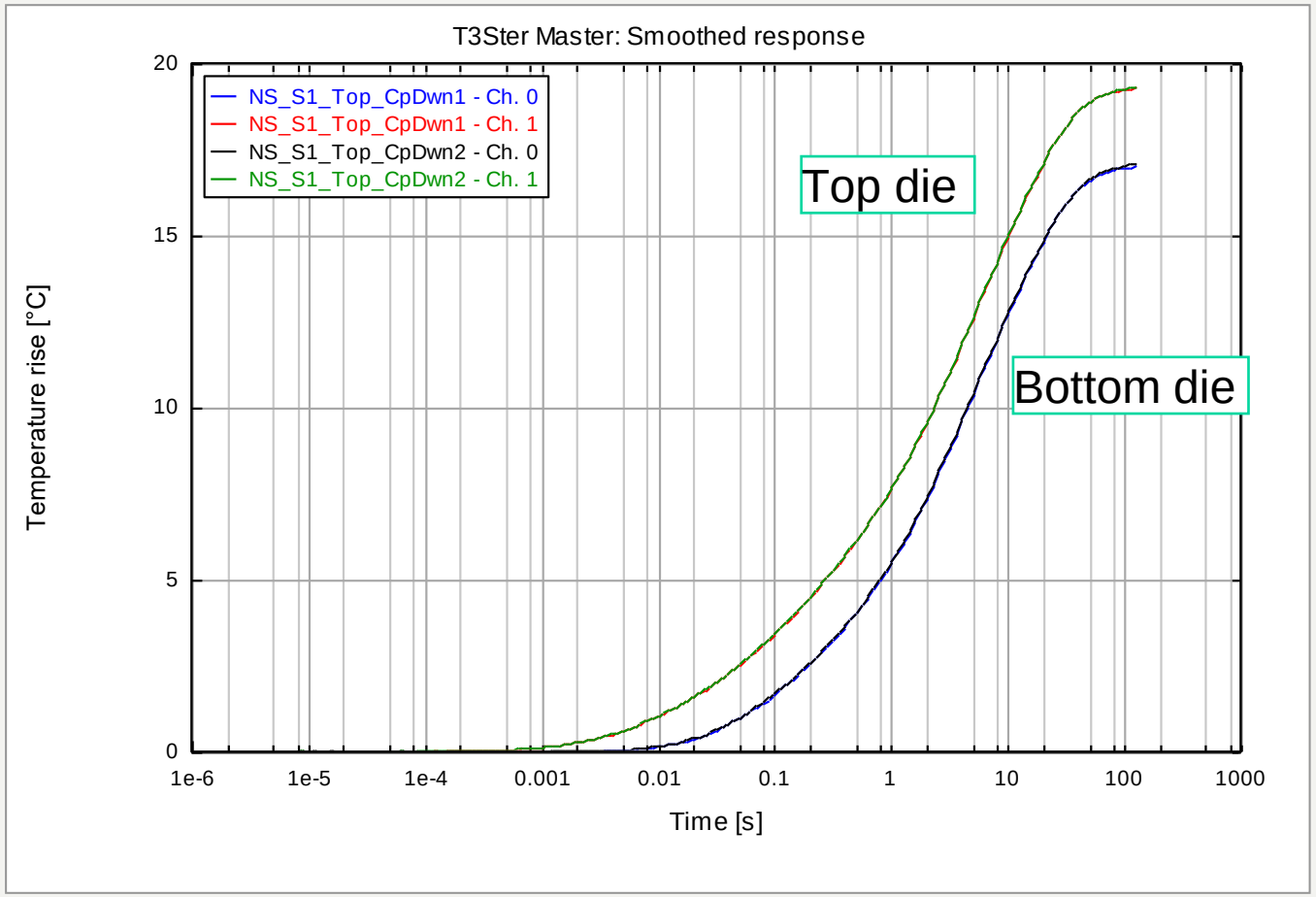
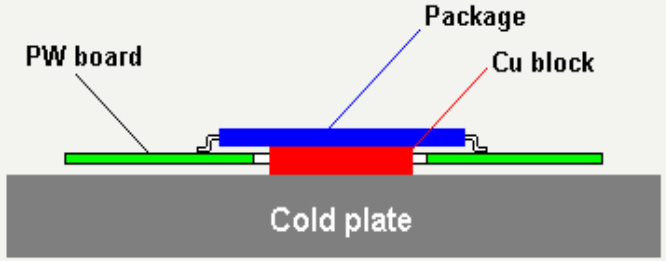
Thermal Transient Test data





Repeated transients, top die powered, temperature at both junctions captured, fitted at cold point

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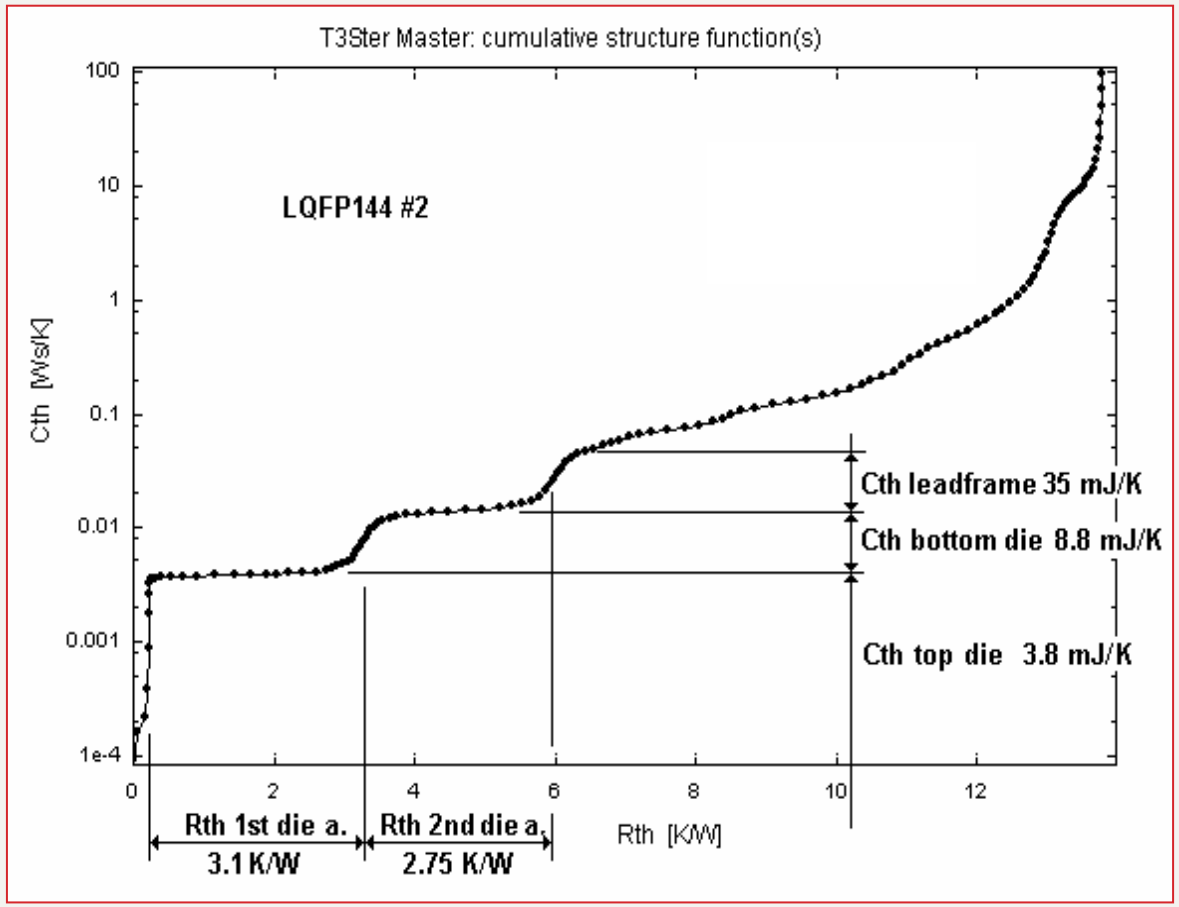
Structure function information



Die attach thermal resistances (measured on cold-plate)

Links to simulation

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Model Calibration

To ensure model accuracy a simulation based Structure Function **must** match the test based Structure Function across all package elements.

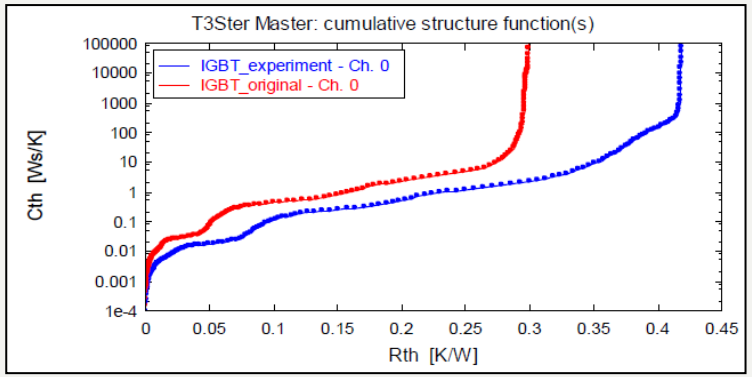
We don’t rely on thermocouple measurements

Only then are we ensured that each object in the package is modelled correctly.

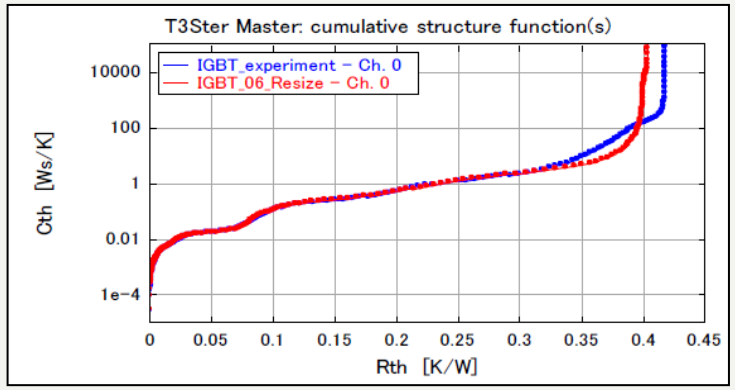
Only then are we ensured that the 3D temperature field is accurate

Only then are we ensured the simulaton model includes all package time constants and will respond correctly for all driving power profiles.

—Uncalibrated



—Calibrated



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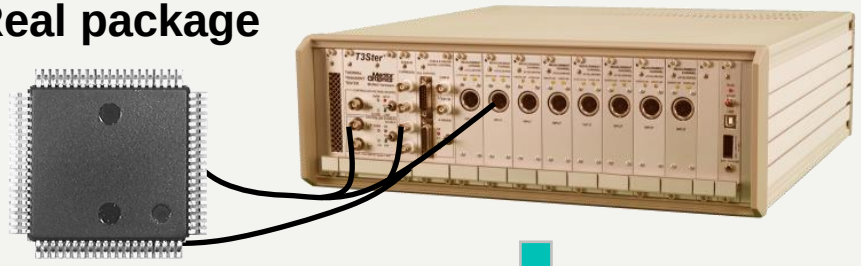
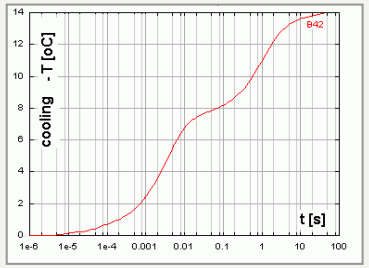
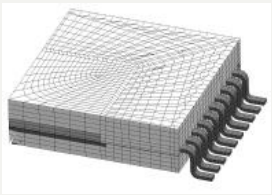
Calibrating simulation models to test data

Real package



Thermal transient measured by ***T3Ster***



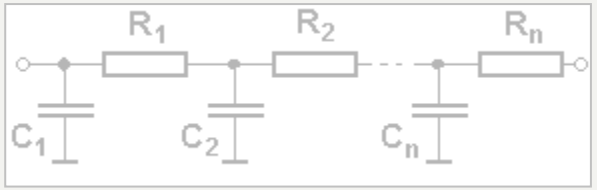


Detailed package model

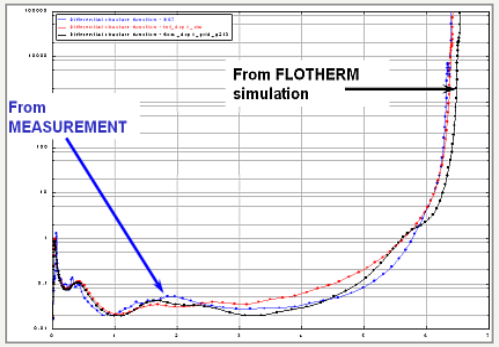
CFD/FEA

Structure Function

Structure functions for test based compact model generation



Structure functions for validation of detailed models



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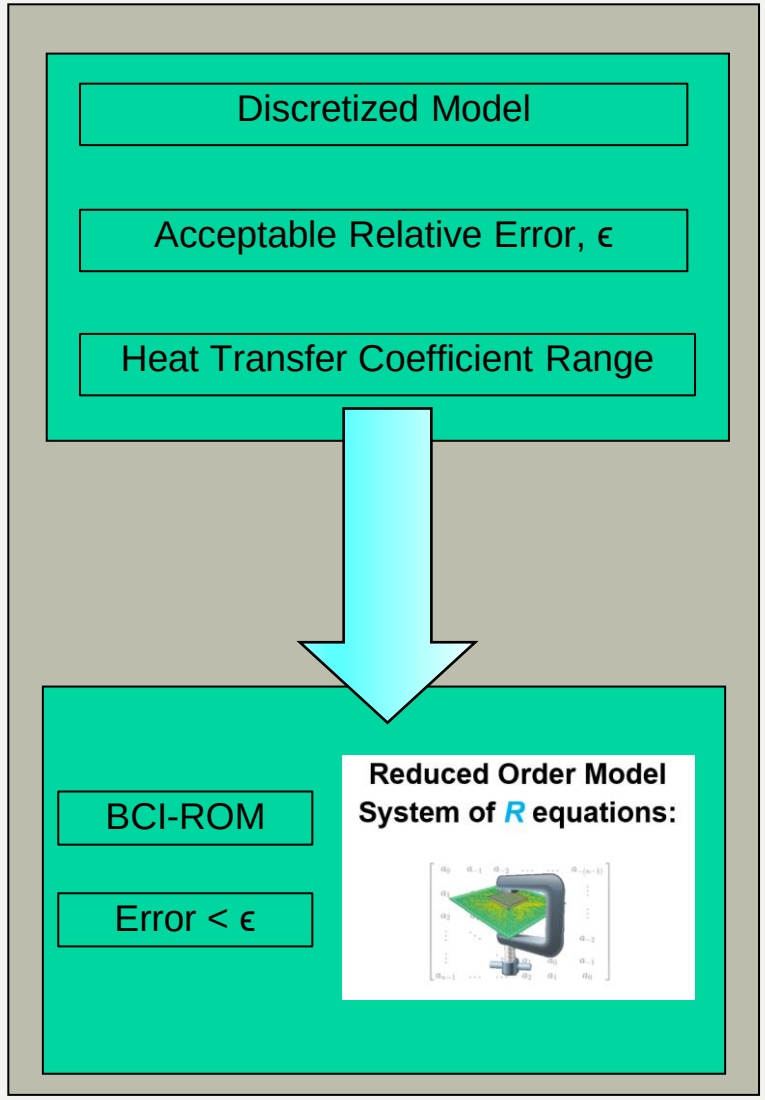
FANTASTIC Method for Reduced Order Models

L. Codecasa, V. d'Alessandro, A. Magnani, N. Rinaldi and P. J. Zampardi, "Fast Novel Thermal Analysis Simulation Tool for Integrated Circuits (FANTASTIC)," *20th International Workshop on Thermal Investigations of ICs and Systems*, London, 2014

Ideal Compact Thermal Model:

- Boundary Condition Independent ✓
- High Accuracy – Known Accuracy ✓
- Supports Multiple Heat Sources ✓
- Transient Support ✓
- Internal Geometry cannot be reverse engineered ✓
- Solves orders of magnitude faster than detailed model ✓
- Can be created quickly and reliably ✓



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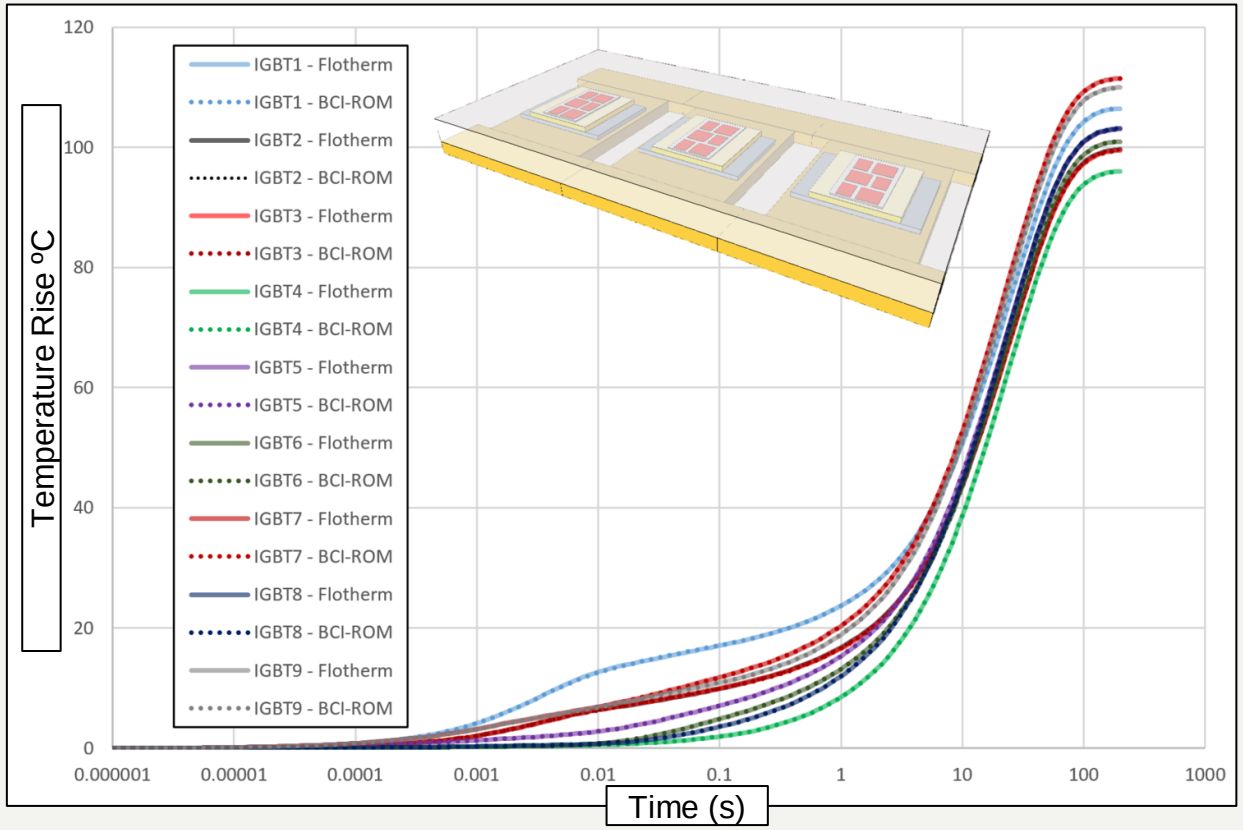
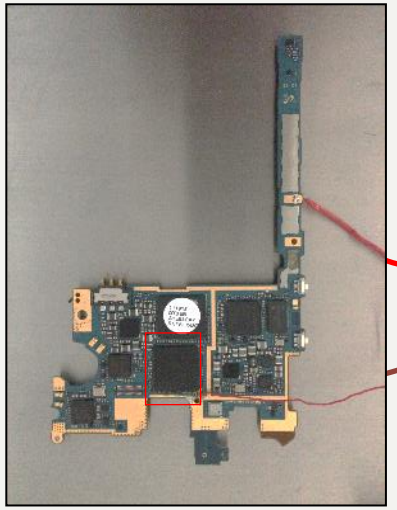
FANTASTIC Accuracy

- A ‘FANTASTIC’ Reduced Order Model is accurate for:
  - Any set of Boundary Conditions
  - Any number of heat sources
  - Any driving frequencies, and at all transient time scales.

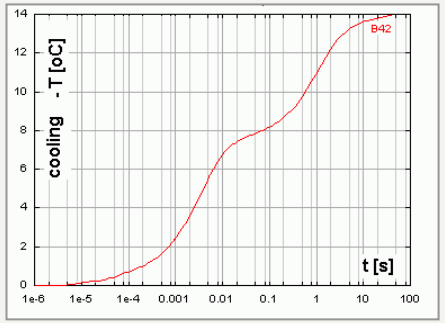
- Unlike any other ROM method, the accuracy is an input!



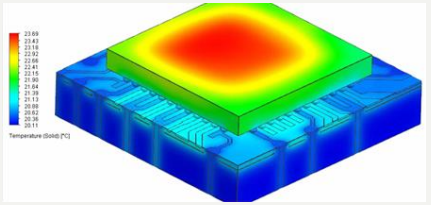
Calibration and BCI ROM workflow

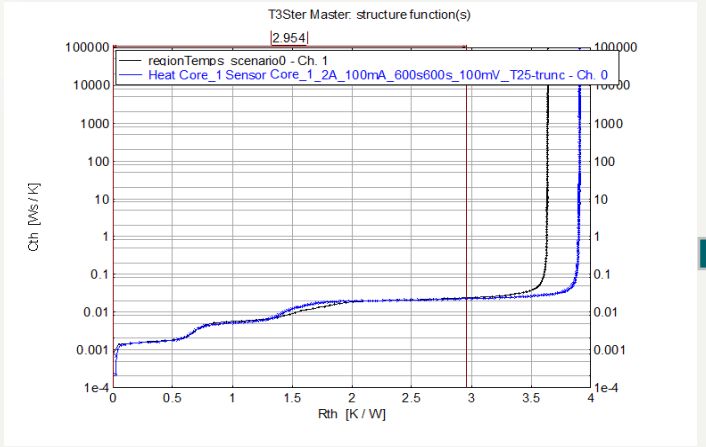


Real package

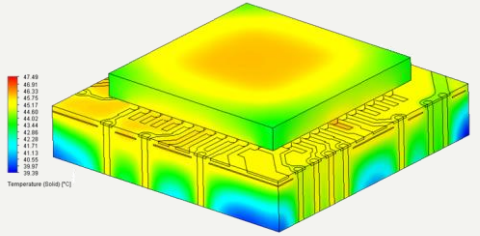


Package model from Vendor

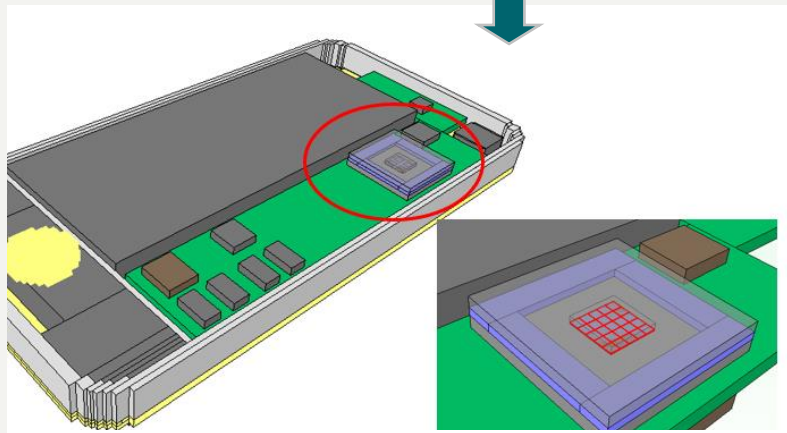




Match structure functions during calibration



Calibrated model



System level model with die power map

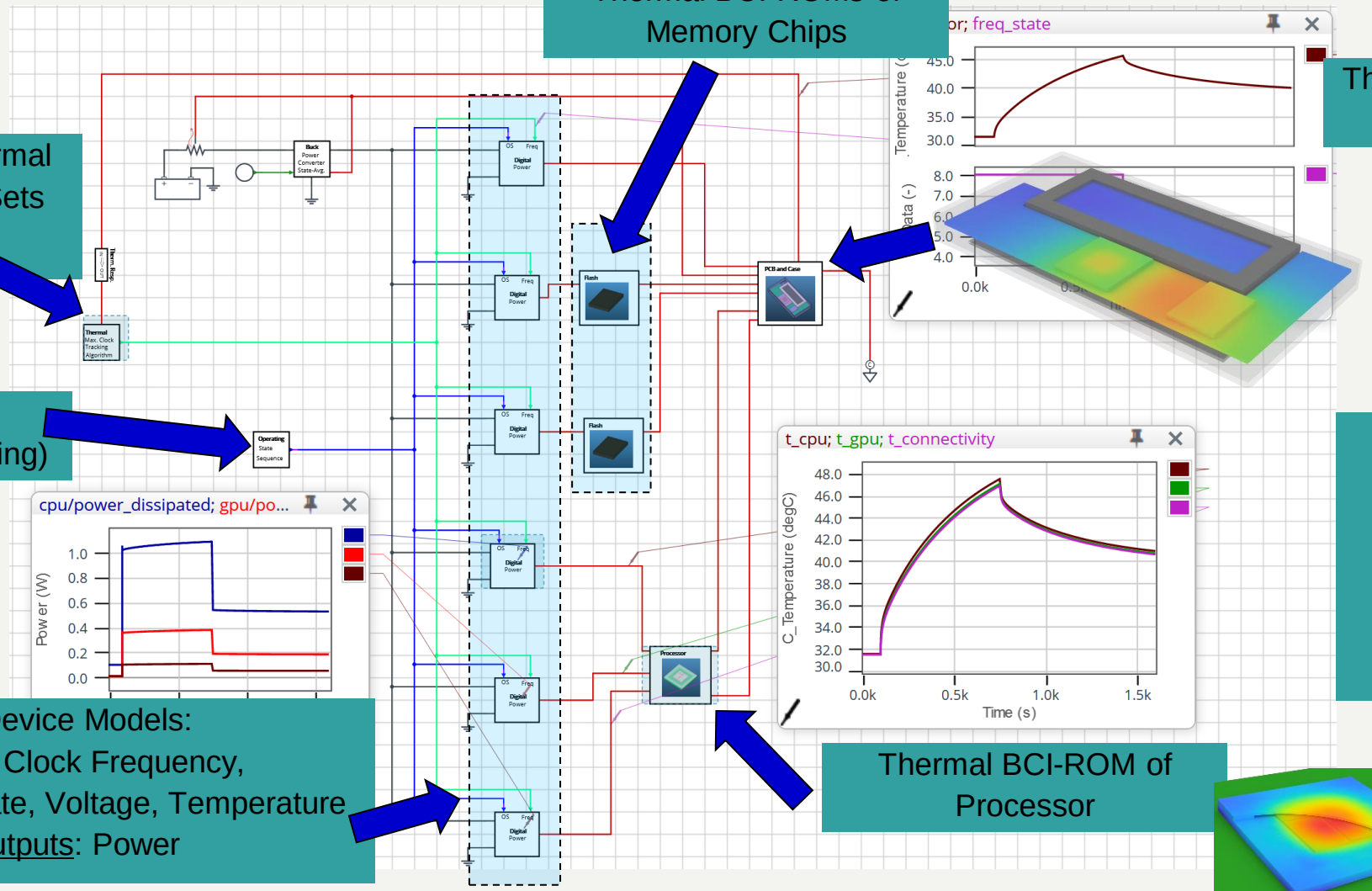
Using BCI-ROMs
Mobile Phone Example

Thermal BCI-ROMs of Memory Chips

Custom Dynamic Thermal Management Policy Sets Clock Frequency

Thermal BCI-ROM of PCB and Phone Casing

Operating State (Idle, Streaming, Gaming)

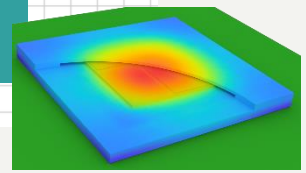


Typical Results

Device Temperatures
Powers
Clock Frequency

6 Device Models:
Inputs: Clock Frequency, Operating State, Voltage, Temperature
Outputs: Power

Thermal BCI-ROM of Processor



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Summary

- Accurate thermal measurement of complex semiconductor packages is possible
- There are multiple choices to select TSP, powering, test environment
- The test data can be transformed to behavioral or structural thermal models
- The test data can be used to supply calibration input to cutting-edge simulations

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Thank you! Questions?

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