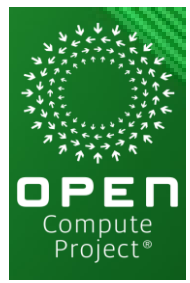
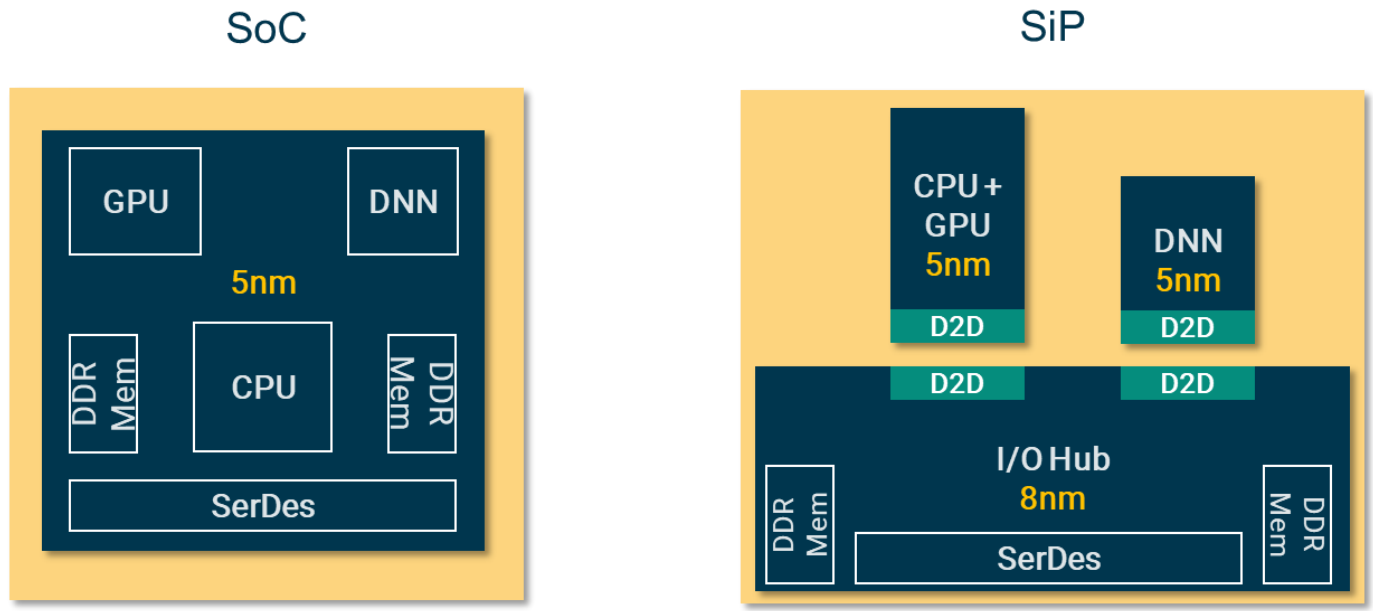
BoW-Based Die-to-Die Interface Solutions

Elad Alon
Co-Founder, CEO

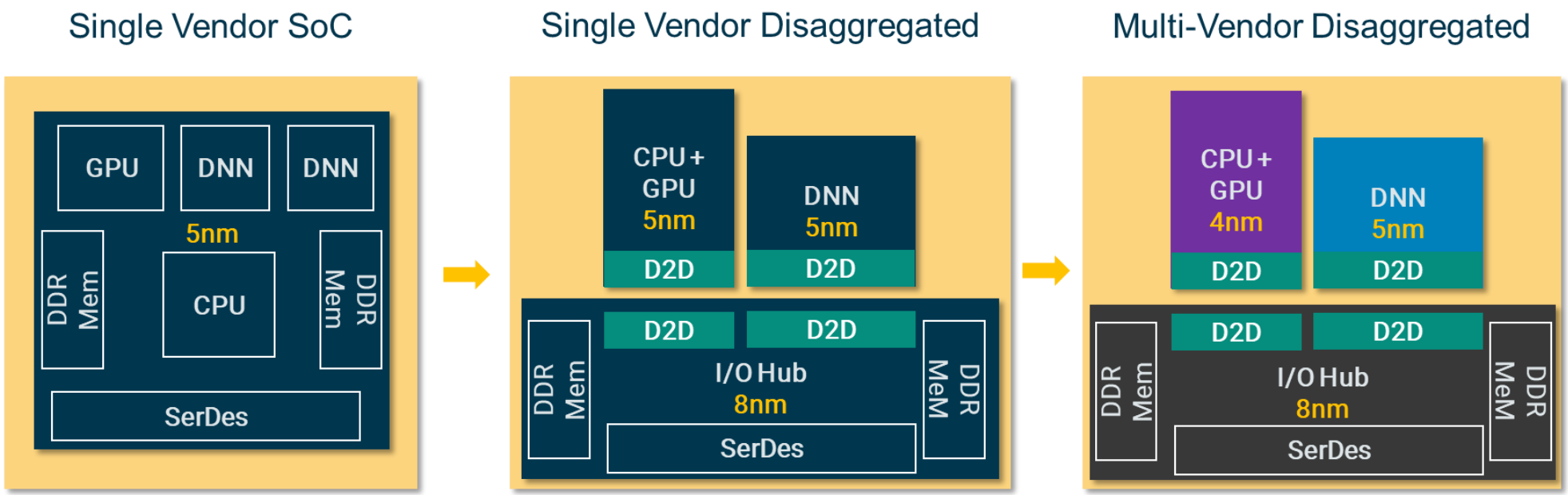


Chiplets and Chiplet Interfaces



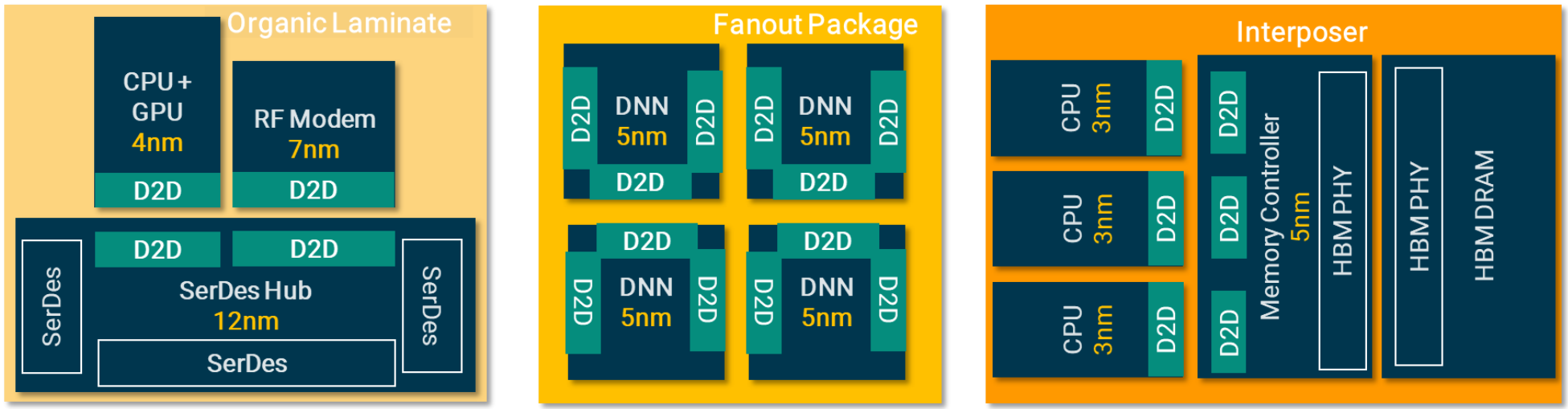
- Chiplets enable improved yields and matching / optimization of process technology to function
- Monolithic wires (~100-200nm pitch) replaced by cross-package die-to-die interconnects (~10's to 100 um pitch)
- These "new" interfaces must be heavily optimized to unlock the promise of chiplets

Key Criteria for D2D Interfaces



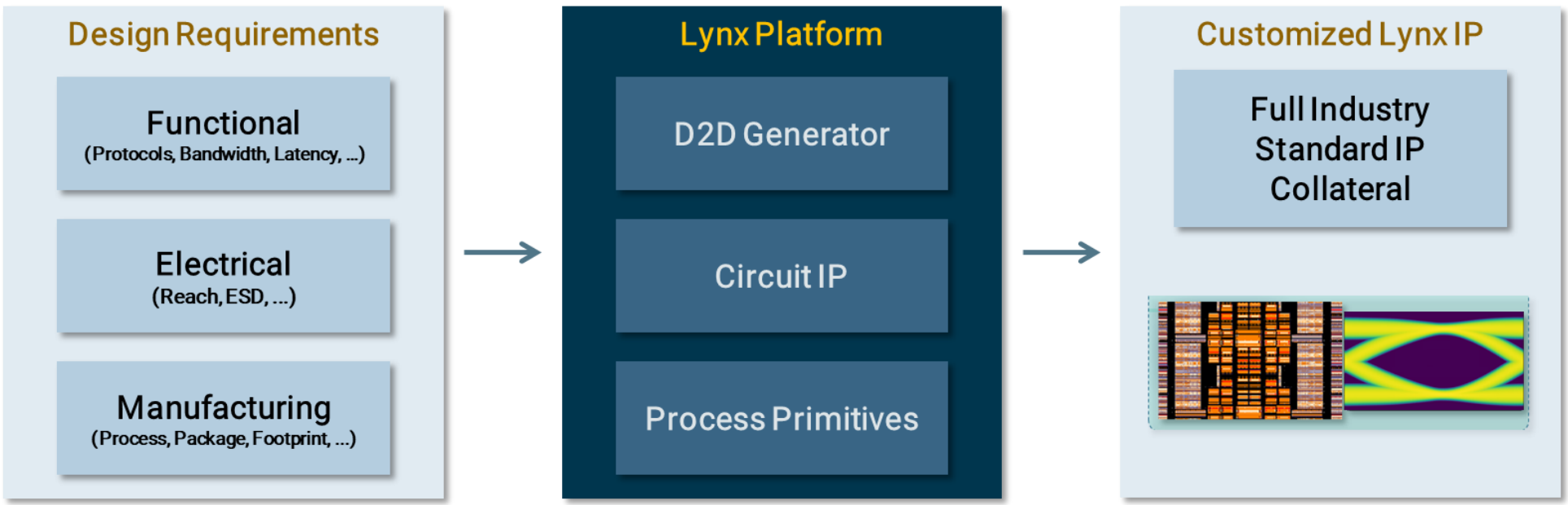
- D2D PPA and portability are key for single vendor disaggregated market
- Interoperability (open standards) pave the way towards multi-vendor chiplet market

One Size Does Not Fit All

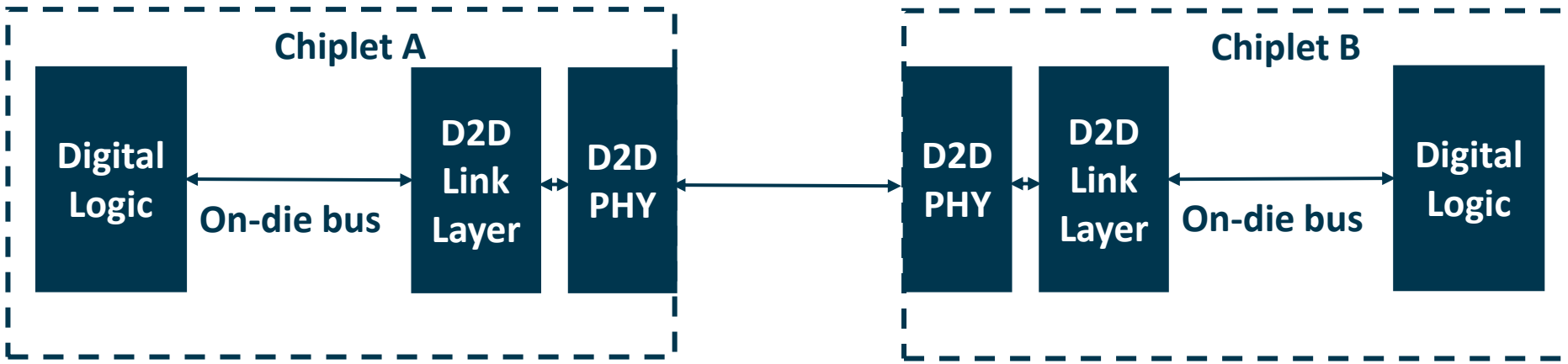


- Requirements and key features of the interfaces are heavily influenced by the end product
  - Significant variations in importance of cost vs. performance vs. power vs …

BCA's Approach: Lynx Platform



Lynx Interfaces



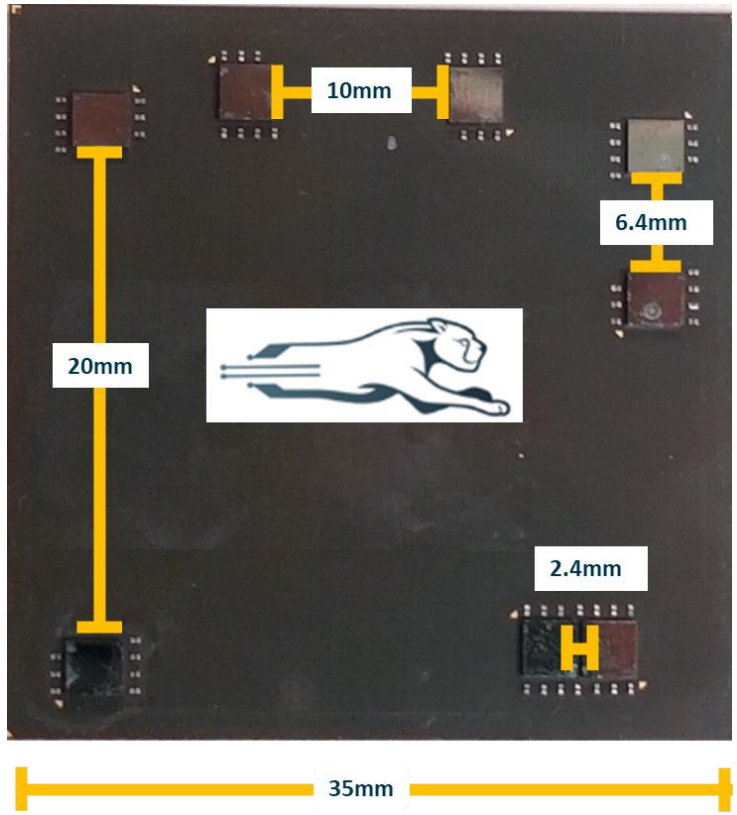
- Focus on in-package parallel links to reduce latency and power relative to e.g. XSR SerDes
  - Lynx supports parallel links with 2-16Gb/s/line, 45-130μm bump pitch

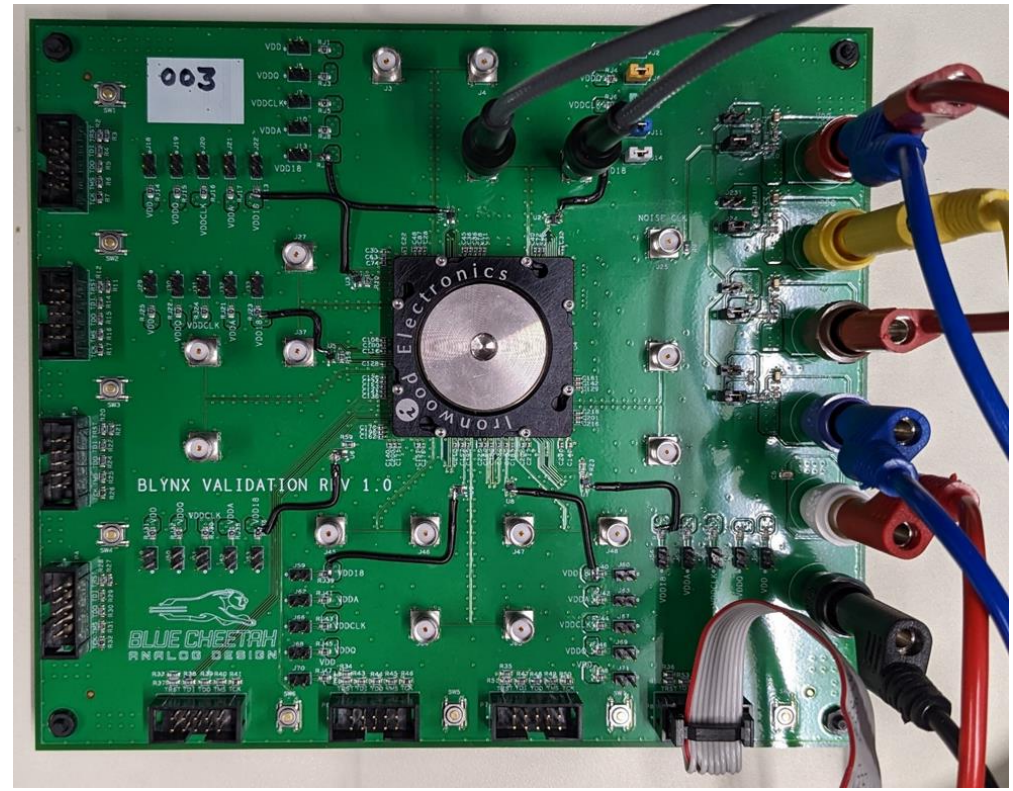
- Lynx (optionally) supports packetized link layers for a wide variety of industry-standard on-die buses

Lynx PPA

- Proprietary low-drift and low-latency clock and data path circuits designed to robustly achieve excellent PPA under harsh integration environments
  - **<2ns** PHY-to-PHY latency
  - **<10ns** bus-to-bus latency (including all CDCs, PHY, and FEC)
  - **<0.15mm²** per 16-bit data slice
  - **<0.5 pJ/bit** at >**20mm** reach on 8-2-8 laminate and **<1e-20** raw error rate

TSMC 12nm BoW PHY Silicon





- First-pass silicon achieves full 16 Gb/s (256Gb/s/slice)!
  - Look out for full announcement soon

About BCA

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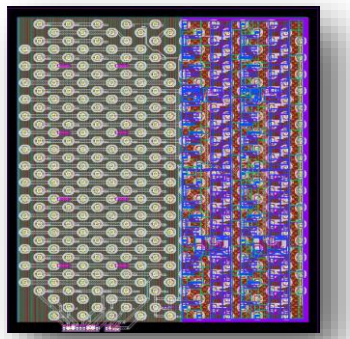

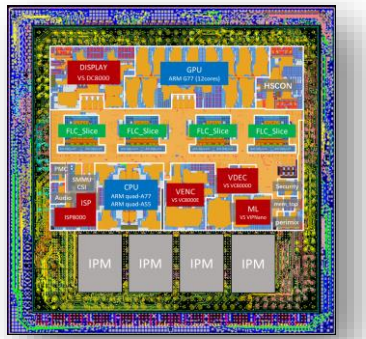

Eric Naviasky
Senior Architect
Co-founder Cadence A/MS IP

Tom Kelly
COO
Co-founder Cadence A/MS IP

- Founded in 2019, led by experienced and globally recognized team of experts
- Multiple first-pass silicon successes in parallel interfaces
- Multiple D2D design wins with Tier 1 customers as well as industry-leading startups