CHIPLET SUMMIT
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ChipletSummit.com

Improving Electromagnetic Simulation for Chiplet-based 2.5D/3DIC Designs

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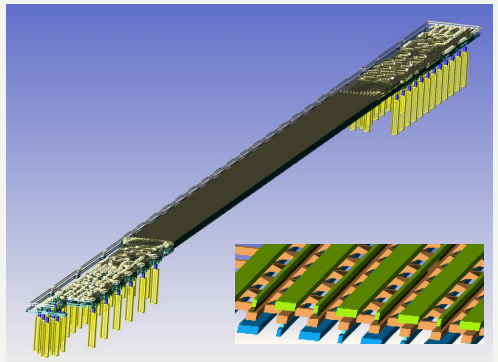
ACCELERATE YOUR IC DESIGN

CONTENT

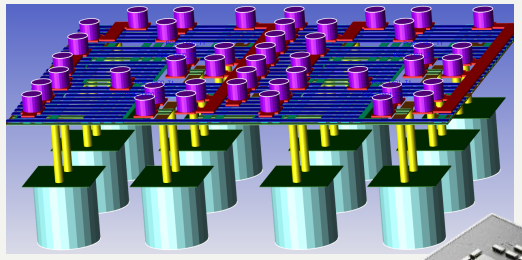
1. SI/PI analysis need for chiplet
2. EM simulation challenges for chiplet
3. Today’s EM simulation landscape
4. Xpeedic’s EM solver solution for Chiplet
5. Benchmark examples
6. Summary

SI/PI Analysis for Chiplet-based 2.5D/3DIC Designs

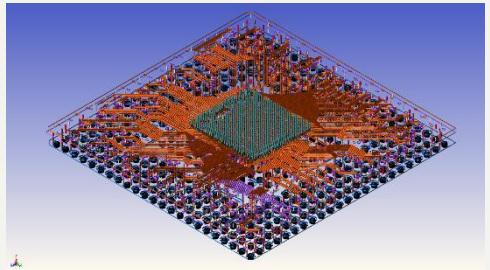
D2D Interconnect Modeling



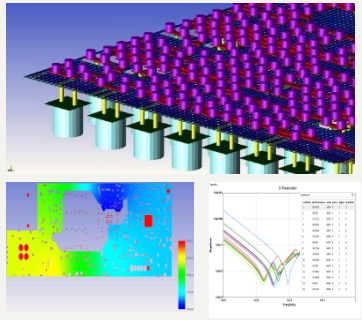
TSV Modeling

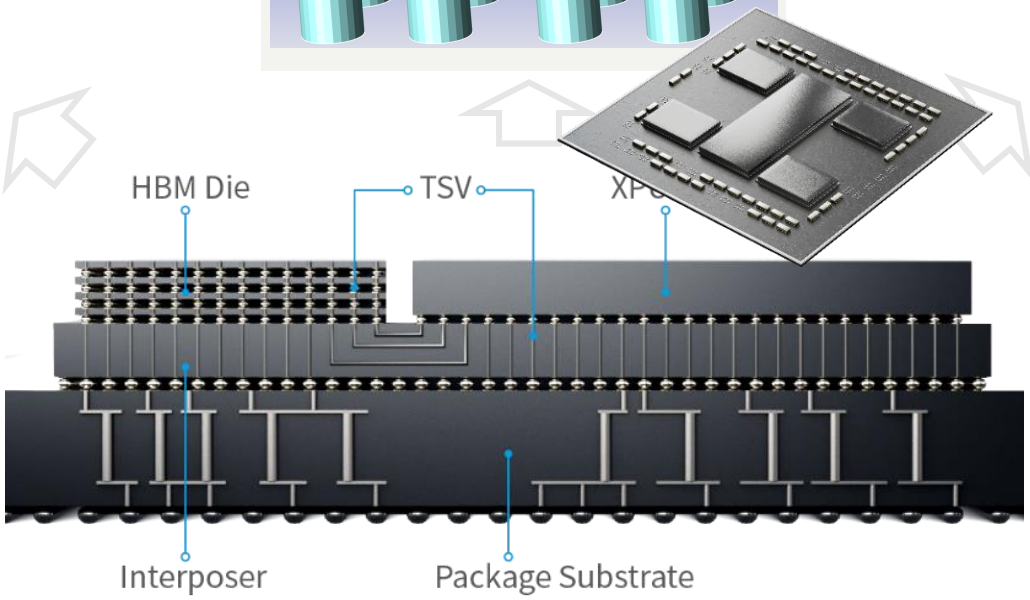


Die-Interposer-Substrate Co-sim

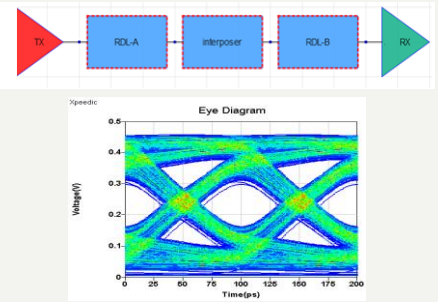


PI Analysis





Channel Analysis

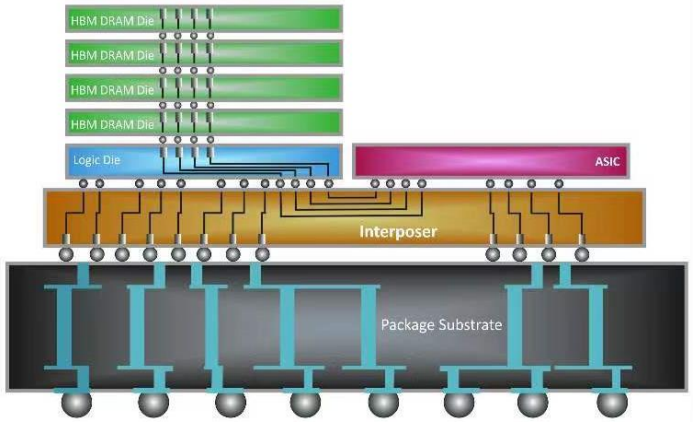


EM Simulation Challenges for Chiplet SI/PI Analysis

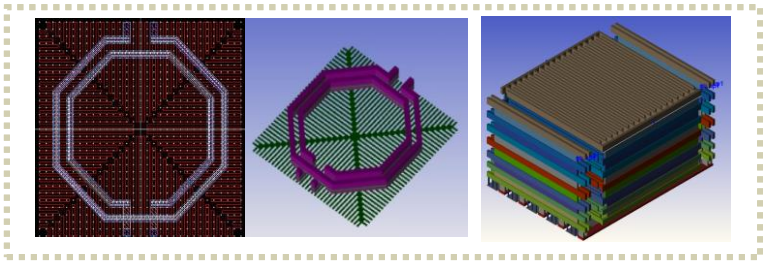
- 3D in nature
  - Densely packed interconnect + bump-via-trace transitions + TSV
  - 3D EM solver is needed
- Large scale
  - Number of D2D interconnects
  - Dense interconnects with small L/S and various ground structures -> crosstalk should be accurately characterized -> many nets should be simulated together
  - Large-capacity EM solver is needed
- High data rate
  - Full-wave EM solver is needed
- Multi scale
  - Multi-scale EM solver is needed for co-simulation of die, interposer, and substrate due to the dramatic L/S difference

Today's EM Simulation Landscape

- Different solvers are preferred at IC level and package/board level
- Disjointed flow from IC, interposer, package, to board
- Difficult to simulate die-on-interposer or interposer-on-package due to the problem size and the multiscale nature of the problem

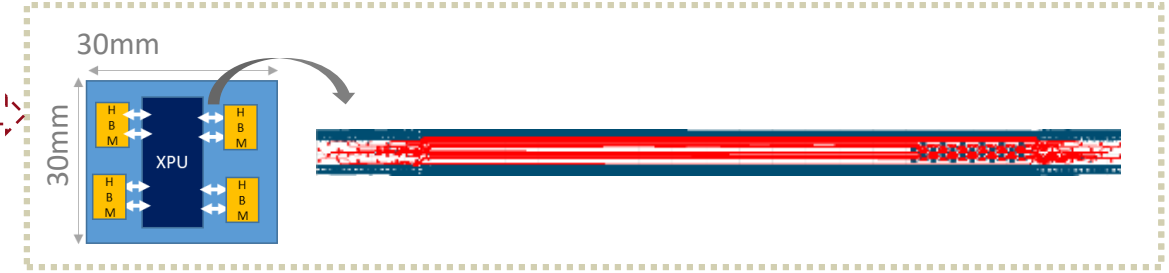


IC

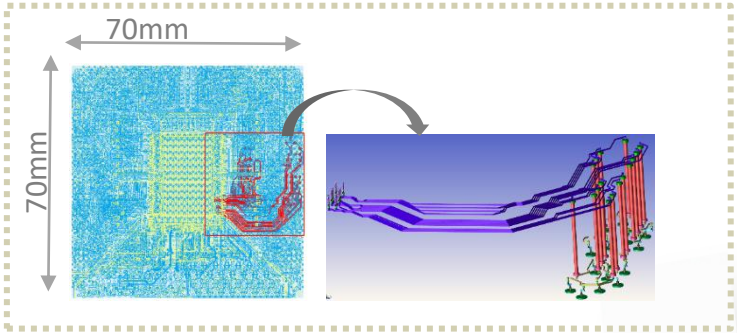


MoM-based solver

Interposer



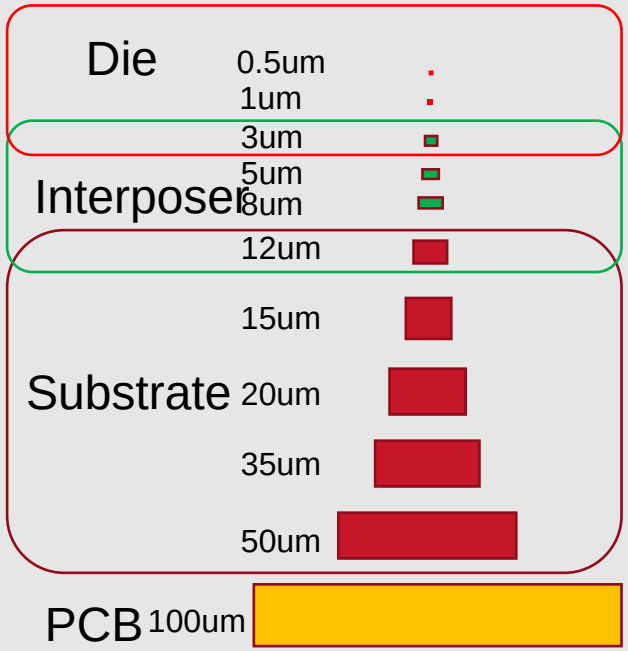
Package/Board



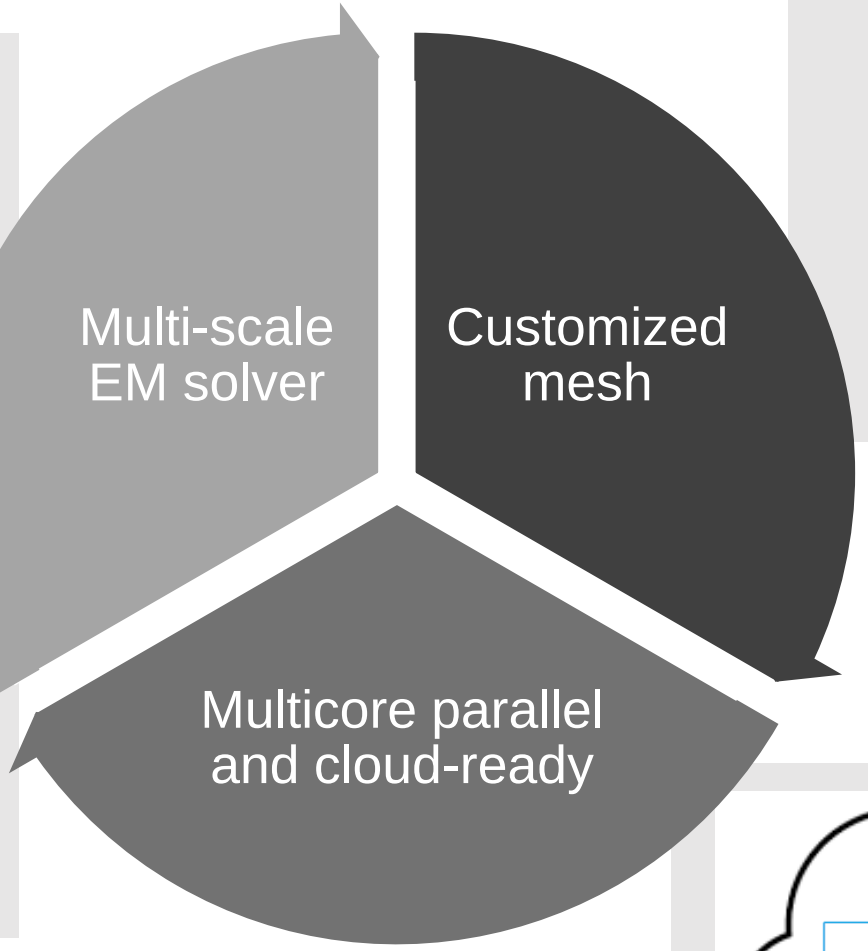
FEM-based solver

Xpeedic's Dedicated Solver/Mesh for Chiplet

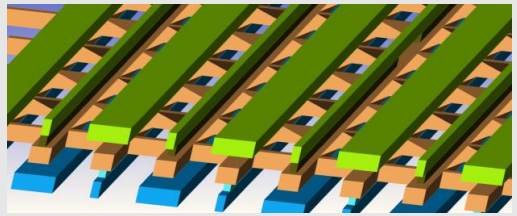
Multi-scale solver to capture 100x-scale difference



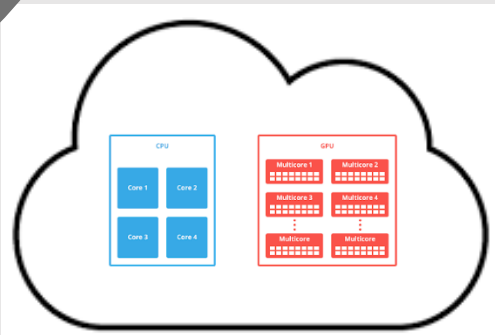
Interconnect width/spacing



Interconnect-friendly mesh

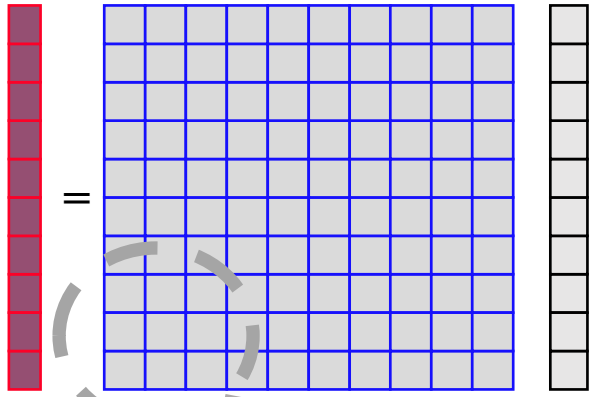


Refined mesh to capture trace skin effect and trace-to-trace and trace-to-ground proximity effect

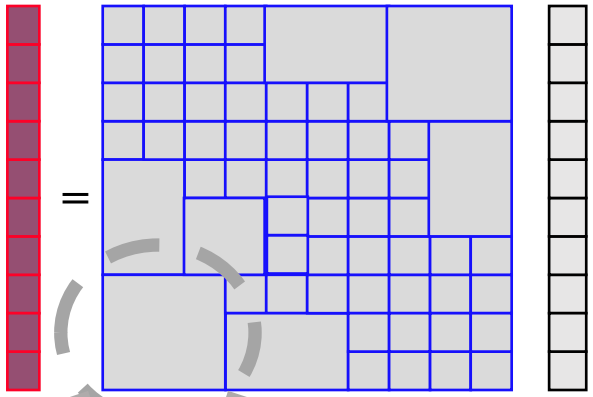


Fast Large-scale Solver

MoM: Matrix Equation



Fast MoM: Matrix Equation



MoM Compression Techniques

- SVD
- ACA
- FFT
- FMM
- ***And many more …***

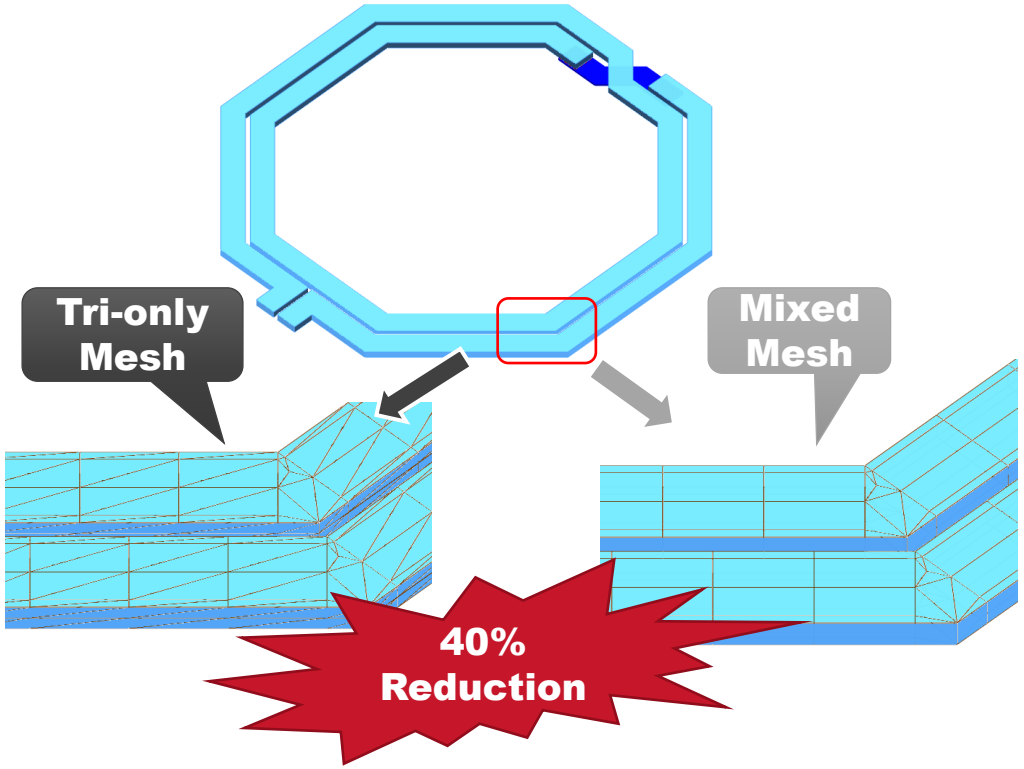
Matrix Solve

- Iterative Approach
- LU Factorization

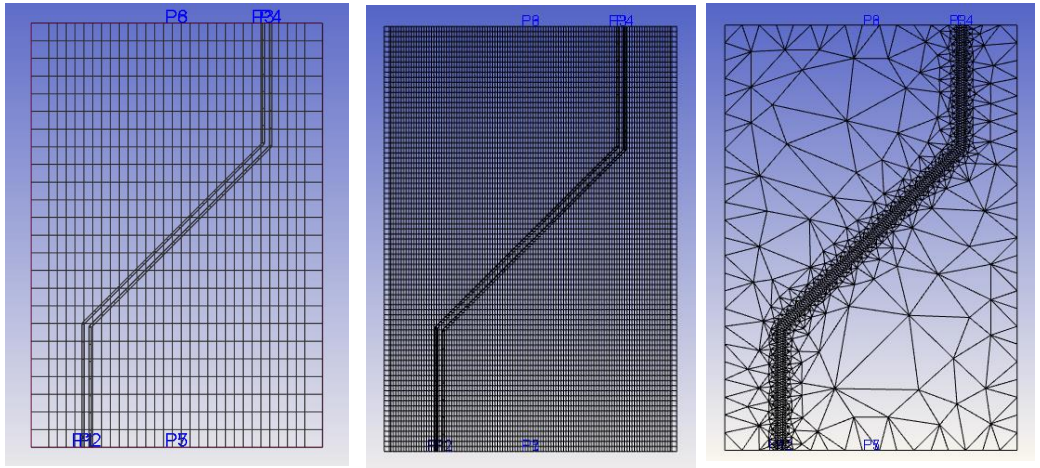
Key idea: Distant interactions can be “compressed”
=> Reduce matrix size from **O(N²)** size to approx. **O(N)** size

Intelligent Mesh Technology

- Optimal rectangle-triangle mixed mesh
- Result in mesh element reduction and mesh regularization



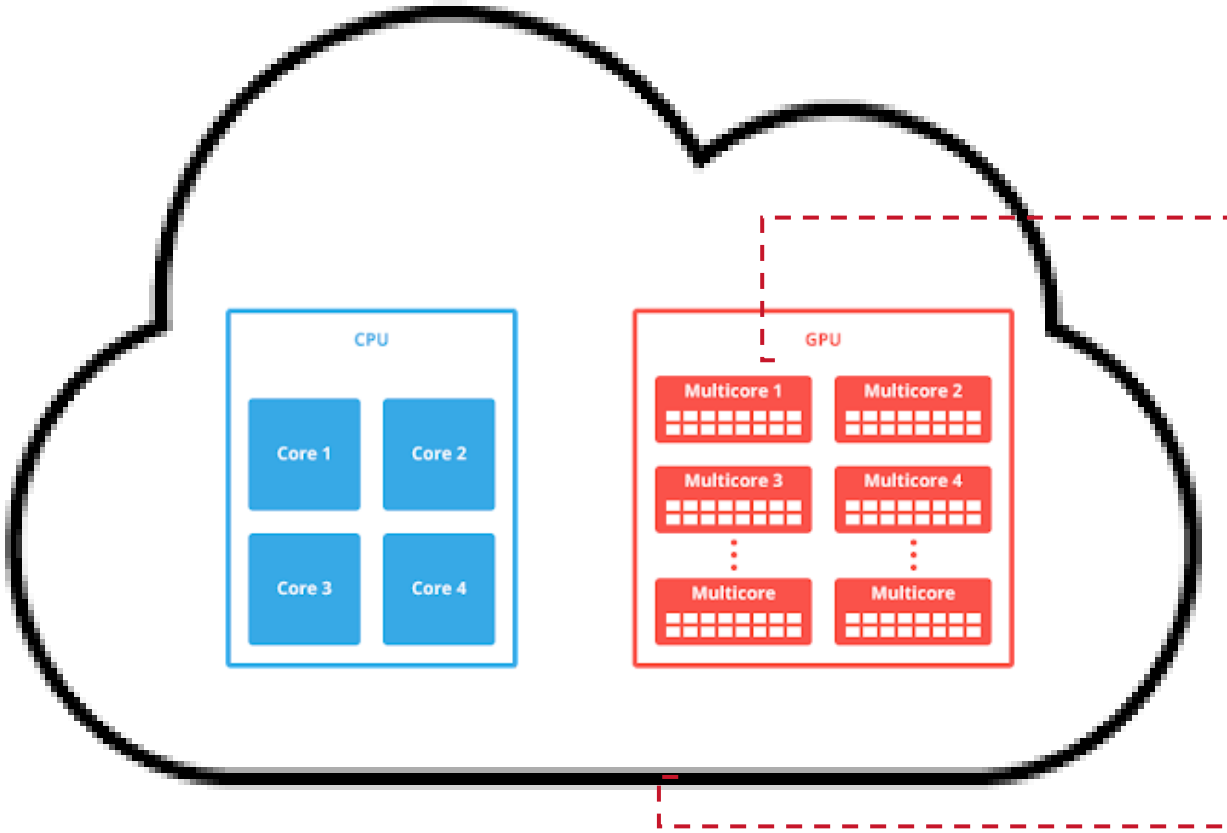
- Auto mesh tunneling technique
- Convergent results with minimum number of mesh elements.



Accurate	Low	High	High
Unknowns	5389	19502	8606

56% Reduction

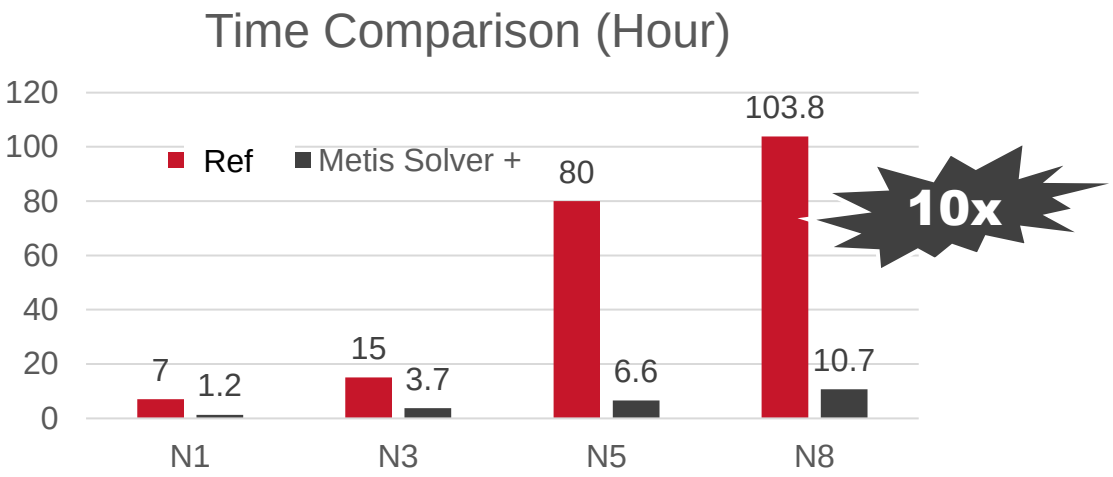
Multicore- and Cloud-Ready

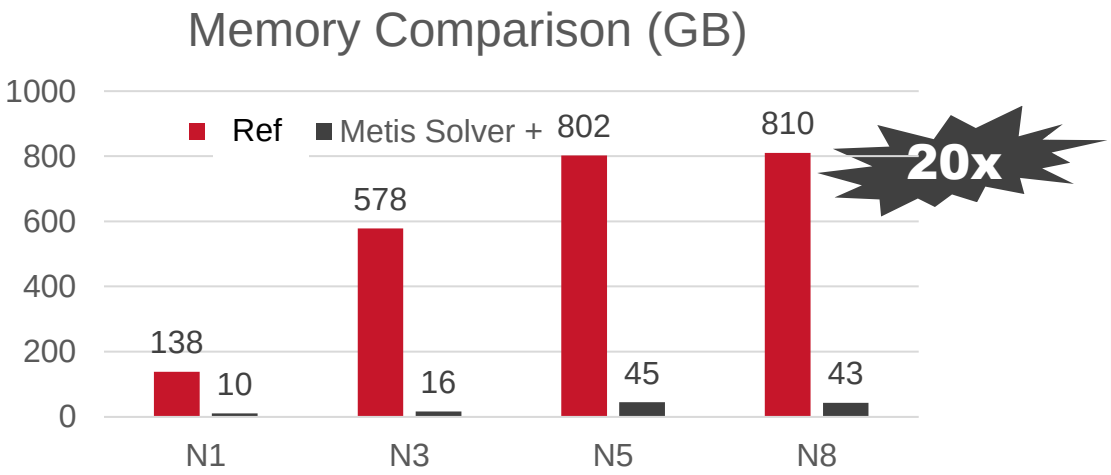


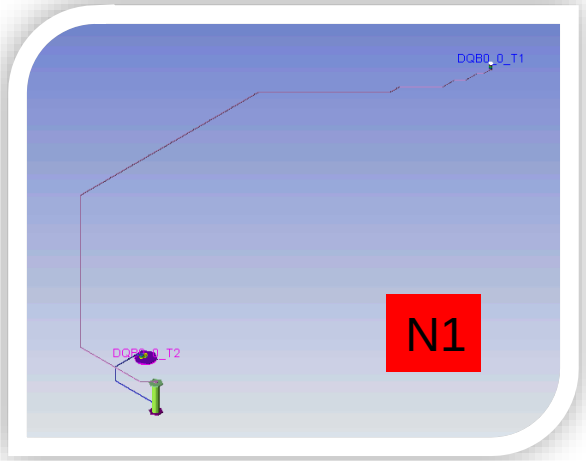
- Shared memory parallel computing should be supported.
- Distributed memory parallel computing is essential for cloud adoption.

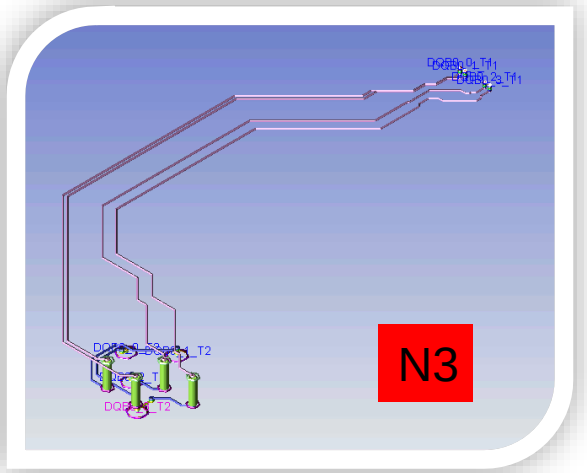
High Capacity and Scalable Solver

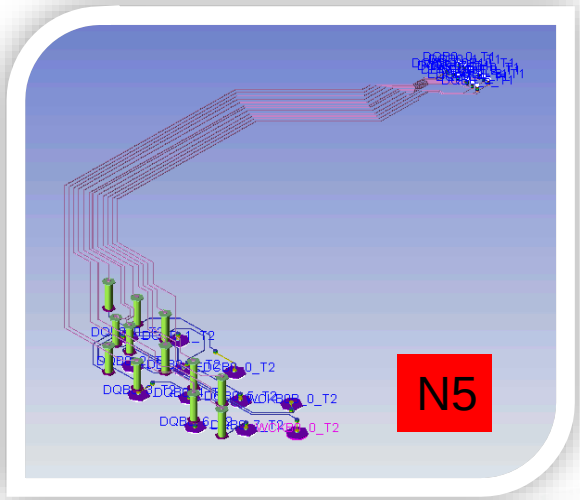
Order of Magnitude Faster than Competitor Tools

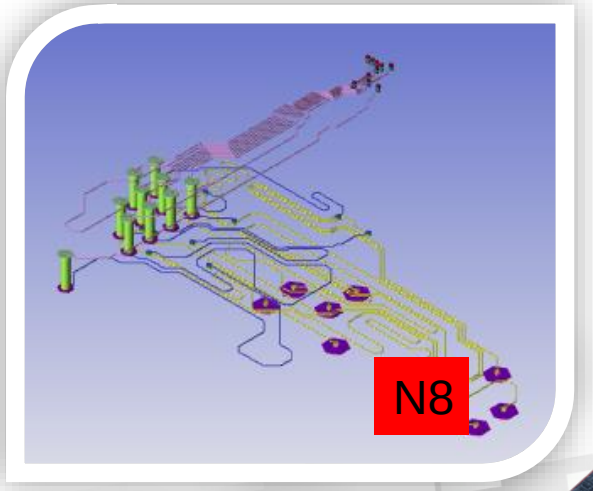






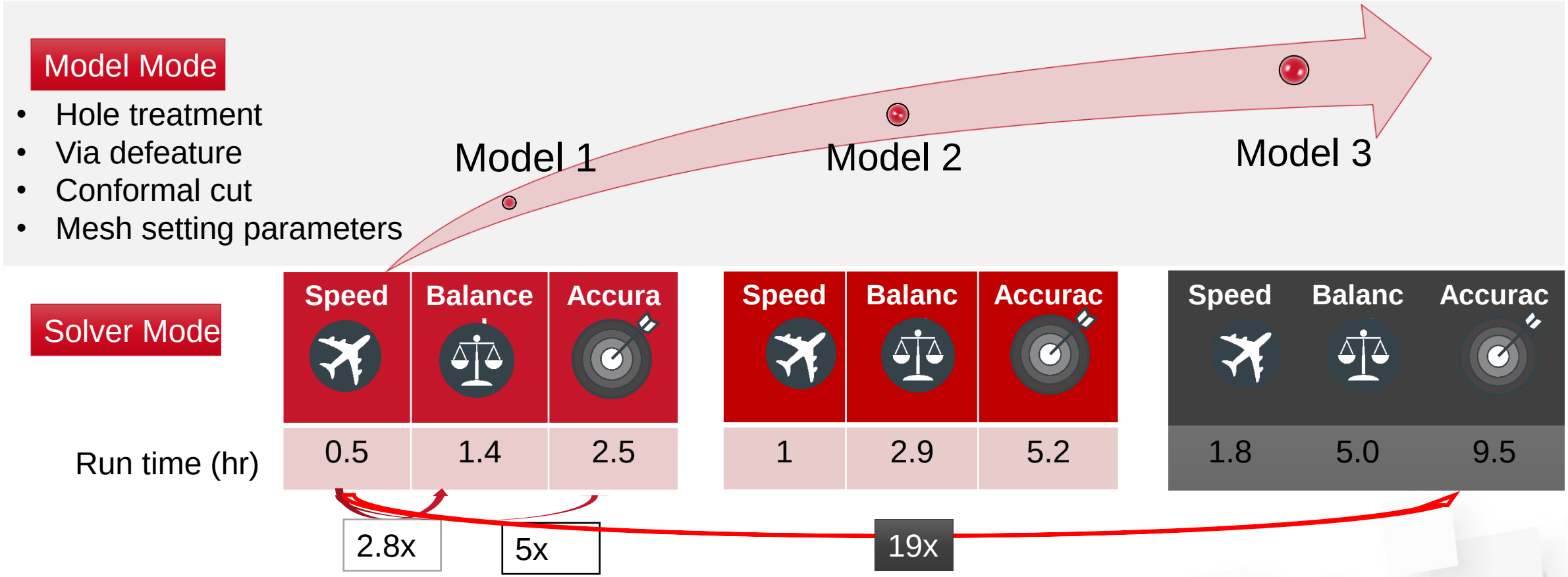




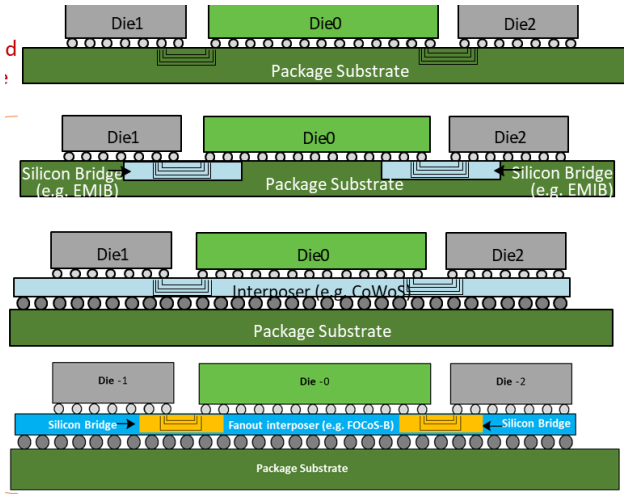


Multi-modes Enable Scenarios from Design to Sign-off

- Geometry simplification and solver modes (speed-balanced-accuracy) cover all your needs for accuracy or speed.



Success with Various Chiplet Cases

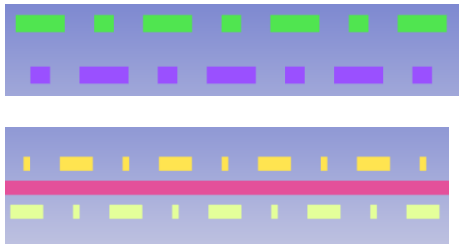


Technology

- TSMC CoWoS-S/R/L
- TSMC InFO
- ASE FOCoS
- Intel EMIB
- Samsung I/H-Cube

Interface

- HBM2/2E/3
- GDDR
- PCI-e



Interconnect

- Coplanar GSGSG with or w/out ground shielding
- Microstrip

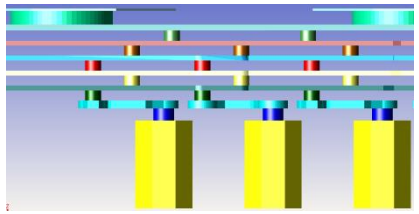
Input format

- GDS + iRCX
- Allegro MCM/SiP
- ODB++

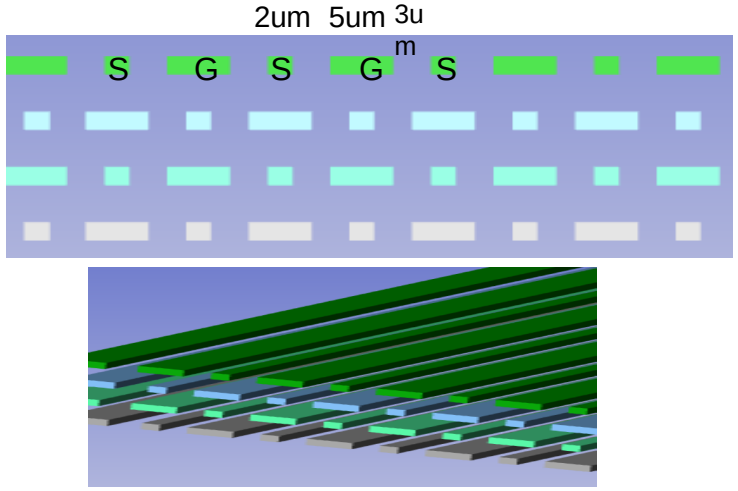
1. HBM Interconnect on CoWoS-R and CoWoS-S

CoWoS-R

TSMC CoWoS-R, 6L Cu layers



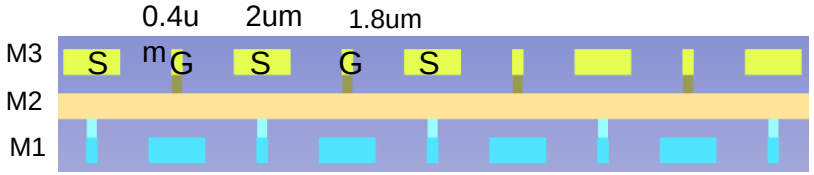
- Coplanar GSGSG
- Routing width/spacing 2um/3um

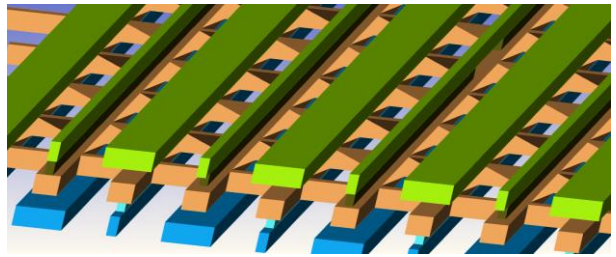


CoWoS-S

TSMC CoWoS-S, 4L Cu layers

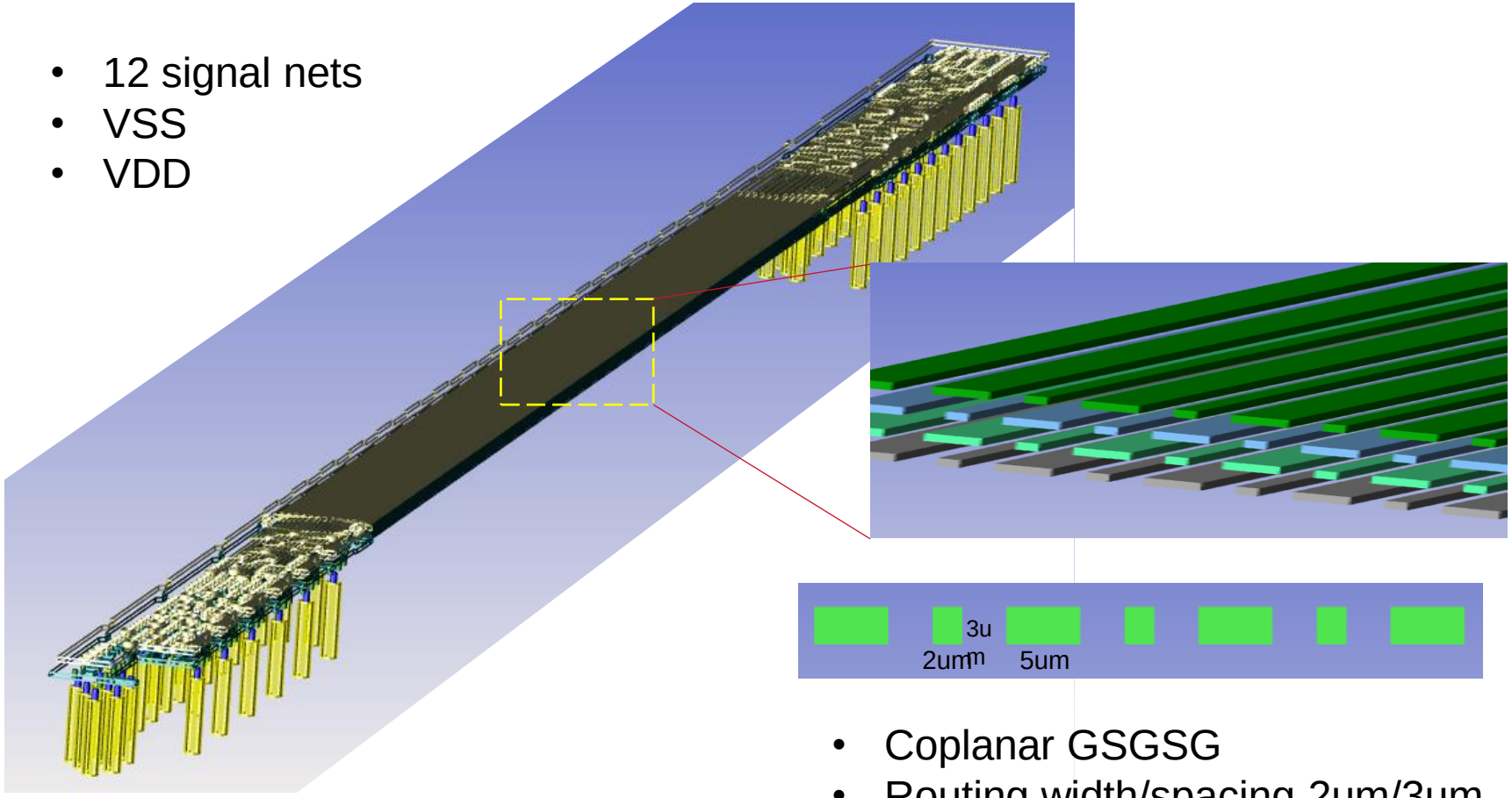
- Microstrip with ground separator
- Routing width/spacing 2um/1.8um





CoWoS-R 12 Nets

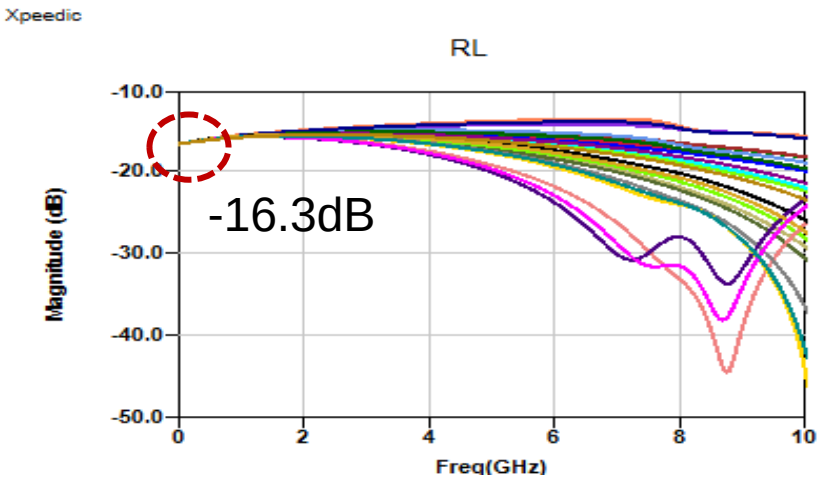
- 12 signal nets
- VSS
- VDD

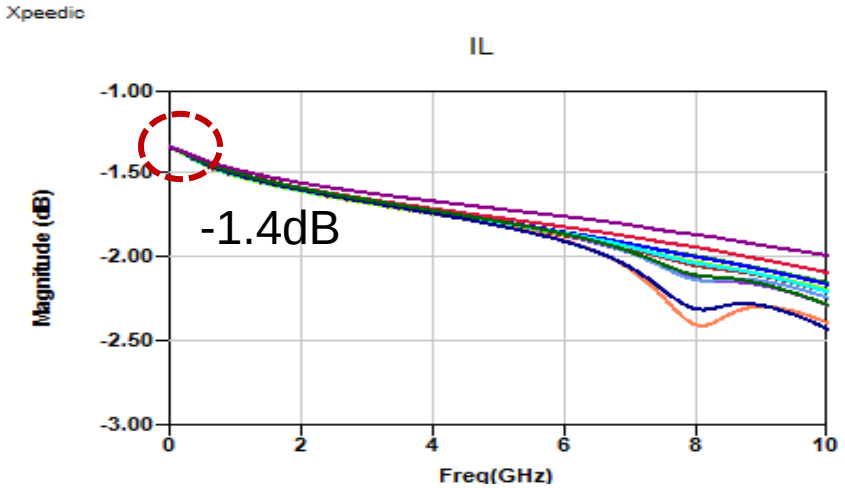


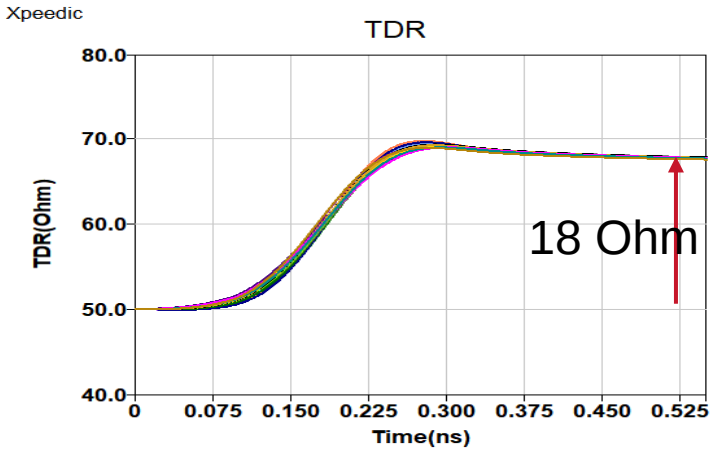
- Coplanar GSGSG
- Routing width/spacing 2um/3um

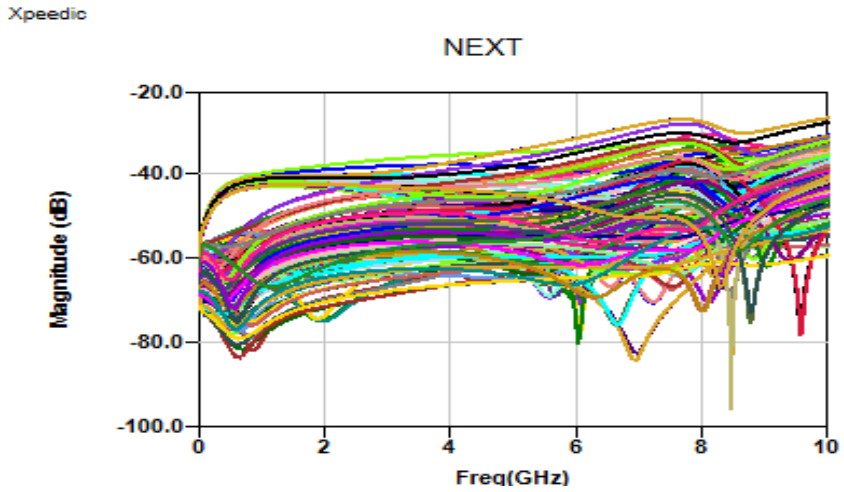
Channel C (12 nets)
HBM0_DM_C[8-9]
HBM0_WDQS_C_T[2]
HBM0_PAR_C[2]
HBM0_DQ_C[64]
HBM0_DQ_C[67]
HBM0_DQ_C[69]
HBM0_DQ_C[70]
HBM0_DQ_C[72]
HBM0_DQ_C[75]
HBM0_DQ_C[77]
HBM0_DQ_C[78]

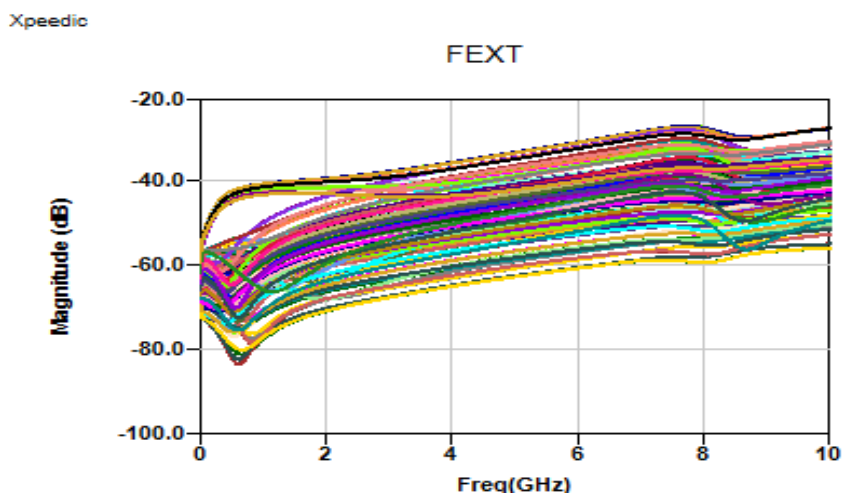
CoWoS-R 12 Nets Results





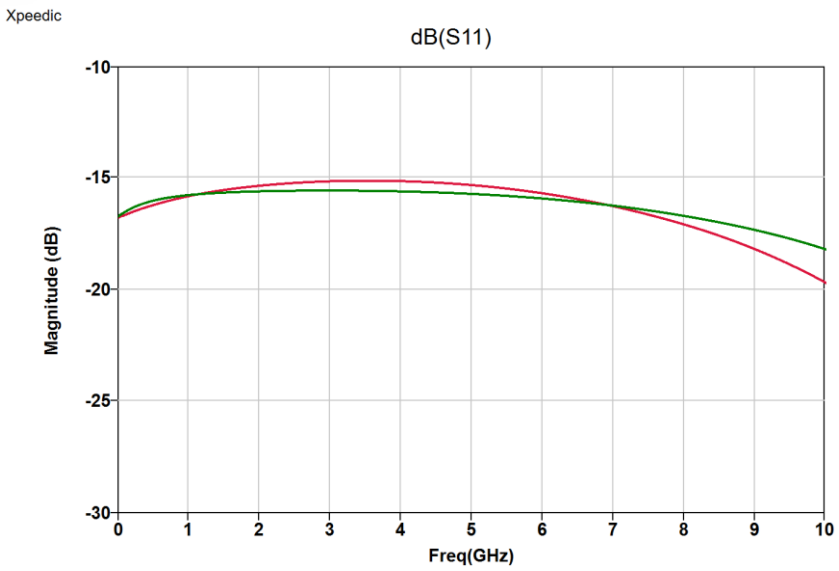


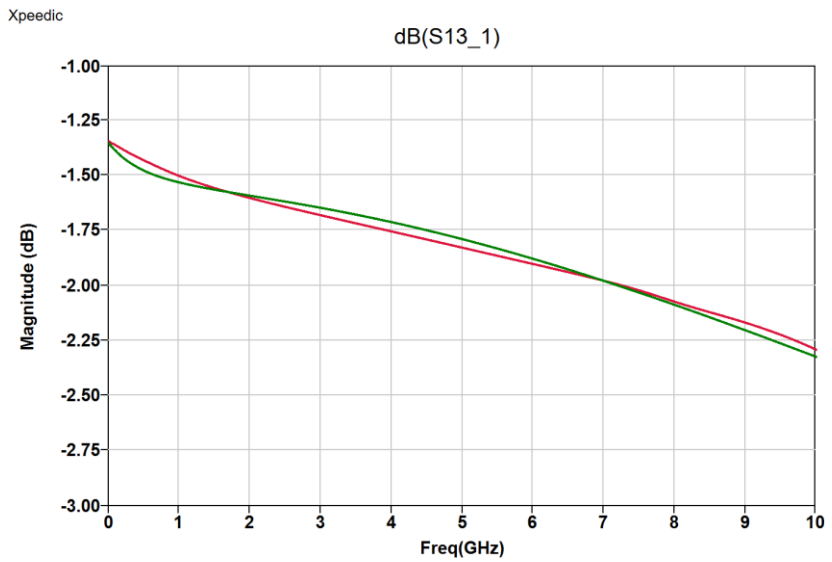


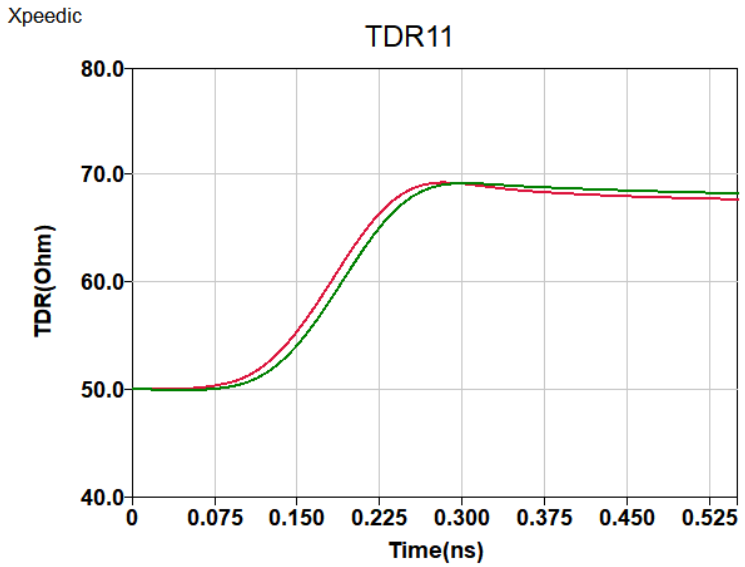


- Rdc=1/sigma*L/W/T=1/5.7e7*5100/2/2.5e-6=18 Ohm
- S11=20*log(Rdc/(100+Rdc))=-16.3 dB
- S12=20*log(100/(100+Rdc))=-1.4 dB

CoWoS-R 12 Nets: Metis vs Reference







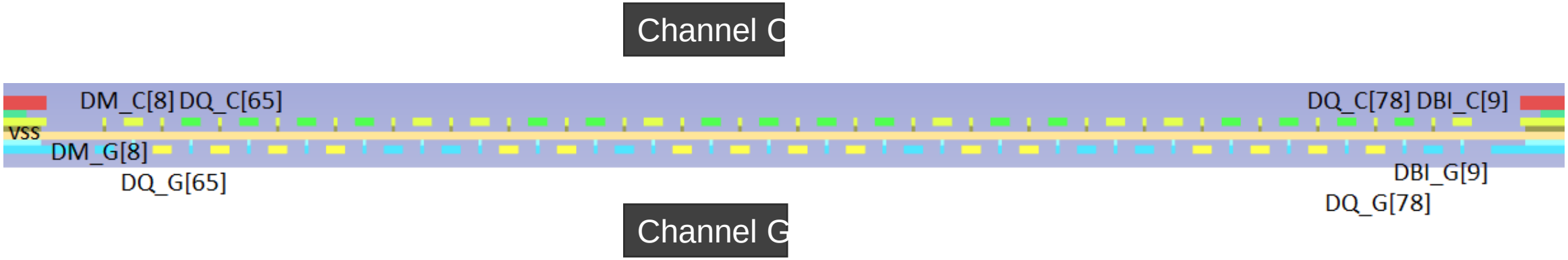
	Freq points	Peak Memory (GB)	WallTime (Hour)
Metis with HPC (10 tasks in parallel)	13	474	2.4
Reference with HPC (4 tasks in parallel)	13	828	24.1

10x

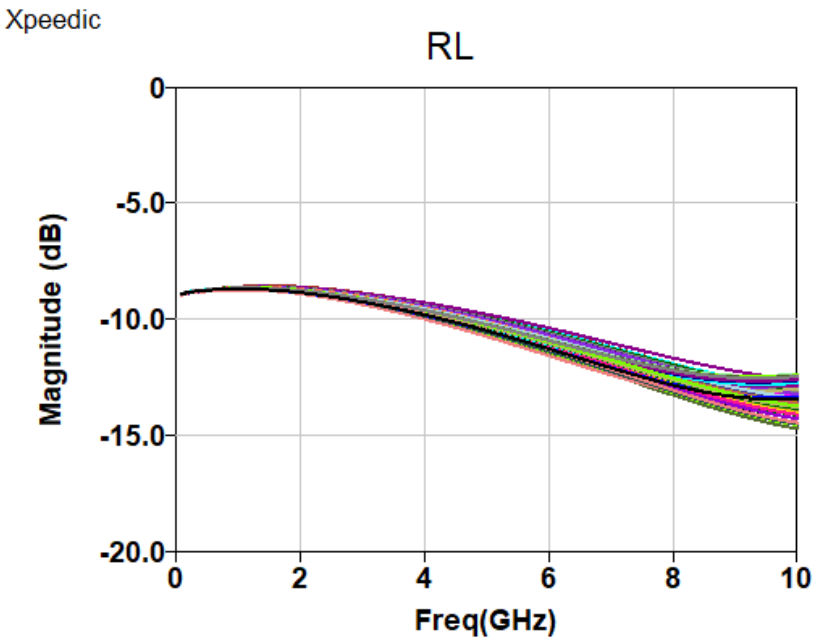
--Metis
--Reference

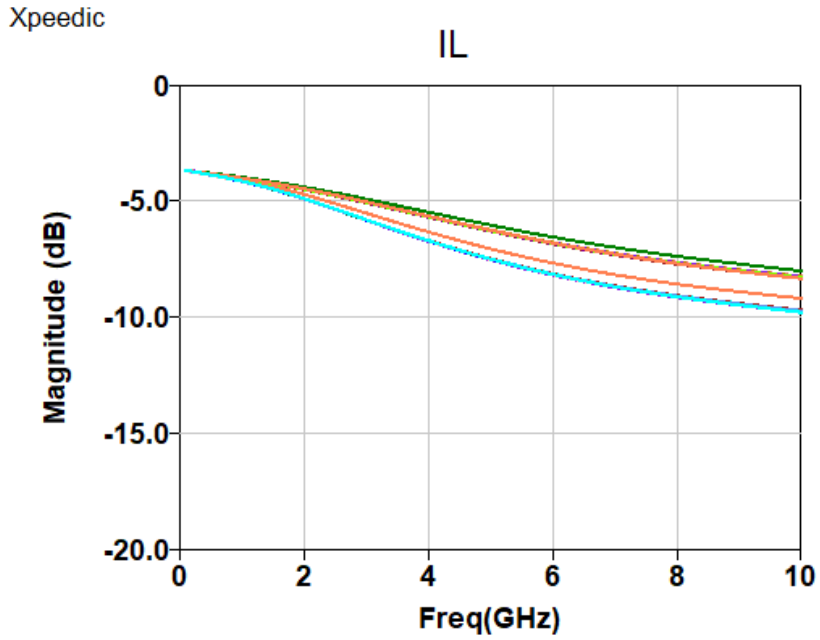
CoWoS-S 48 Nets

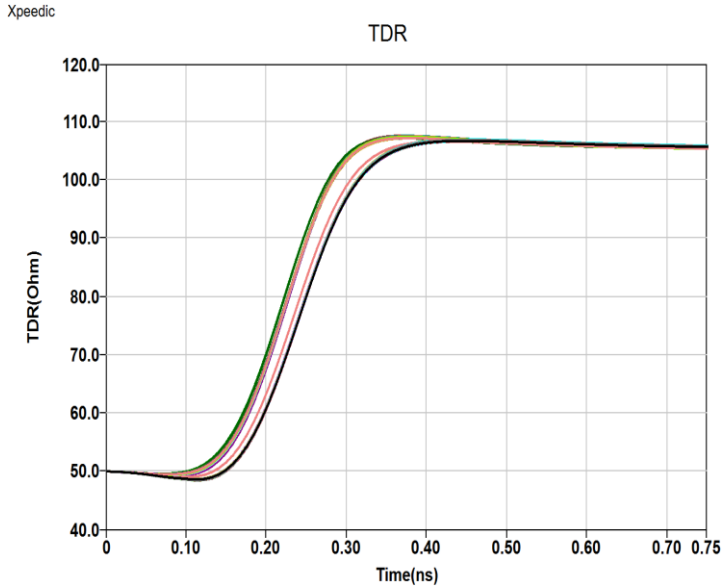
- 24 nets from Channel C on metal3 and the same 24 nets from Channel G on metal1 are simulated
  - 16 DQ's (64-79), 2 DBI's, 2 DM's, 2 WDQS', 1 RD, and 1 PAR



CoWoS-S 48 Nets Results





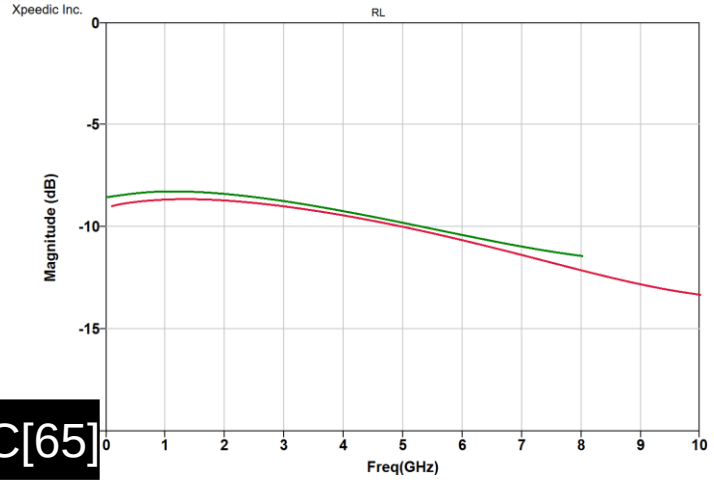


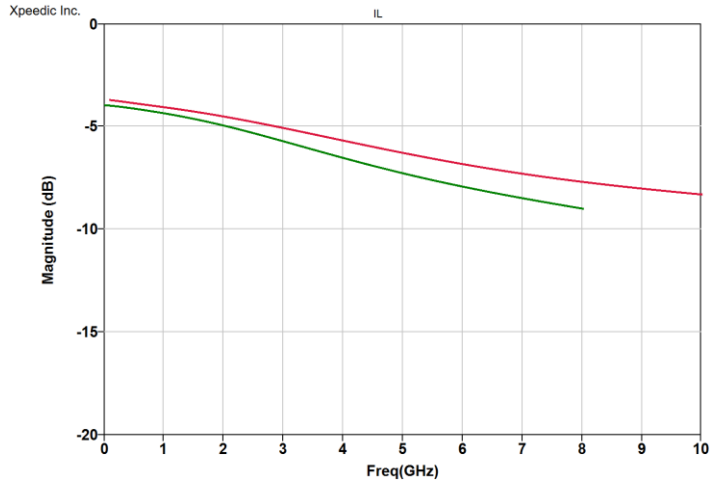
	Freq points	Peak Memory (GB)	WallTime (Hour)
Metis with HPC (5 tasks in parallel)	10	394	17

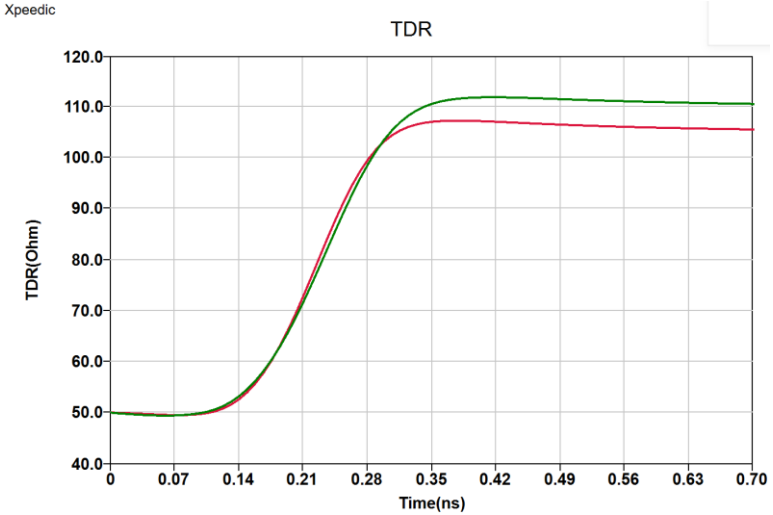
CoWoS-S 48 Net: Metis vs Reference

— Metis
— Reference

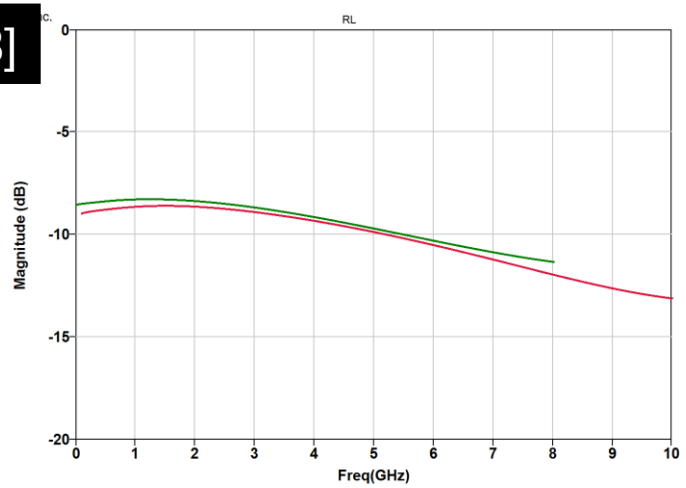
DQ_C[65]

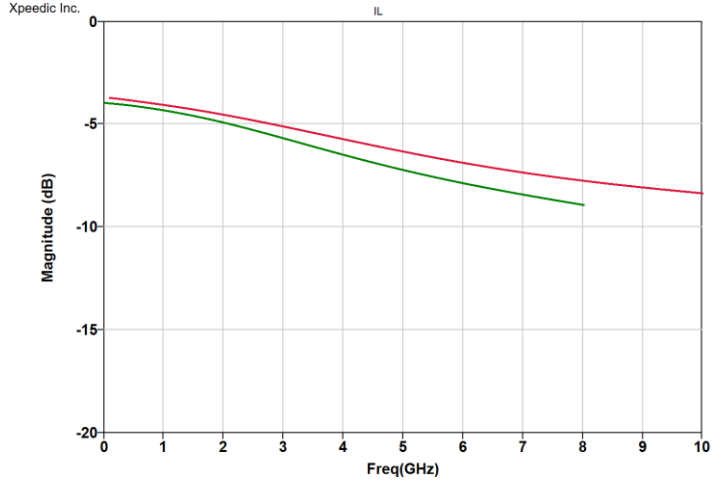


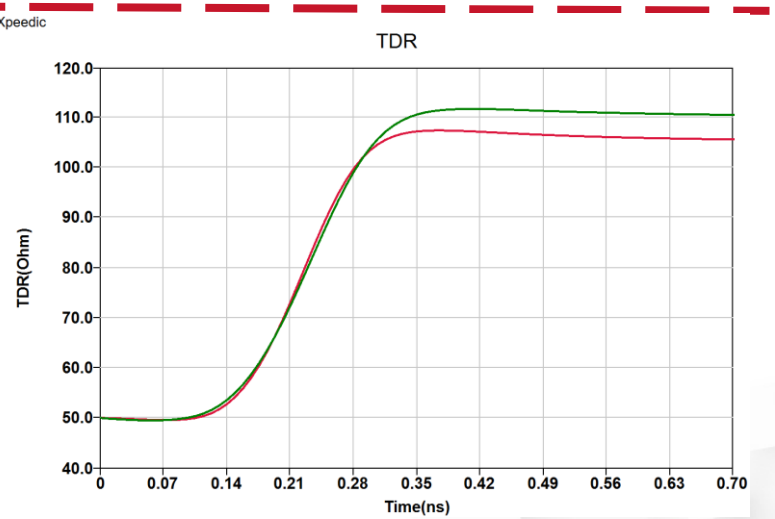




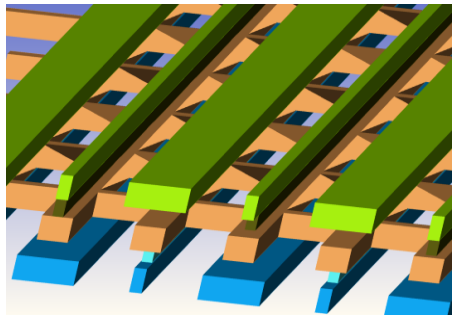
DM_C[8]

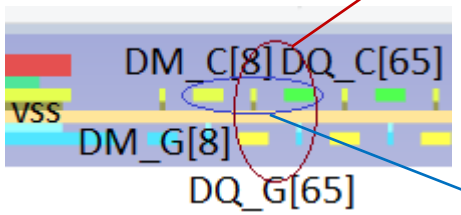




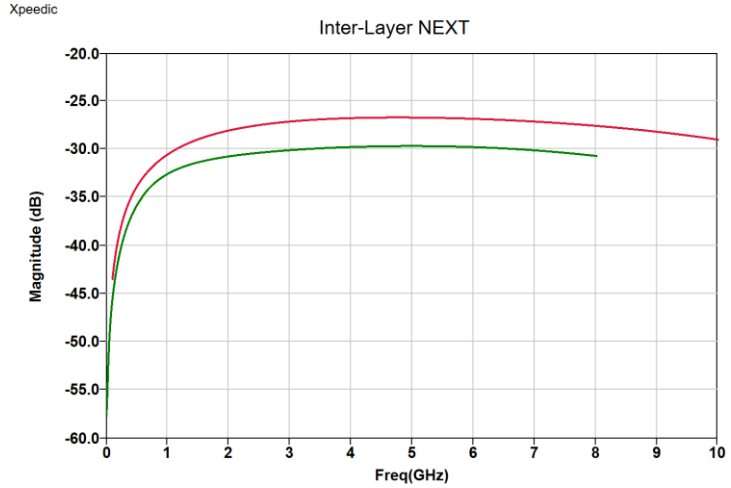


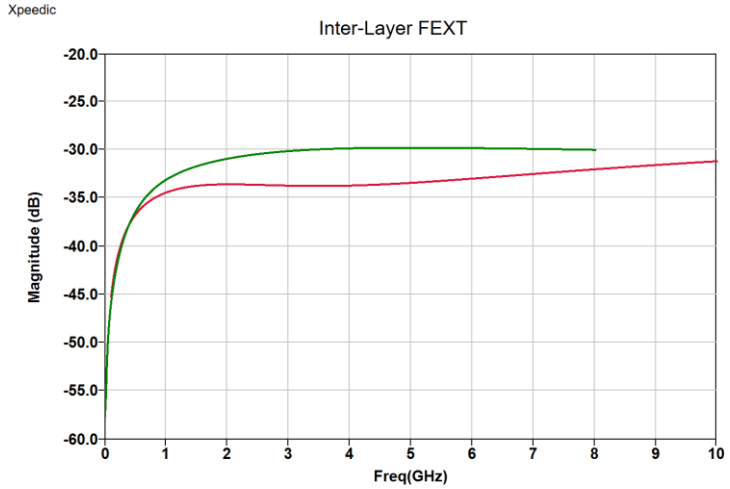
CoWoS-S 48 Net: Inter- & Intra-Layer Crosstalk

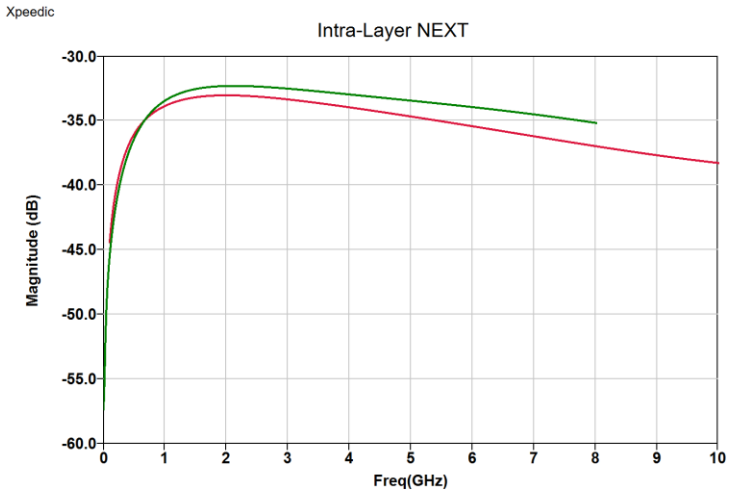


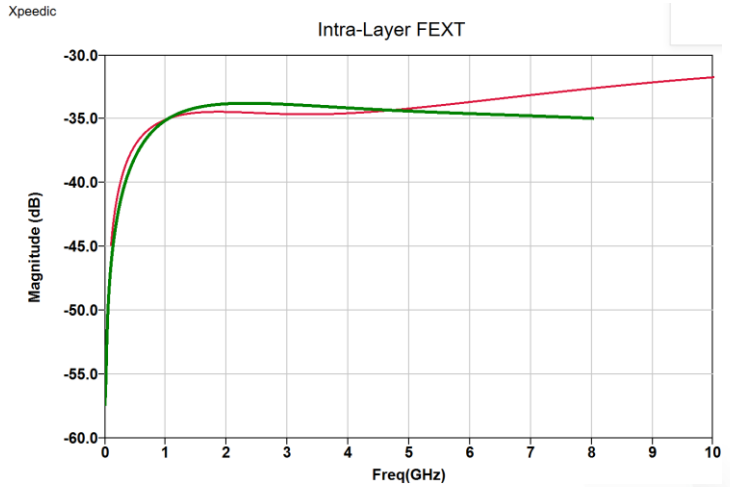


— Metis
— Reference



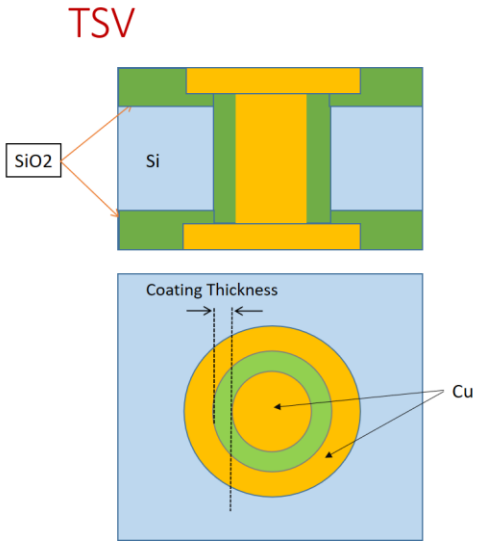


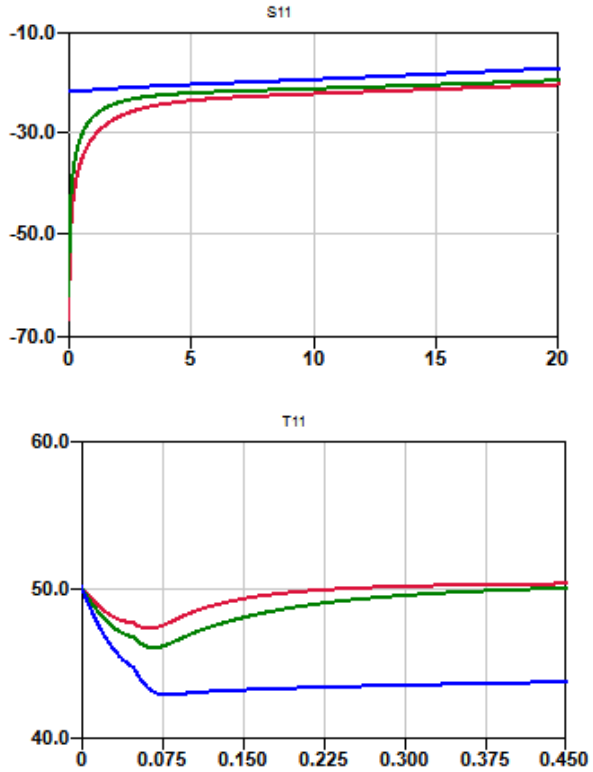


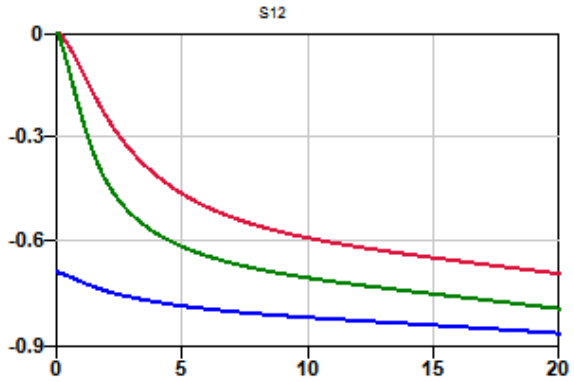


SerDes Channel with TSV on CoWoS-S

- TSV is supported in Metis;
- Metis solver can accurately capture the slow-wave, dielectric quasi-TEM, and skin-effect modes from DC to high-frequencies;
- The TSV coating does not cause significant mesh increase.

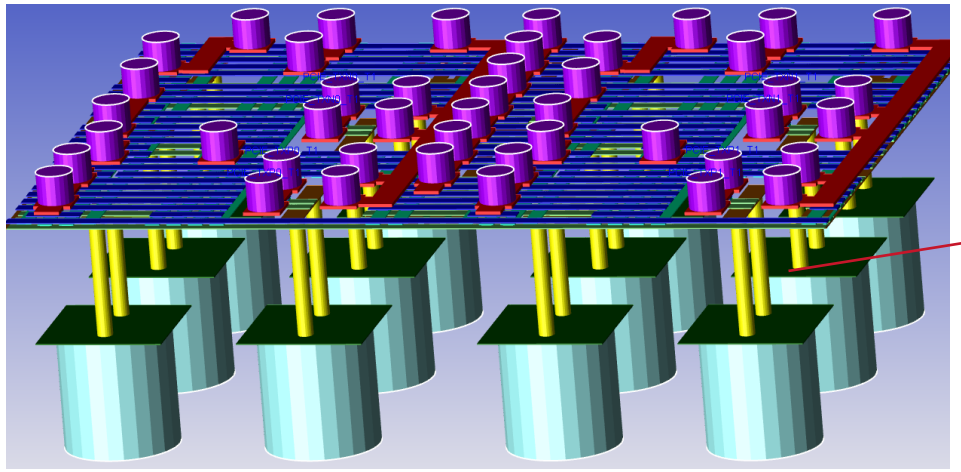


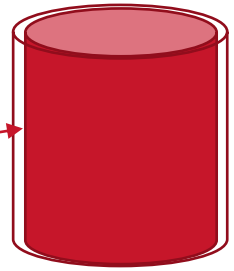




— 1 um coating
— 0.5um coating
— no coating

SerDes Channel with TSV Example

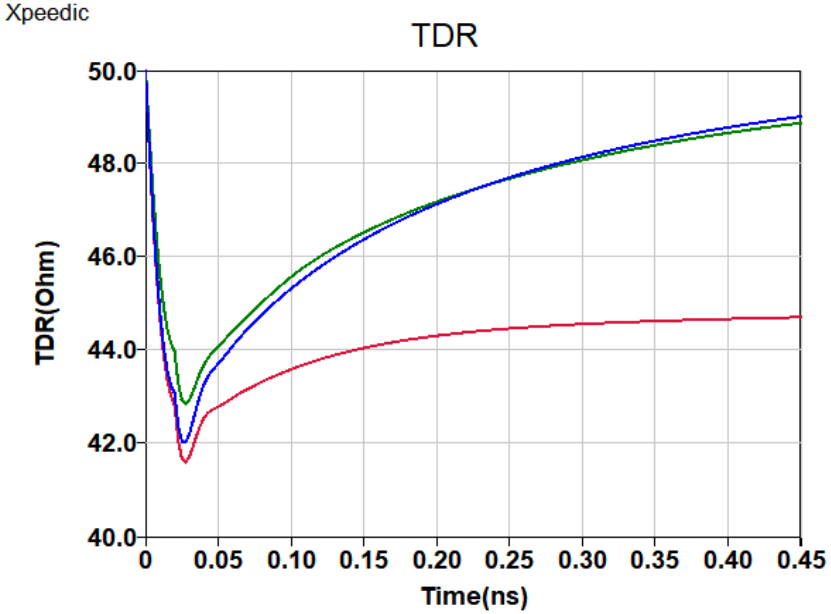




TSV with SiO_2 coating

---Metis (no coating)
---Metis (W/ coating)
---HFSS (W/ coating)

Xpeedic



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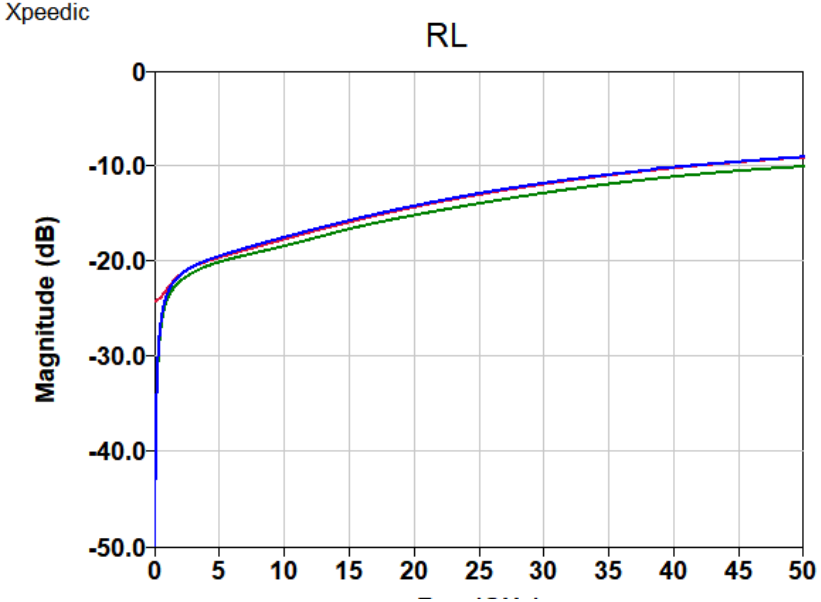

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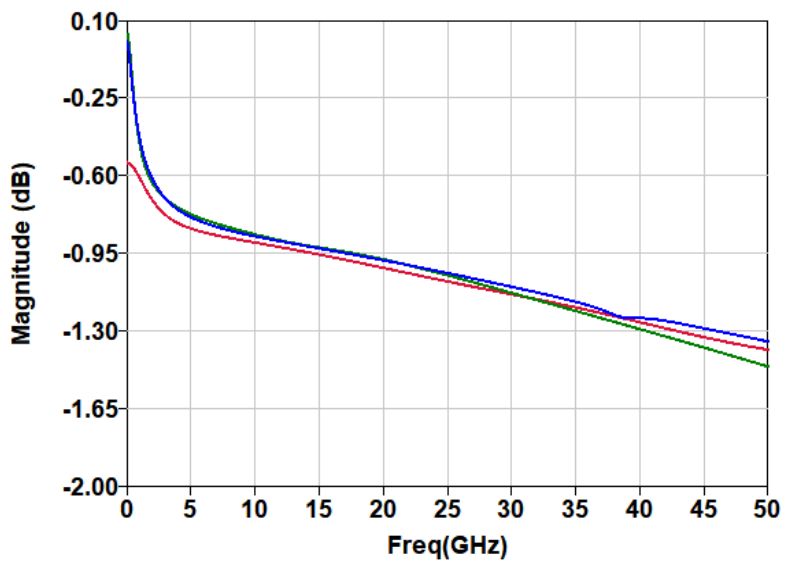
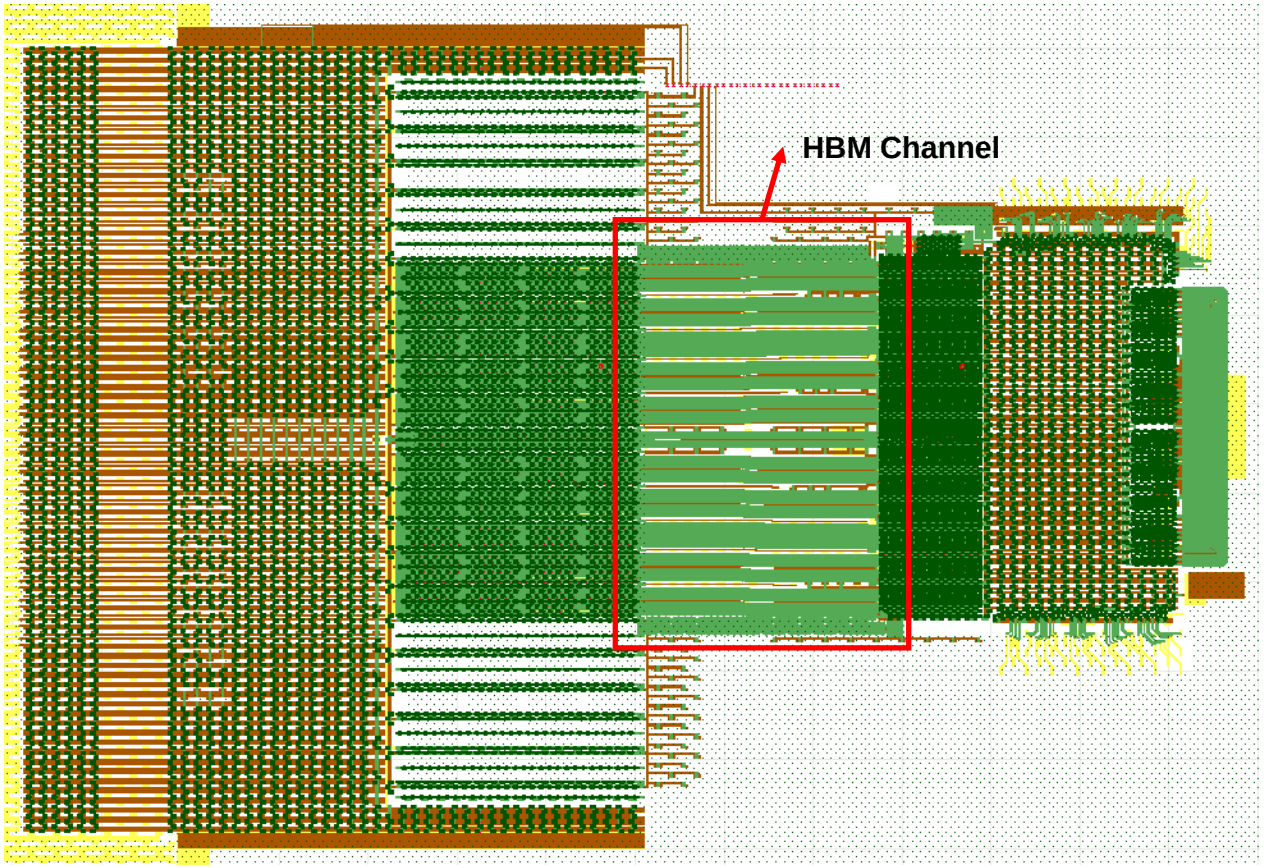
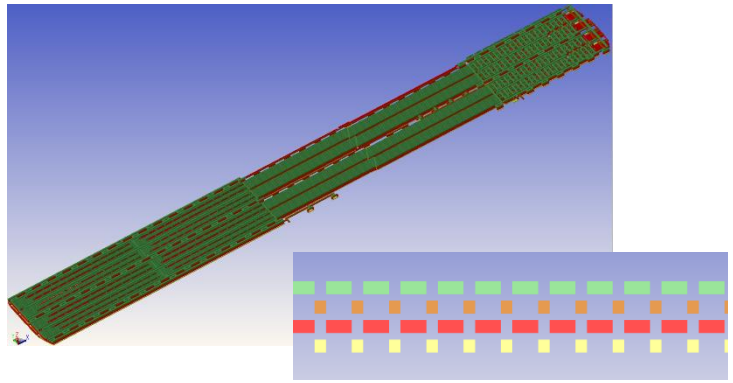
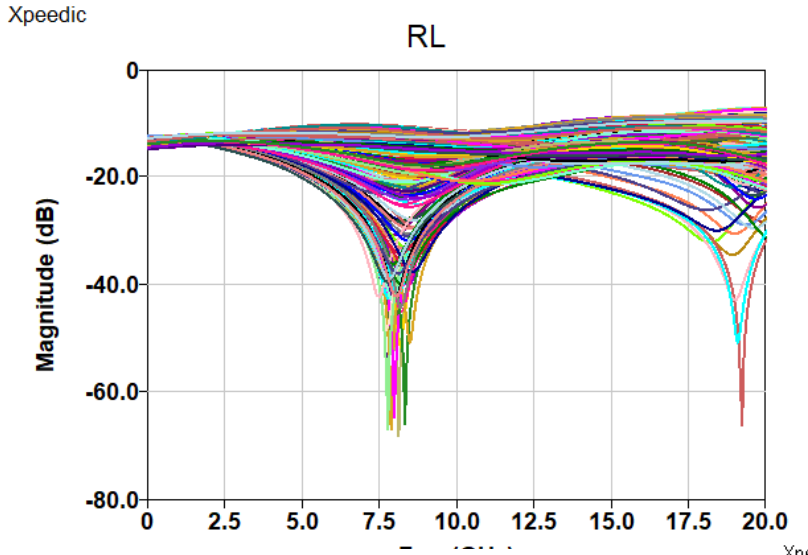


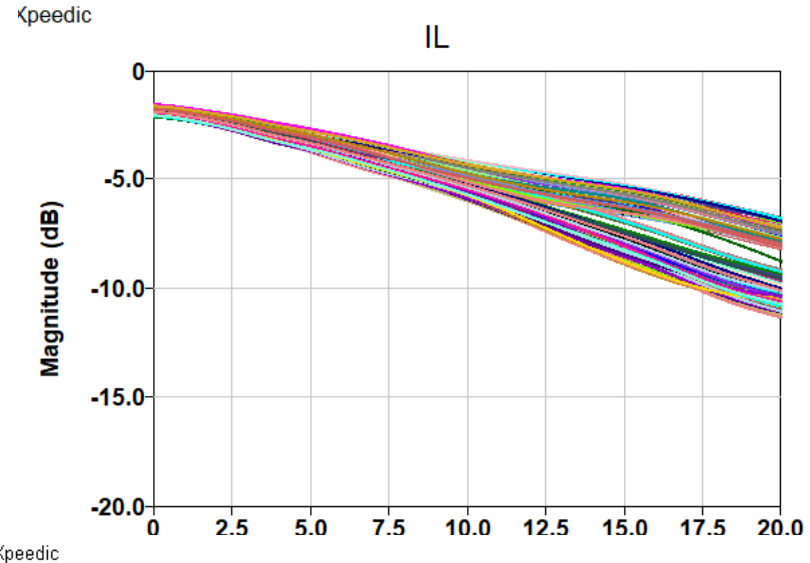
2. HBM Channel with Samsung I-Cube

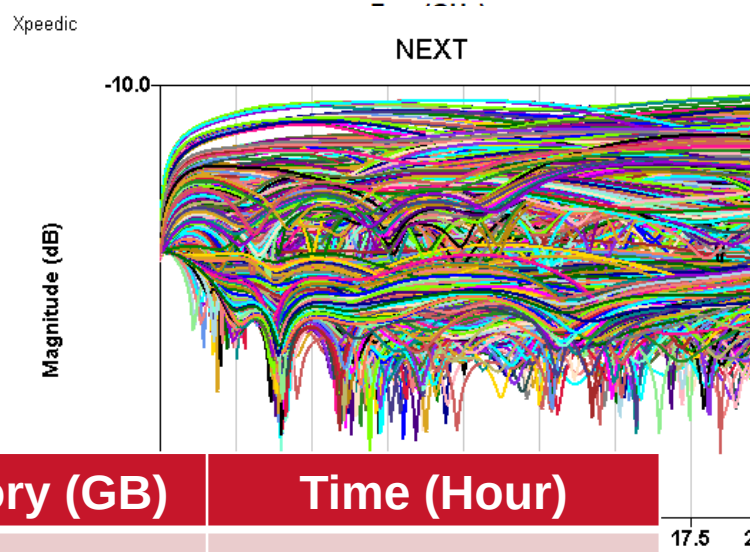


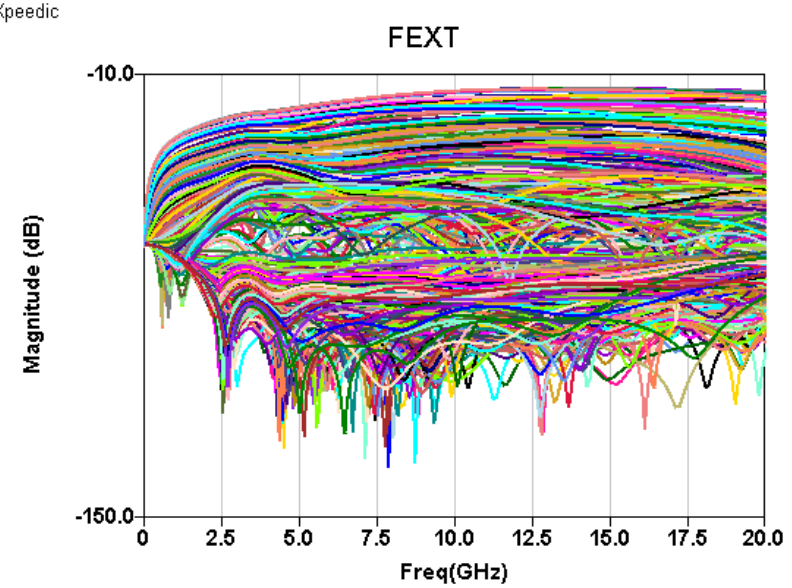
HBM Channel Extraction (192 nets)











A total of 192 nets:

- DQ b/f/j/n 0~31
- DBI b/f/j/n 0~3
- DERR b/f/j/n 0
- DPAR b/f/j/n 0
- ECC b/f/j/n 0~1
- RD b/f/j/n 0~1
- SEV b/f/j/n 0~1
- RDQS b/f/j/n 0_c/t
- WDQS b/f/j/n 0_c/t

	Freq Points	Memory (GB)	Time (Hour)
Metis	20	597	64

Summary

- Chiplet poses great challenges for SI/PI analysis
- A new EM solver is required to cover all the chiplet needs
- The novel EM solver from Xpeedic enables accurate and efficient simulation for chiplet designs
- Success stories on various chiplet designs demonstrate its key advantages on capacity and accuracy.