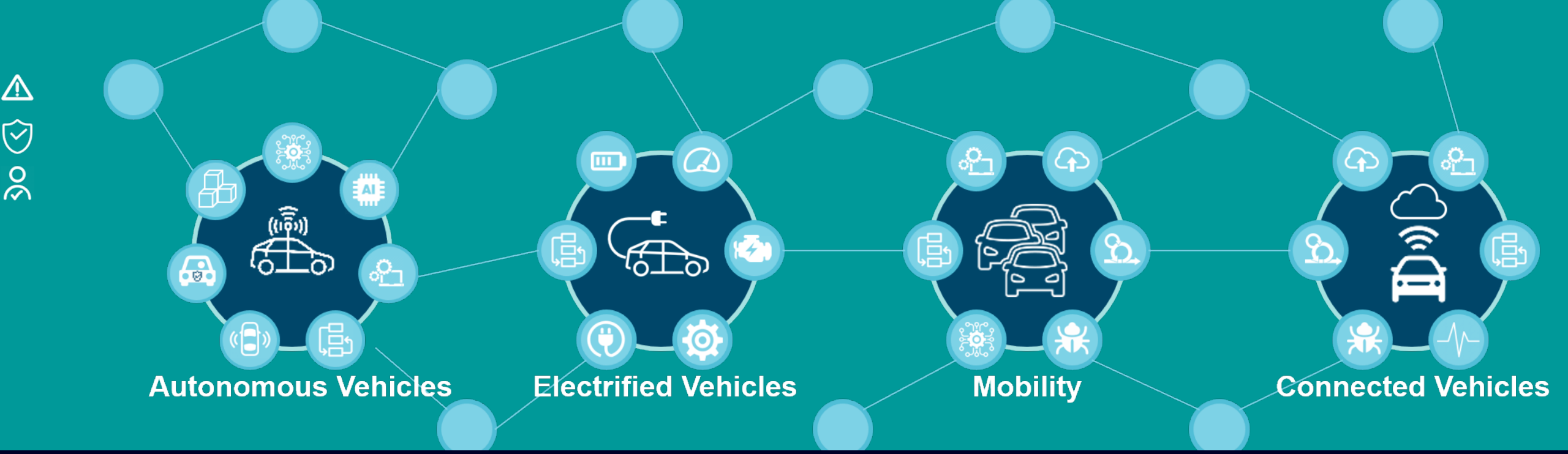

Chiplets - a platform-concept for automotive ADAS systems

Andy Heinig - Group Manager System Integration - Fraunhofer IIS
Keith Felton – Manager Product Marketing Semiconductor Packaging – Siemens EDA

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AGENDA

1. Trends in automotive electronics
2. Monolithic SoC limitations
3. Hardware solution for Chiplets
4. Chiplet interface standards
5. Solution for ADAS ECUs

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Electronics innovation and Automotive Segment Growth

AUTONOMOUS

- Functional Safety
- Safety systems
- Connectivity
- Navigation

By 2030, 50% of automotive costs will be electronics-based

– Statista

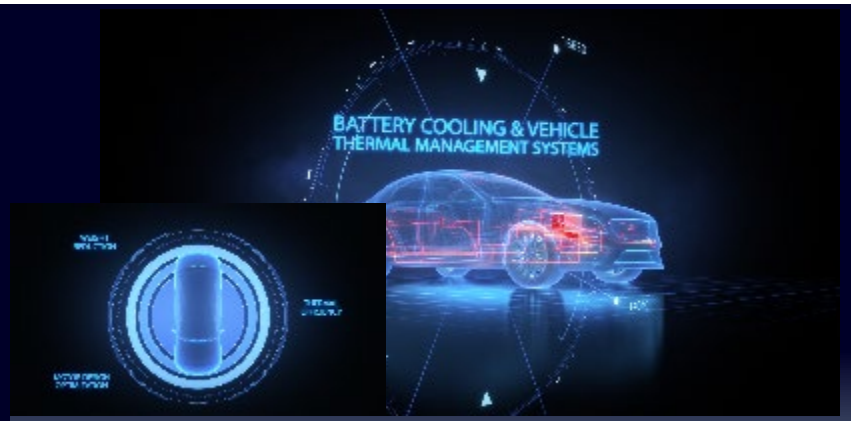
ADAS

- DIS
- Infotainment
- ACC
- CAS

Over 1700 new startups enter the automotive segment

- CBinsights

ELECTRIFICATION



- Power Electronics
- Electric motor control
- Thermal management

2020 - 5M zero-emission vehicles in China

2030 – Only zero emission vehicles produced in Germany

2040 – Only electric cars allowed in UK

– Trendwatch

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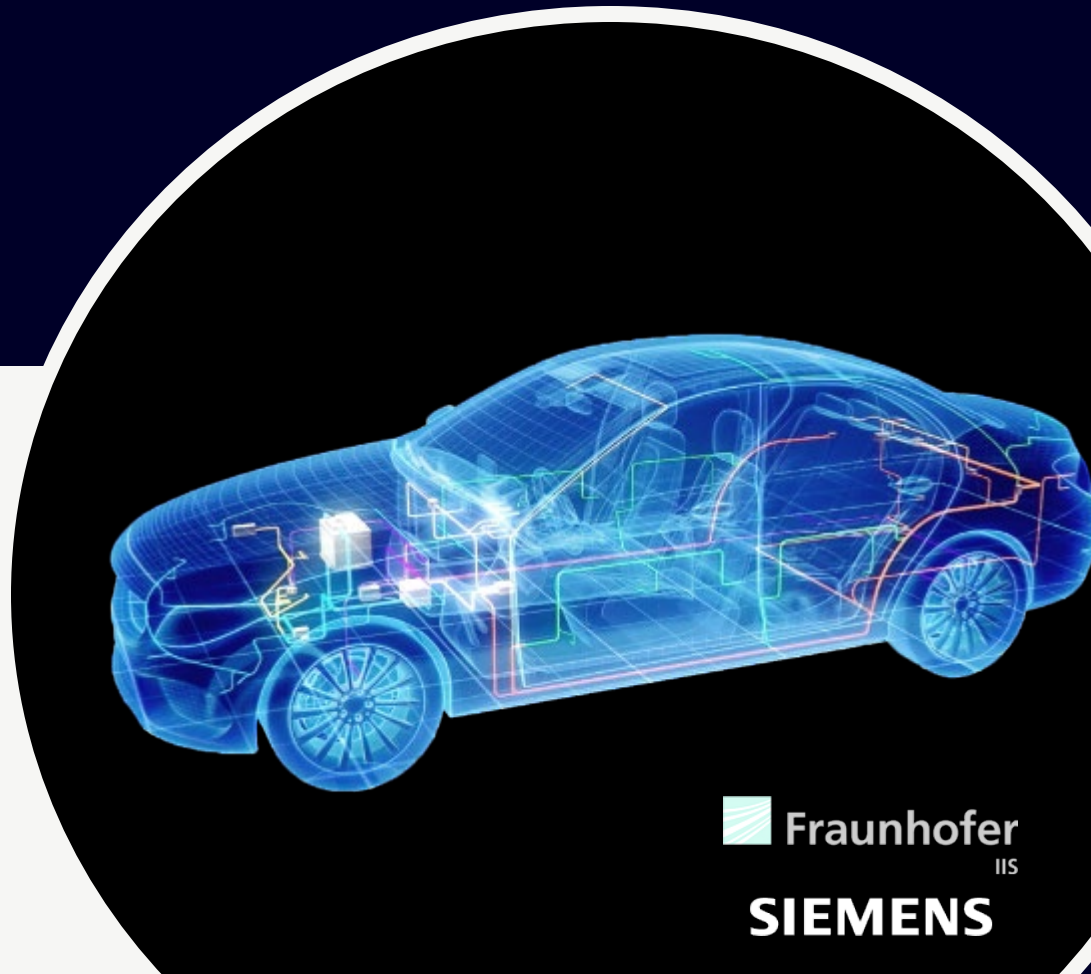
“80% of product innovation and differentiation [is] now electrical, electronics and software.…”

- Siegmar Haasis (Daimler R&D CIO)



By 2030, 50% of automotive costs will be electronics-based

Statista, 2019

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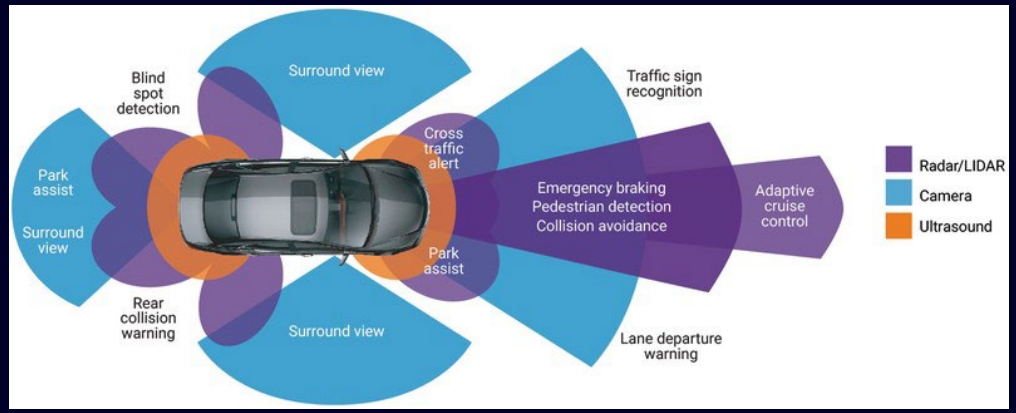
Challenges for automotive ADAS/Autonomous electronics

Significant processing power needed for ADAS and autonomous functionality	Higher levels of functional integration	Advanced technology nodes necessary for both digital and memory devices	Need for lower power consumption
Centralized system processing versus decentralized	New implementation concepts – 1, 2, 4 main processing units (number of SoCs)	Configurability/Adaptability for different vehicles and markets	Cost of design NRE and units



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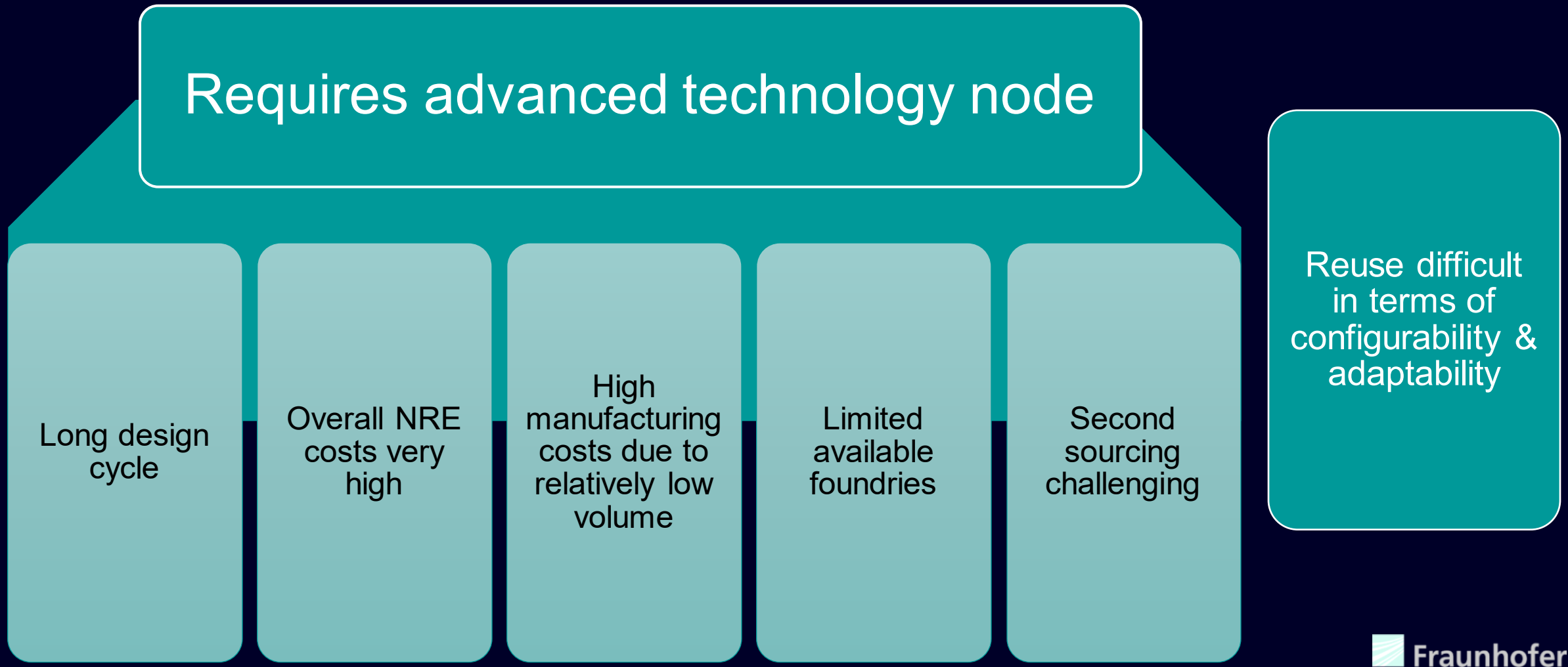
Traditional Monolithic System-on-Chip (SoC) ECU



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Heterogeneous Integration using chiplets

Disaggregation of SoC functionality into smaller node optimized blocks or chiplets

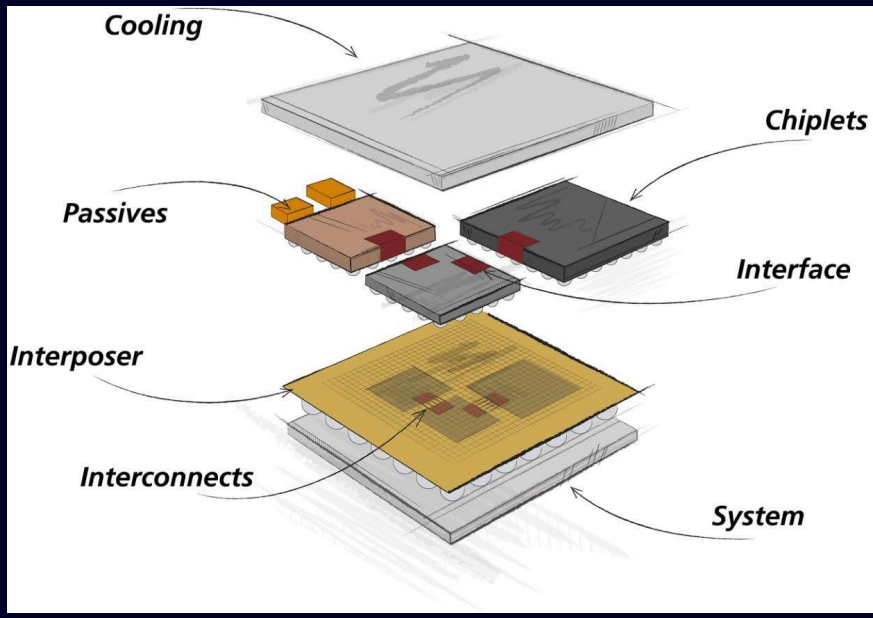
Standardized interfaces allows plug-and-play of different functional blocks/chiplets (logic, analog etc…)

ECU is defined at the package level through Heterogeneous integration

Reuse of basic blocks possible for configurability/adaptability

Multiple sources of chiplets possible

Multiple sources of system assembly/integration possible



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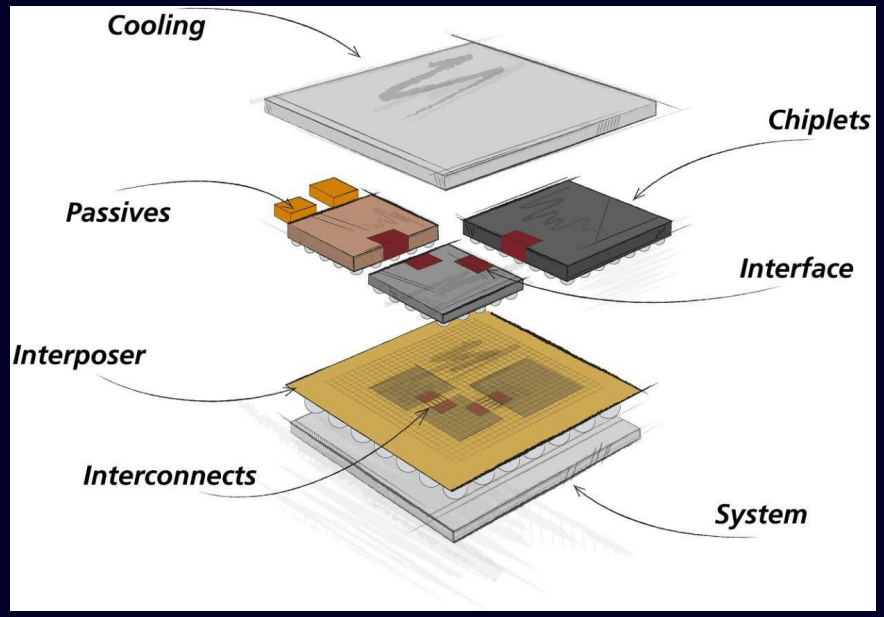
Heterogeneous Integration using chiplets

- Integration of different technologies
  - Digital – Processor, Accelerators
  - Analog
  - Memory
- Different chiplet interface protocols required
  - Single cores together to clusters e.g. AXI
  - Analog together with processors e.g. low level protocols
  - Memory together with processor e.g. HBM, LPDDRx



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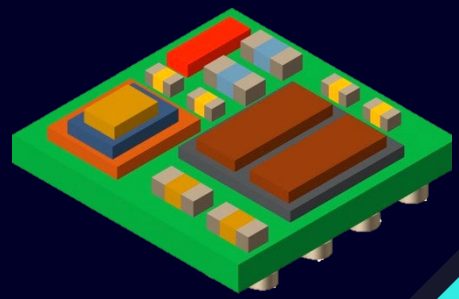
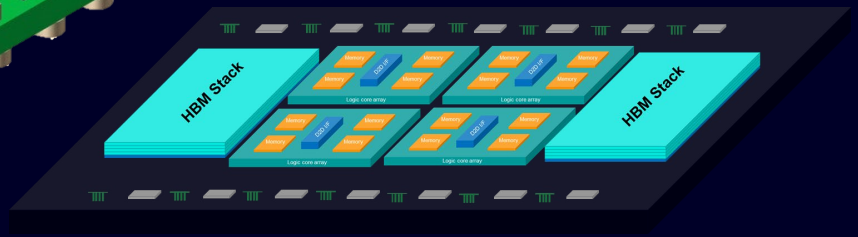
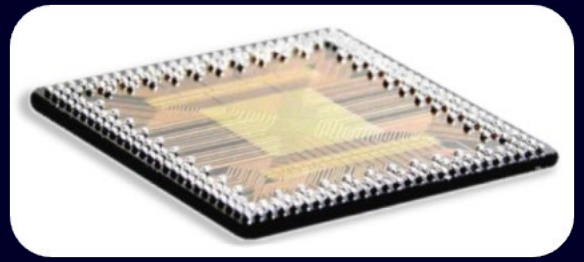
Choosing the right integration platform

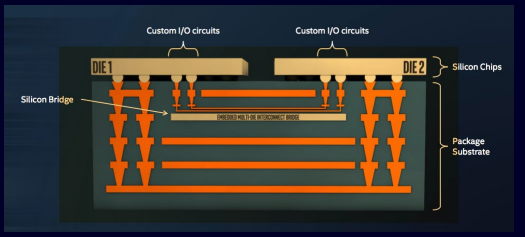
Many to choose from

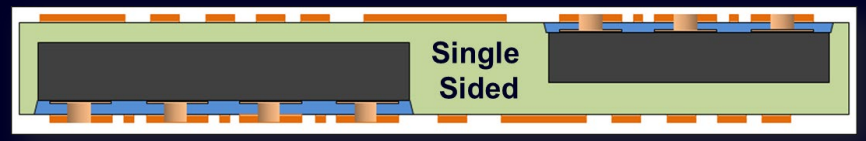
- Laminate based
- Interposer based (organic or silicon)
- FOWLP (RDL build up)
- Silicon bridges (in laminate or FOWLP)

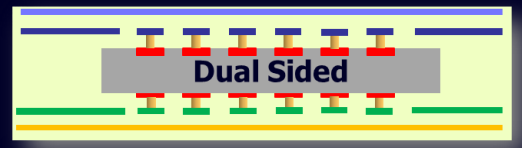












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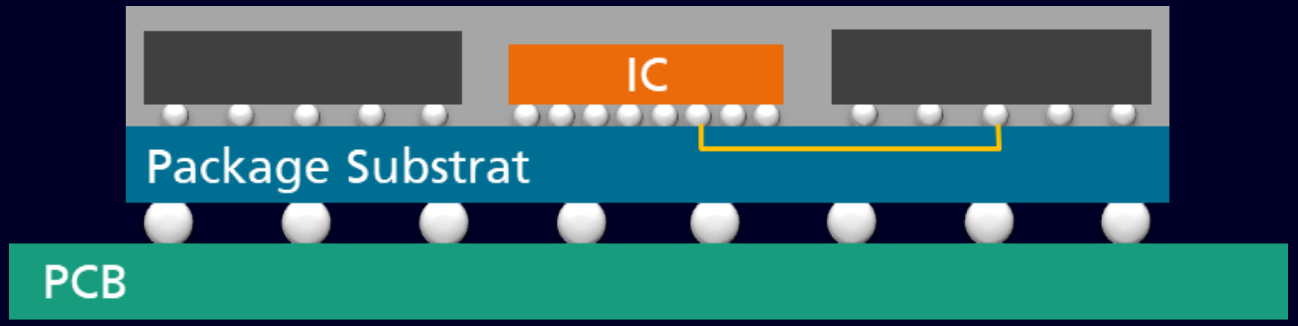
Substrate integration options – Organic Laminate

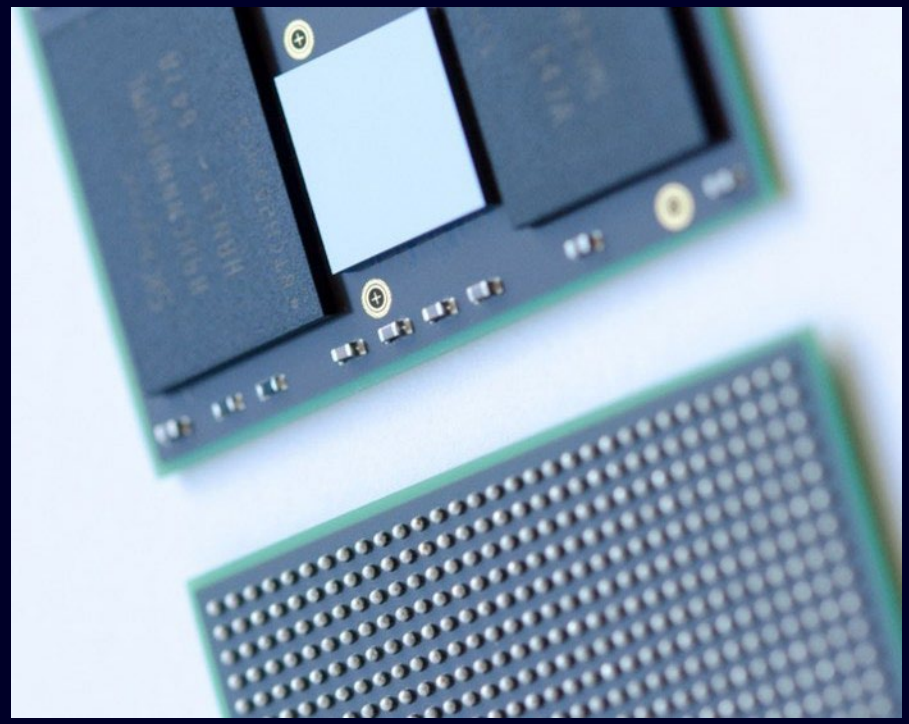
Advantage

- Classical proven solution
- Very low-cost

Disadvantage

- Only large line/space possible
- Uses more power





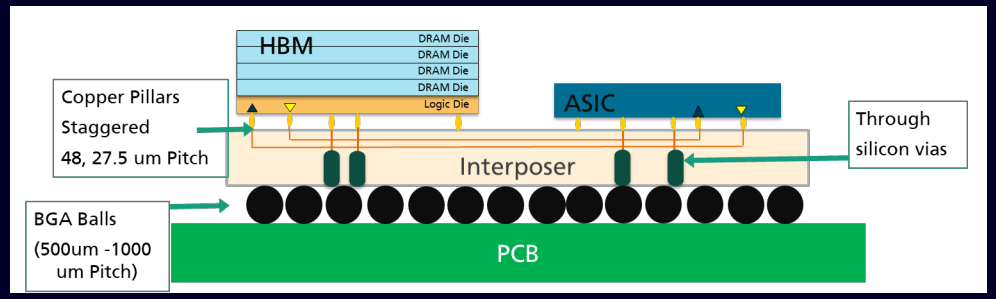
Substrate integration options - Interposers

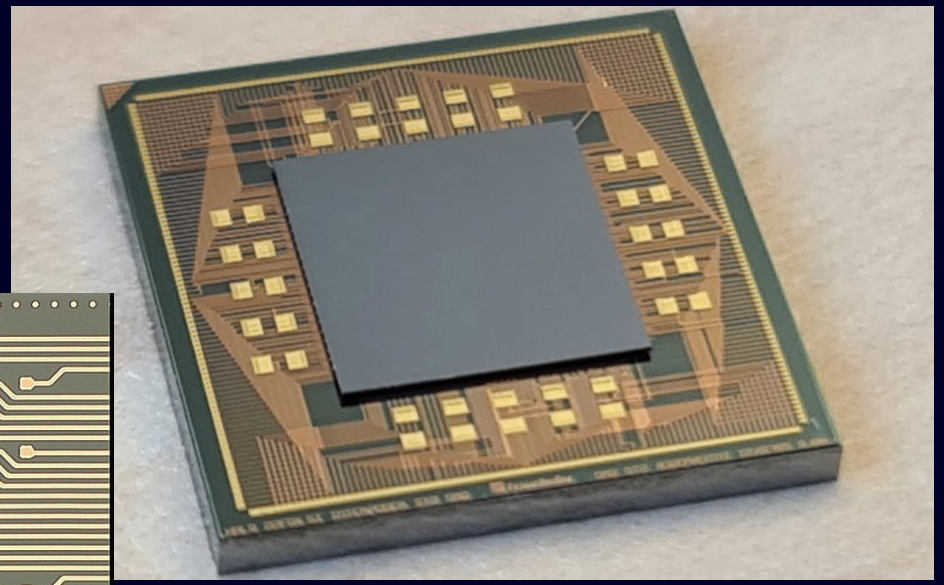
Advantage

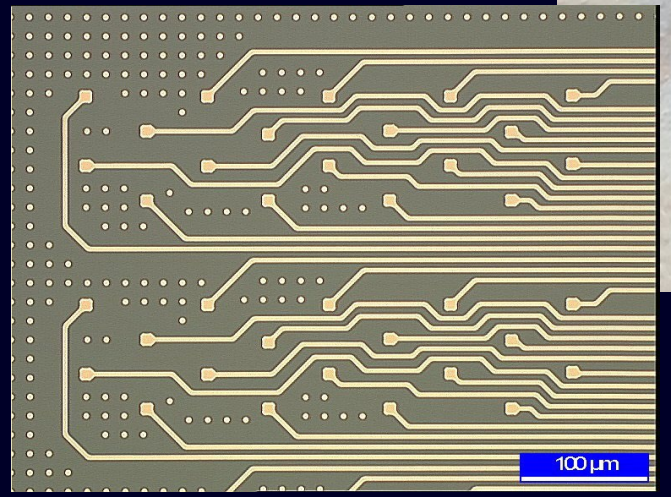
- Good warpage control with large systems
- Very fine Line/Space possible

Disadvantage

- Expensive solution







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Substrate integration options – Chips last FOWLP

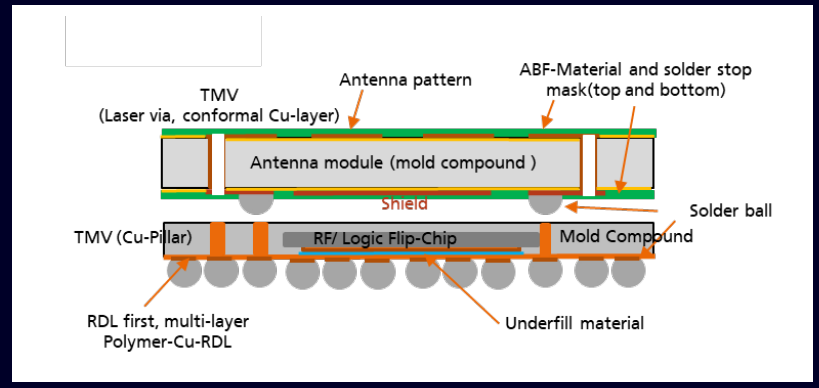
Advantage

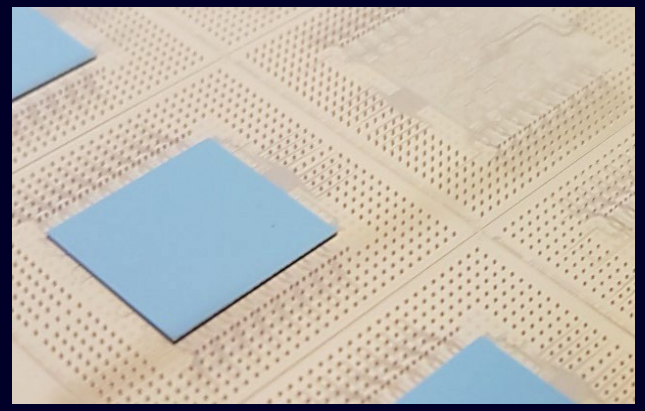
Low cost

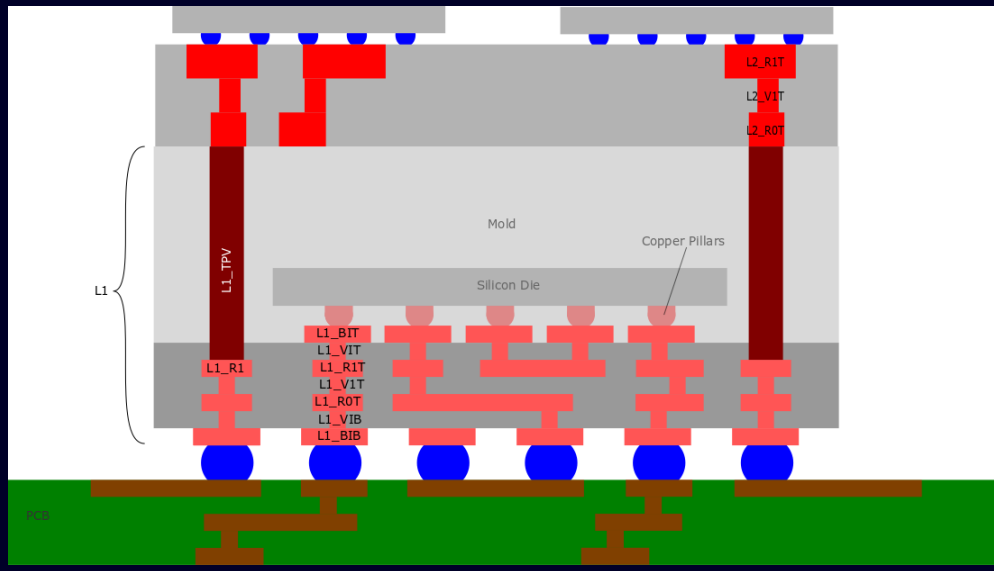
Very fine Line/Space

Disadvantage

Warpage at larger systems







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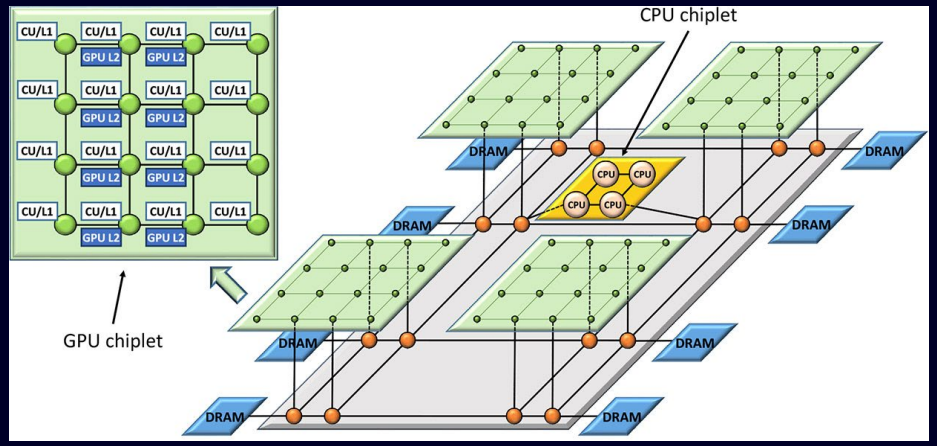
Connecting everything with interfaces

- Chiplets require die2die I/O interfaces so they can perform as an integrated device
- The fewer interface protocols adopted increases integration opportunity & flexibility
- Many protocols exist and are being developed
- BoW
- AIB
- SerDes XSR/USR
- UCIe
- HBM2

Chiplet Interface Protocols - Bunch of Wire (BoW)

Published standard by Open Domain Specific Architecture (ODSA)

- 16 lines at 16Gbit/s (double data rate)
- Pitch not specified – typically, 100-130 um pitch
- Definition of electrical interface
- No definition of high level protocols
- Support from Meta, Microchip, Facebook, …



Advantage

Laminate based chiplet technology possible

Disadvantage

Limited scaling – based on laminate substrates

Chiplet Interface Protocols - Universal Chiplet Interconnect Express (UCIe)

Support from: AMD, Arm, ASE, Google, Intel, Meta (Facebook), Microsoft, Qualcomm, Samsung and TSMC

Version 1.0 available

Laminate based

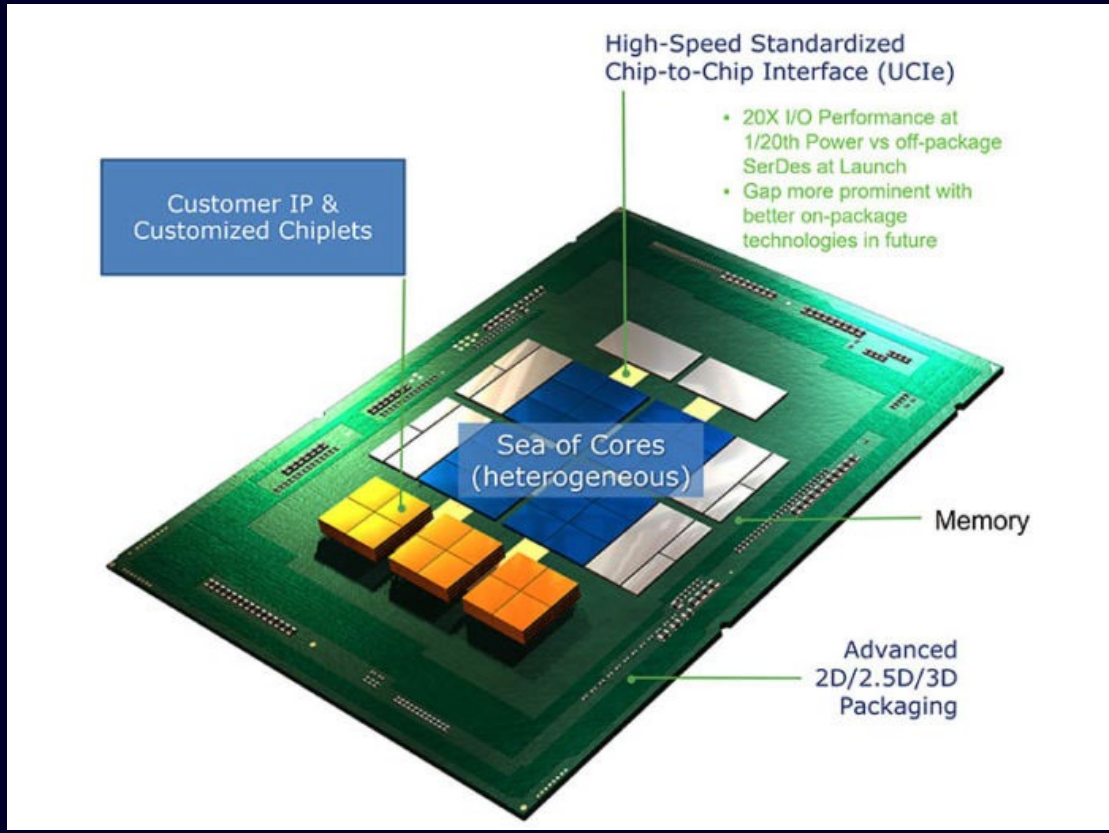
- 16 lines at up to 32Gbit/s (double data rate)
- Typically, 100-130 um pitch

Silicon Interposer based

- 64 lines at up to 32Gbit/s (double data rate)
- Typically, 25-55 um pitch

Definition of electrical interface

- high level protocols – CXl, PCIe



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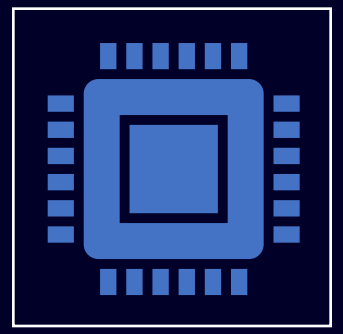
Chiplet Interface Protocols - Universal Chiplet Interconnect Express (UCIe)

Advantage

Laminate and silicon interposer based chiplet support



Disadvantage

2 different sub-standards on package side

Different sub-standards on protocol side

Different implementation of chiplet IP is possible, reducing interoperability

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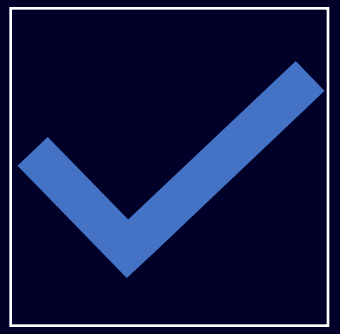
Chiplet Interface Protocols - High bandwith memory (HBM)

Established standard - Version 2.0 available

1024 lines at 2Gbit/s (double data rate)

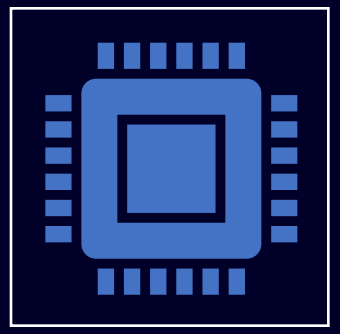
55 um pitch



Advantage

Very high performance

Can also be used as standard for processor-processor communication



Disadvantage

Silicon Interposer technology necessary

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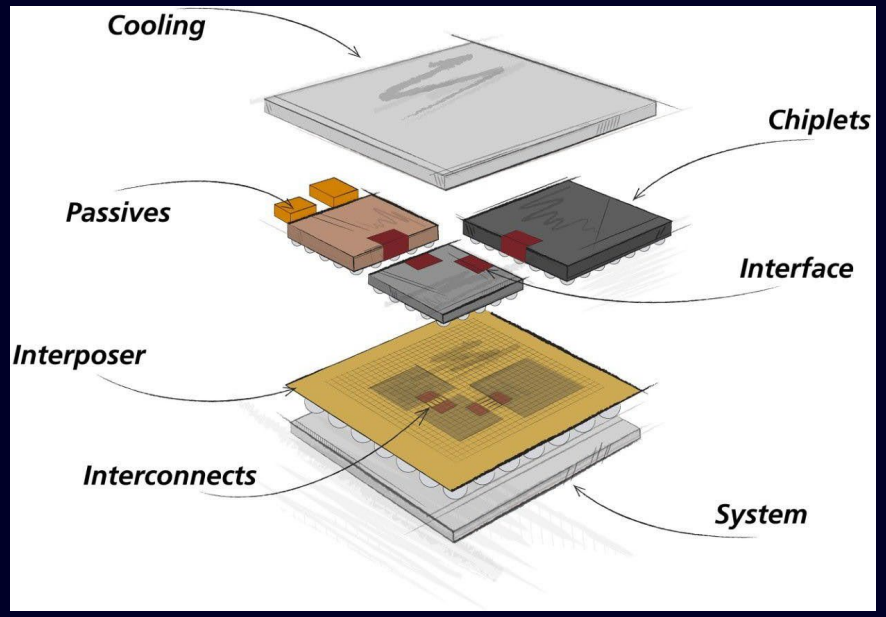
Automotive ECU recommendation

Heterogeneous Integration of different technologies

- Digital – Processor, Accelerators
- Analog
- Memory

Number of devices/chiplets depends on:

- Configurability/Adaptability – disaggregate multi processor logic into homogeneous modules
- Configurability/Adaptability – separate accelerators



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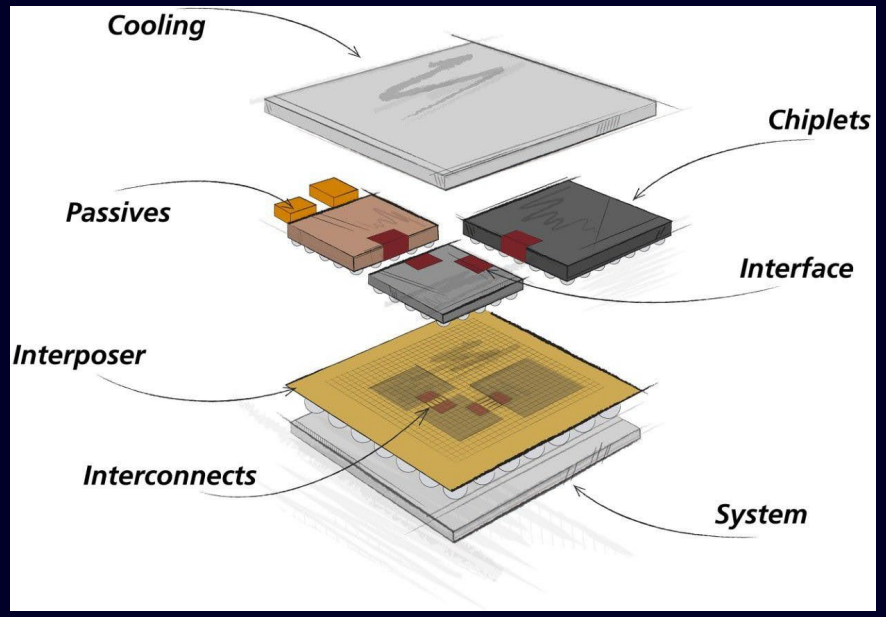
Automotive ECU recommendation

Analog – Digital device interface

- E.g., Analog-digital-converter, Digital-analog-converter
- Reduced data-rate necessary (small number of interconnects)

BoW interface is a good fit



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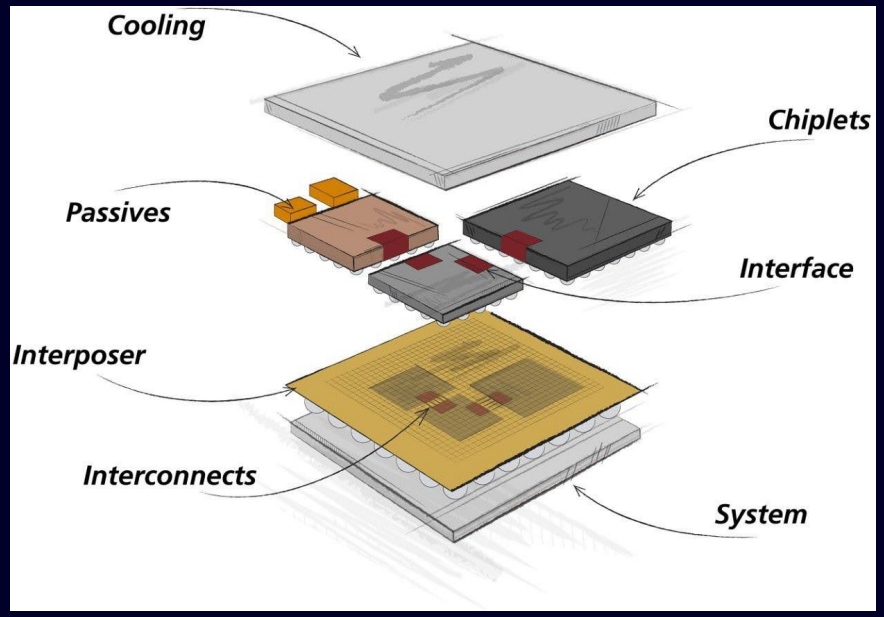
Automotive ECU recommendation

Digital – Digital device interface:

- E.g. processor cluster, accelerator
- electrical protocol definition and protocol layer definition necessary
- High or very high data-rate necessary (high number of interconnects)

UCIe interface is a good fit



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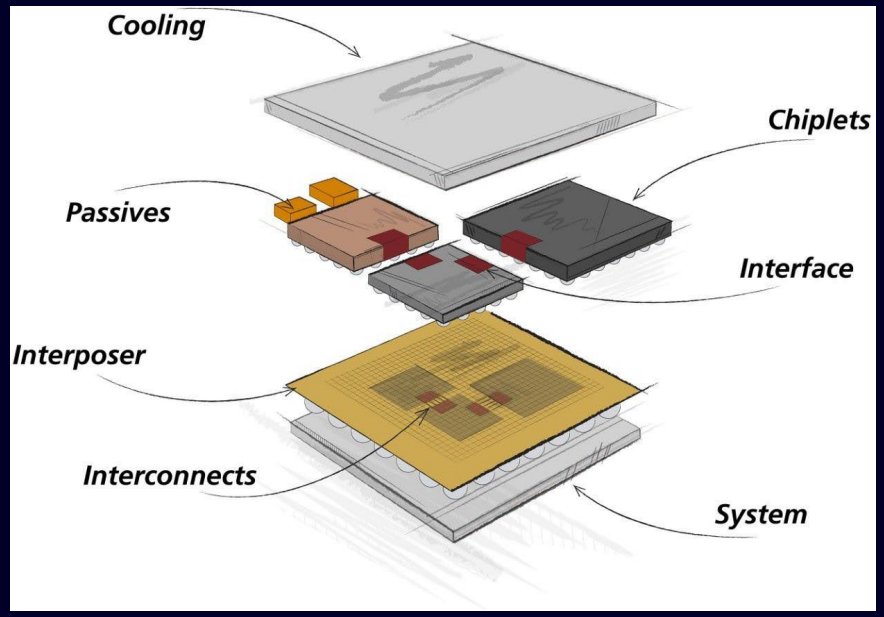
Automotive ECU recommendation

Digital – Memory device interface:

- High or very high data-rate necessary (high number of interconnects)
- HBM interface recommended



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Automotive ECU Summary

Chiplet based heterogeneous integration offers a superior path to monolithic SoC

Currently no single interface fits all needs

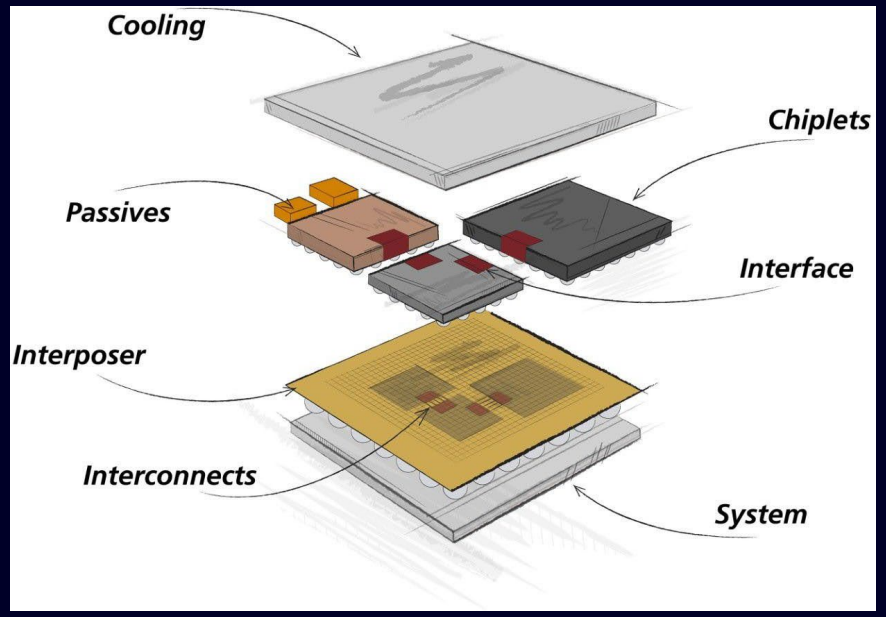
- Multi protocols necessary
- Reduces interoperability

HBM and partially UCIe requires a silicon interposer

- Cost
- Reliability

BoW + UCIe (version for laminates) can be utilized with an organic interposer

- However HBM cannot be used unless with a silicon bridge



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