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DFT Architecture for chiplet based heterogeneous ICs and Systems In Package

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Outline

- DFT (Design for Test)
  - Economics of Test: Quality and Cost

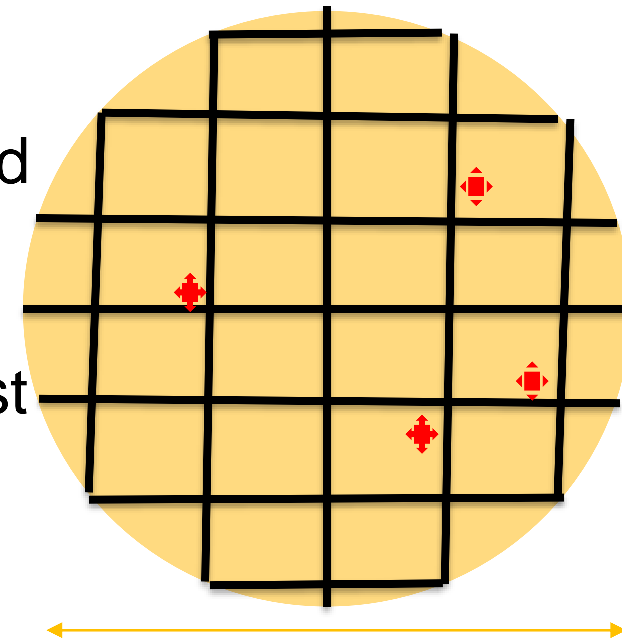
- Heterogeneous ICs and Systems-In-Package
  - Current Trends in System Integration: Chiplets
  - 3D IC Test Problem

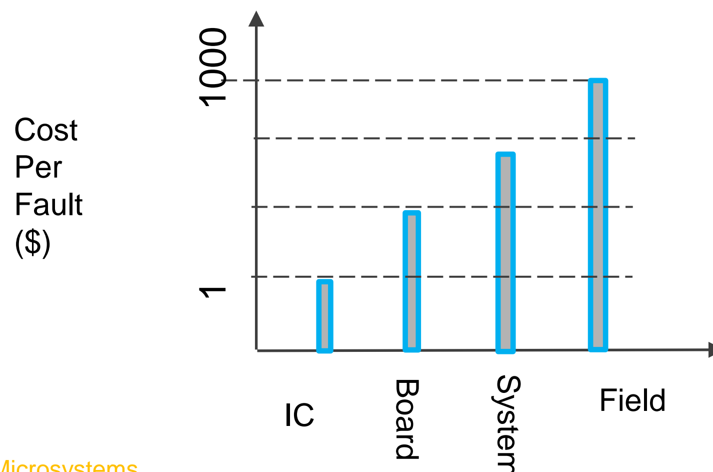
- Proposed Architecture
  - Test Technology Standards from IEEE (Institute of Electrical and Electronics Engineers)
  - Hierarchical Control for System DFT
  - Interconnect Test Illustrated

- Conclusion

Economics of Integrated Circuit Test

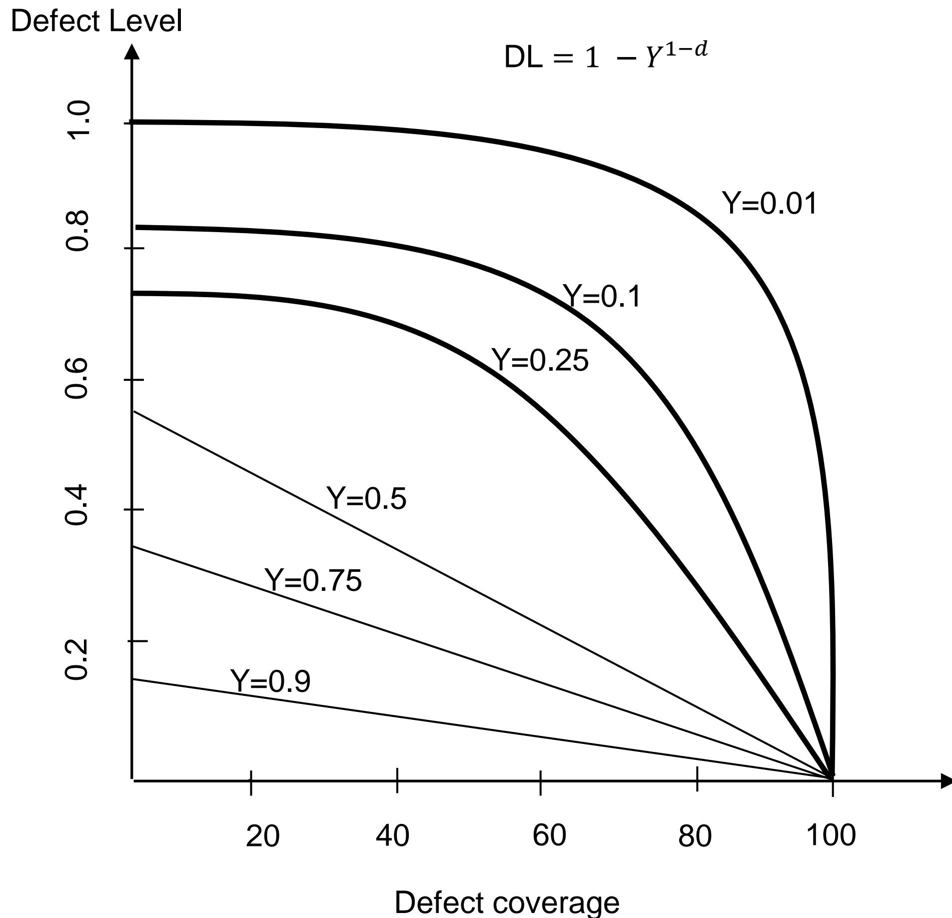
- Yield: A major economic driver for Electronic Device Manufacturers (EDM)
- Silicon Manufacturing is prone to process related defects
- Defect – Faults – Errors
- Wafer & Die Level Test
  - Known Good Die (KGD) is Key for Highest Yield
- 16/20 = 80% Yield from this Wafer
  - Dissecting each Chip into multiple sub core increase Yield at cost of increased packaging cost





Reference: Sun Microsystems

Yield, Defect Level and Defect Coverage



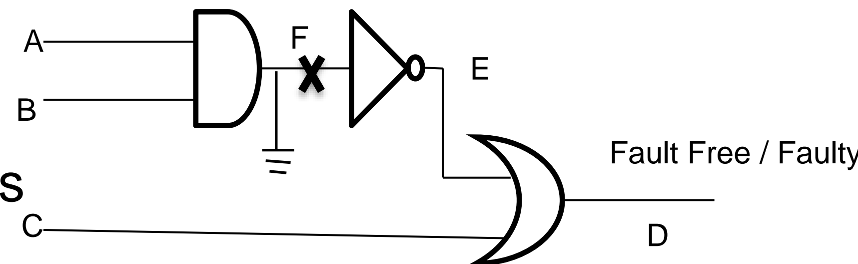
Reference: Williams and Brown TC 1981
Reference: ITC 2000 Tutorial

DL = Defect Level = Prob of shipping a defective product
This is Escape rate
Y = Yield = Prob of manufacturing a defect-free product
d = defect coverage = Prob that applied test detects defect
This determines test quality

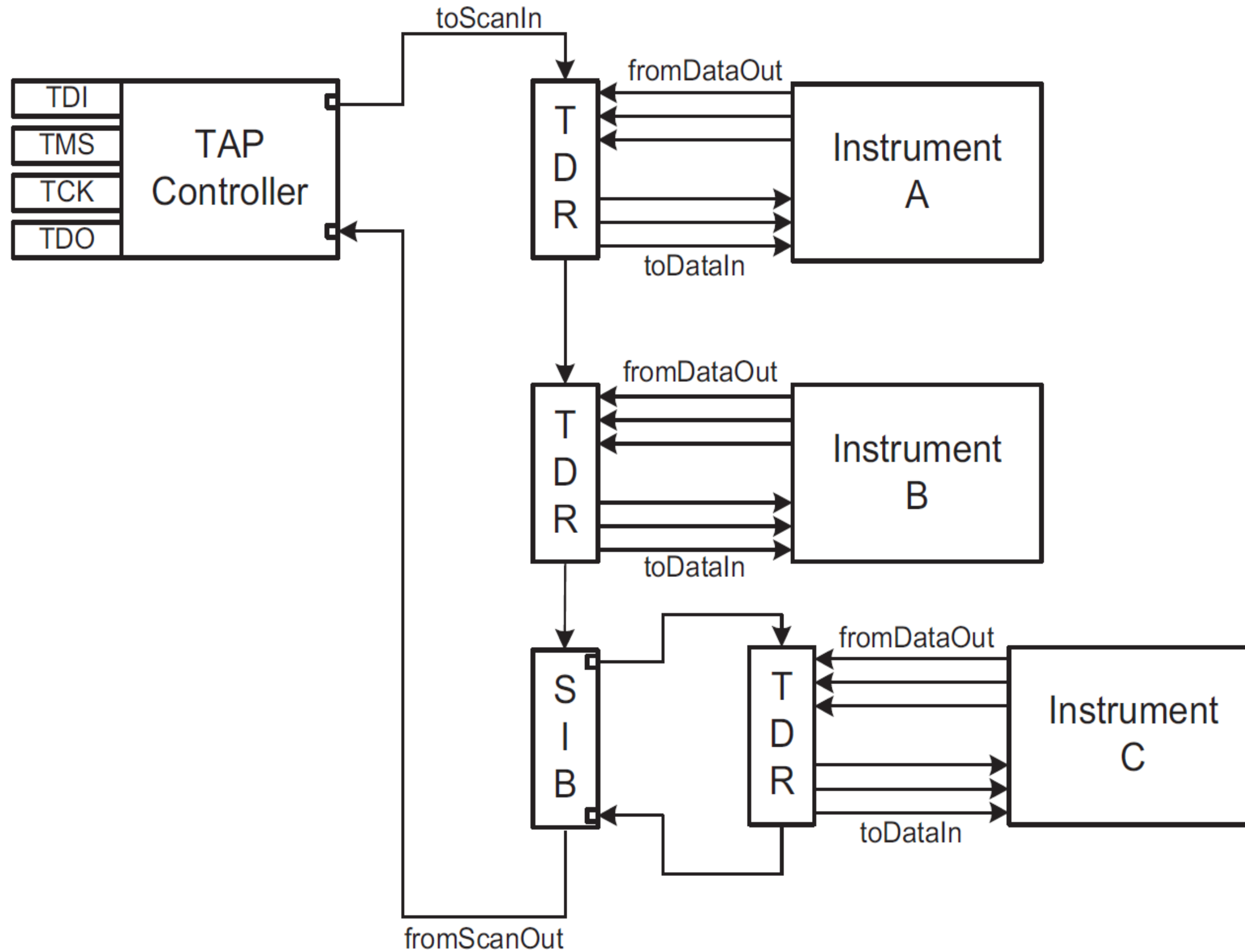
- Transistor size scaling down per process node
- Decreasing feature size increases probability of defects during manufacturing process
- Need Quality Tests to increase defect coverage
- Need Cost effectvie Test since 40% of the IC costs are attributed to Test

DFT Design for Testability

- Structured Design Techniques to enhance Testability:
  - Focus on Structural, Defect oriented test over Functional Test
  - Controllability and Observability
- Most Widely Used DFT Techniques
  - Automatic Test Pattern Generation (ATPG) based on Scan Storage Elements
  - Built In Self Test (BIST) for Memory and Logic Structures
- Test Access Port (TAP) (IEEE 1149.1)
  - Boundary Scan for Board Interconnect Test between Dies/ICs
  - Standardized 4 pins TCK, TDI, TDO, TMS
  - Allows Hierarchical Access
- IEEE 1687 iJTAG
  - Boundary Scan for Board Interconnect Test between Dies/ICs
  - Standardized 4 pins TCK, TDI, TDO, TMS
  - Allows Hierarchical Access
- Core Level Test Standard (IEEE 1500)
  - Specifies DFT Guidelines for Reusable IP Cores
  - Reduces Pattern Generation Time for SoC
  - Seamless Integration with IEEE 1149.1

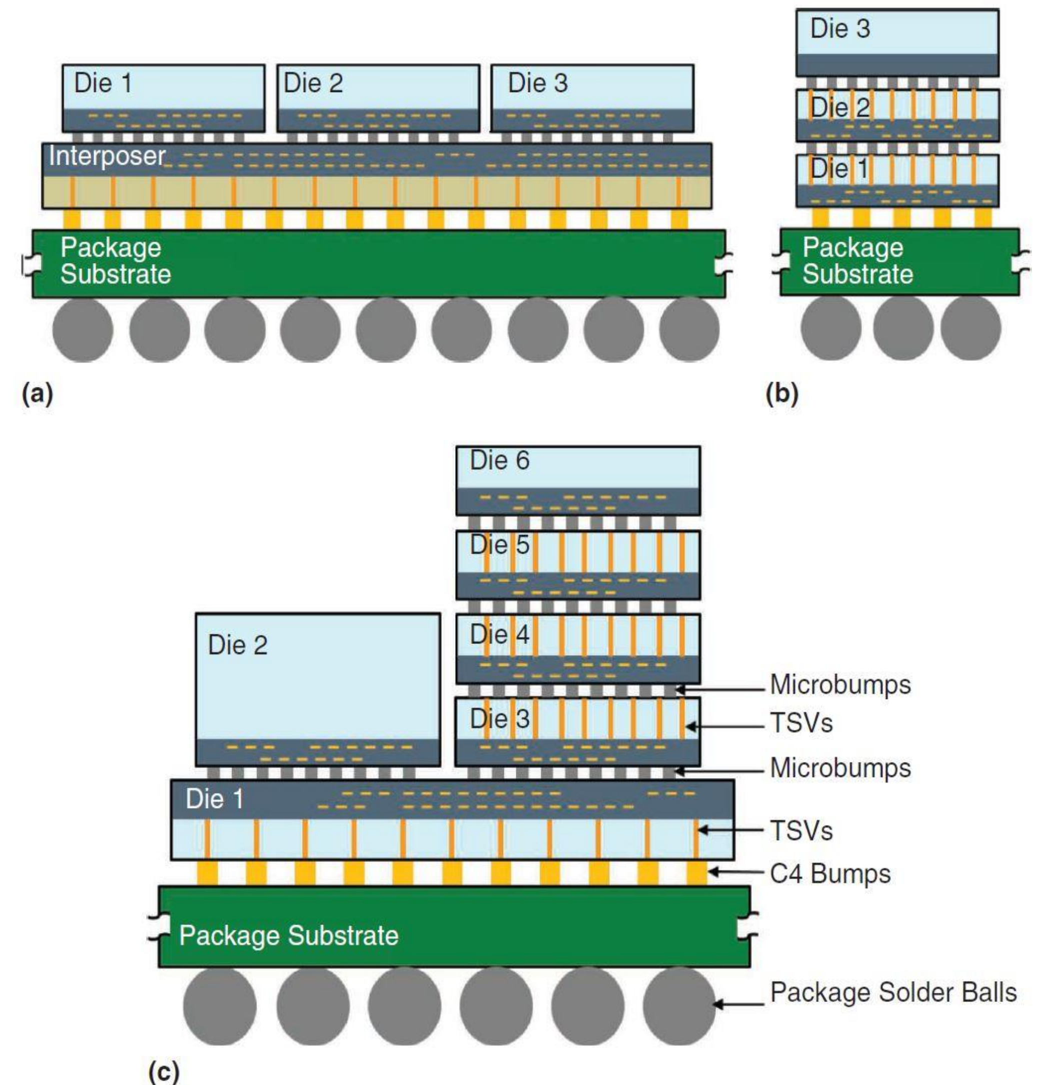


Embedded Instruments Test Access: IEEE 1687



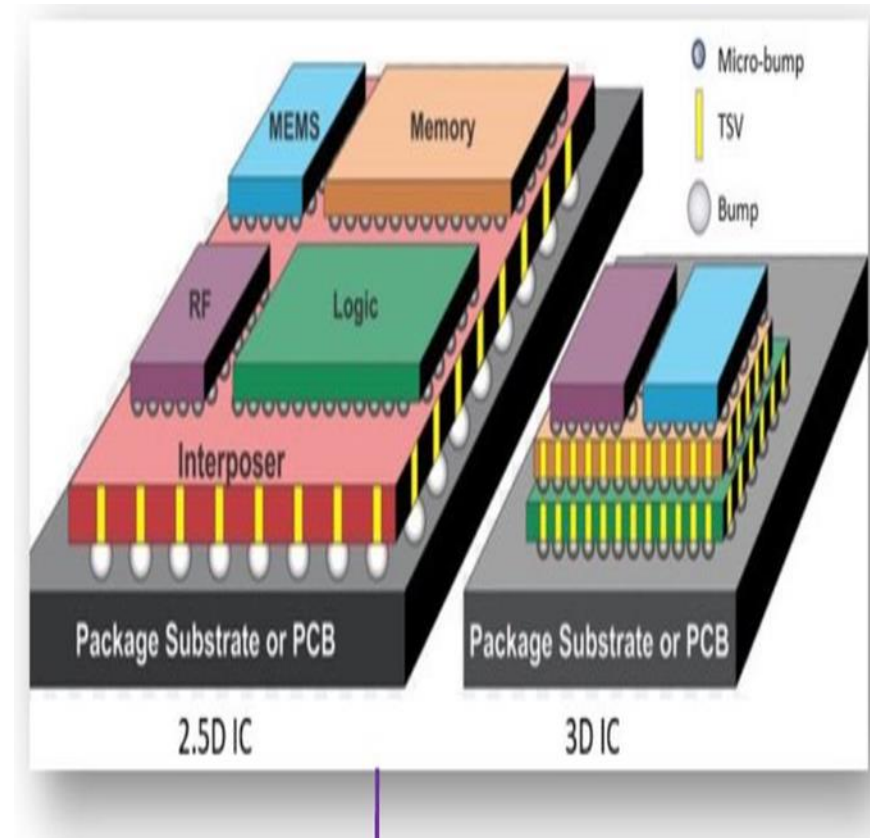
Current Trend: System Integration with chiplets

- Moore Law and associate scaling is becoming a challenge.
- Computational Requirements exploding due to AI / ML applications, ADAS, Augmented and Virtual Reality applications, Cloud as well as Edge Computing
- Monolithic System on Chips is reaching reticule limits of Silicon Manufacturing
- Heterogenous Integration with Stacked Chips/Chiplets: Advantages
  - Integration of known good dies from various mature process technologies i single package
  - Higher Bandwidth: input/output loads between dies are minimal
  - Stacking saves power and space



3D Stacked IC Test challenges

- DFT Architecture needs to be planned carefully bottom up.
- Test Standards have typically focussed in Board Level Testability (IEEE 1149.1)
  - Scan Vectors using Automatic Test Pattern Generation
  - Built In Self Test (BIST) for Memory and Logic Structures
  - Importance of Known Good Die (KGD)
- Package Level DFT
  - Integration of known dies implementing varying DFT Techniques: Memory Die interfacing with Logic Die
  - Pre and Post package Test for Large and dense arrays of inter-die interconnects vertical Interconnections using through-silicon vias (TSV)
  - Test Pattern Reuse from Constituent Chiplets
  - IO Bandwidth, Costly Repair
- System Level DFT



Reference: Tessolve Semiconductor

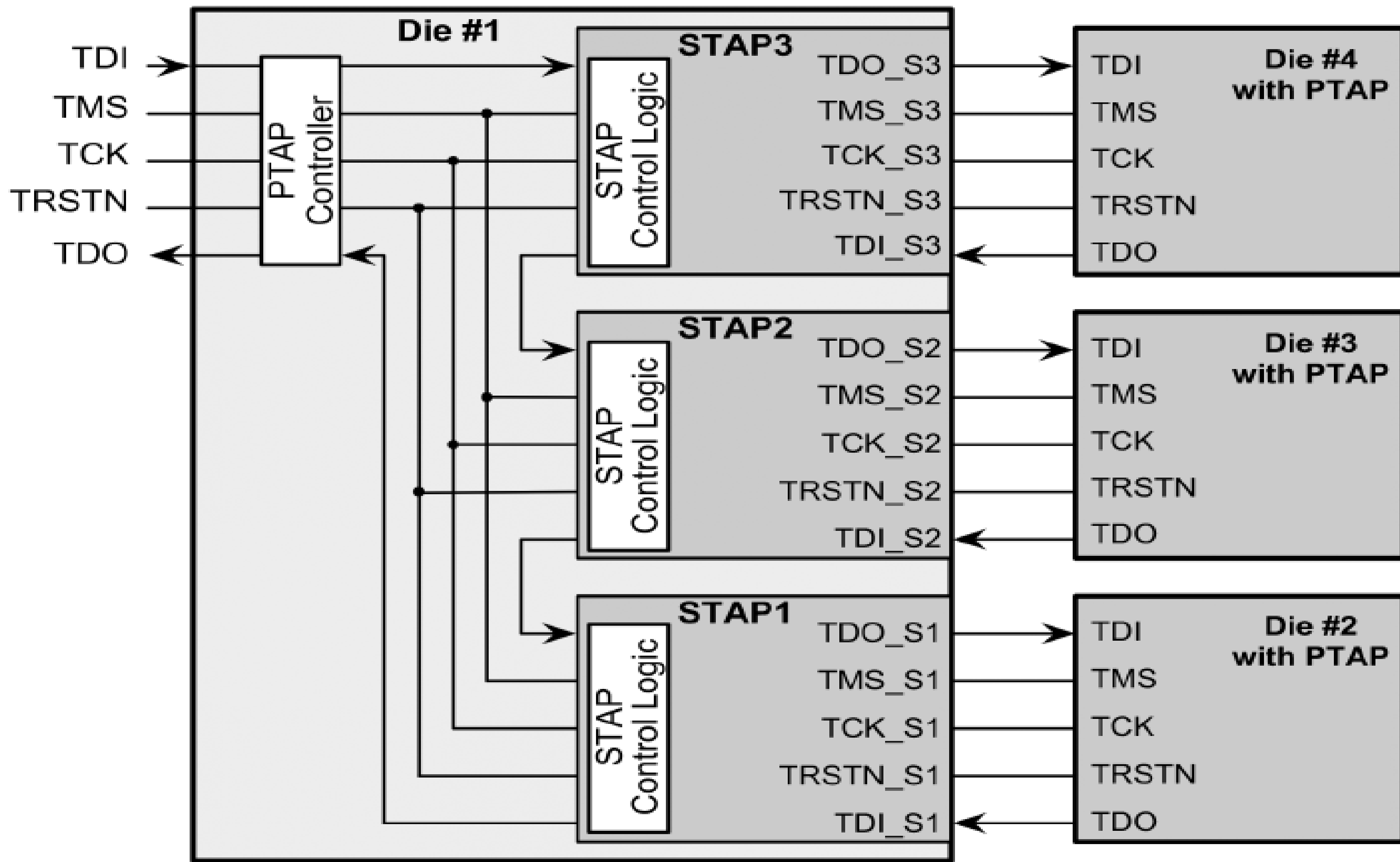
3D Stacked ICs Test Access: IEEE 1838

- Specifies DFT Guidelines in Dies integrated as modules in 3D multi-die, single package systems

- Allows transporting test collaterals
  - Transport test stimuli from 3D Stack's external interface up to a die or inter-die interconnect
  - Transport the corresponding test response back down

- Handles many packaging topologies
- DFT Architecture needs to be planned carefully bottom up.

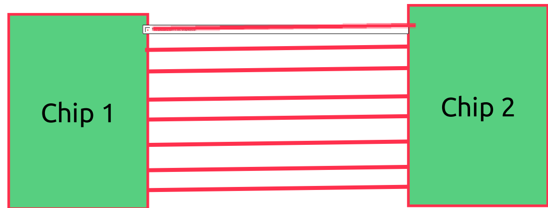
3D Stacked ICs Test Access: IEEE 1838



Hierarchical DFT architecture

- Strategy based on All 4 IEEE Test Standards (1149.1, 1500, 1687 and 1838)
- Hierarchical Control for enables DFT at each integration level
- Implementing DFT compliant with standards at Chiplet levels guarantee that once Chiplets are integrated , a System Level test access architecture emerges
- Careful Design of SiP level Test Controller is mandated.
- Test Parallelization is key. Intelligent test schedule to meet power budget is a design challenge for Test Controller
- System DFT needs Top-Down Architecture and Bottom-Up Implementation

D2D Interconnect Testing In 2.5D SiP



Up Counting Sequence	Down Counting Sequence
0 0 0	1 1 1
0 0 1	1 1 0
0 1 0	1 0 1
0 1 1	1 0 0
1 0 0	0 1 1
1 0 1	0 1 0
1 1 0	0 0 1
1 1 1	0 0 0

Die 1
Die 2
Die 3
TAP
TAP
TAP
Interposer
TSV
TDI
TDO

TAP: Test Access Port (1149.1)

Boundary Scan Cell

Pattern Count = 2 * lg (N)
for N Interconnects

Conclusion

- Chiplet Based SiP and 3D Stack ICs need careful architectural design plan for DFT
- IEEE Testability Standards like 1838 play a key role in enabling hierarchical design features to achieve a goal of Package Level DFT for 3D Stacked ICs using most prominent test standards IEEE 1149.1, IEEE 1500 & IEEE 1687
- This approach enables successful reuse of die level tests well as inter-die interconnects test to guarantee highest quality product at lower cost