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# Using Predictive SI Analysis to Ensure Successful Chiplet Integration

Subramanian Lalgudi, Siemens EDA

John Caka, Siemens EDA

Jawad Nasrullah, Palo Alto Electron, Inc.

# Importance of Signal Integrity for Chiplet Integration (1/2)

**WHAT IS STANDING IN THE WAY?**


Monolithic processors include decades of chip design to optimize:

- Intrachip communication with optimized timing and reduced latency
- Thermal characteristics
- Power efficiency
- **Signal Integrity**
- Application-specific behaviors

These optimizations can be incompatible with a chiplet-based strategy as new characteristics such as routing may have to be redesigned.

Proprietary solutions suppliers must see the value in collaborating to increase profit by increasing the market size and associated opportunities for revenue streams.

Like all new technologies that benefit from standardization, there is frequently a battle for competing standards. When competing standards become incompatible and fight for market share, advancement tends to be slower and hard earned.

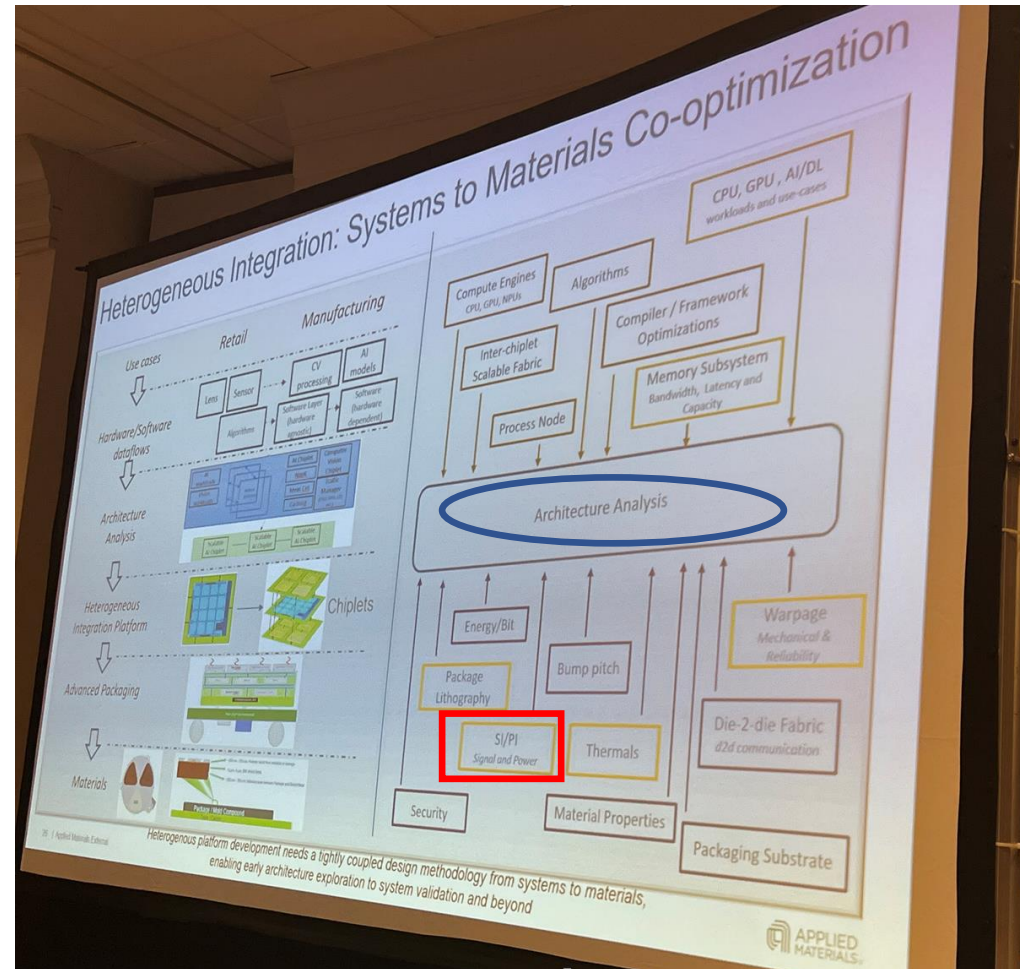


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Chiplet Market Update | Chiplet Summit Presentation | [www.yolegroup.com](http://www.yolegroup.com) | ©2022 | 25

Courtesy: Yole Keynote, Chiplet Summit 2023

# Importance of Signal Integrity for Chiplet Integration (2/2)

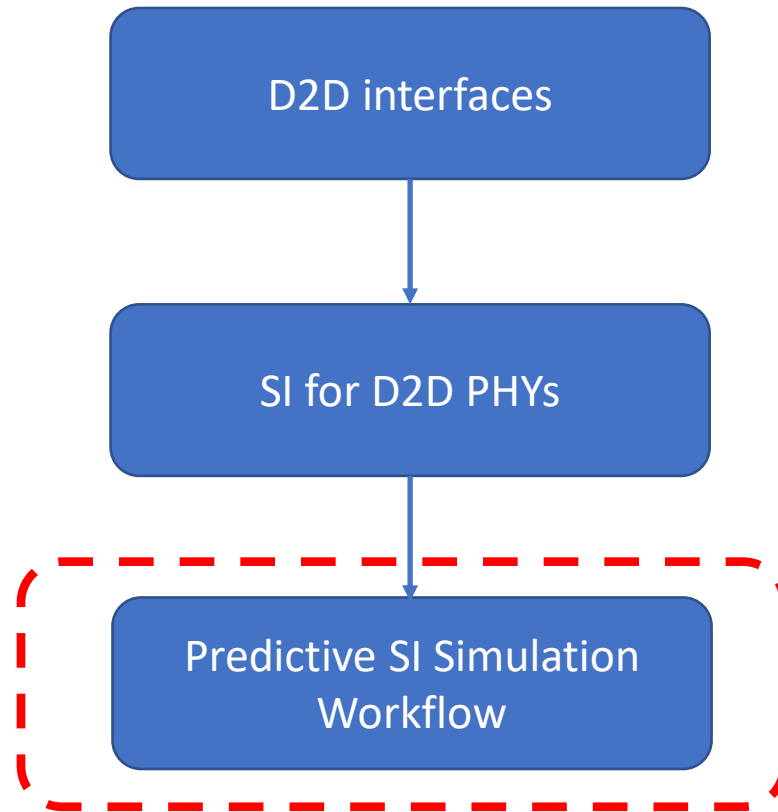


Courtesy: Applied Materials Keynote, Chiplet Summit 2023

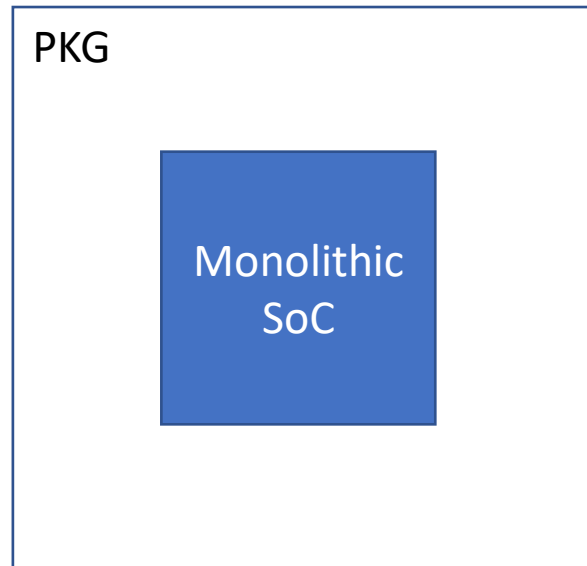
# What is Predictive SI Analysis?

$$\text{Predictive SI Analysis} = \text{Traditional SI analysis} + \text{D2D Interconnects} + \text{Architectural Analysis Stage}$$

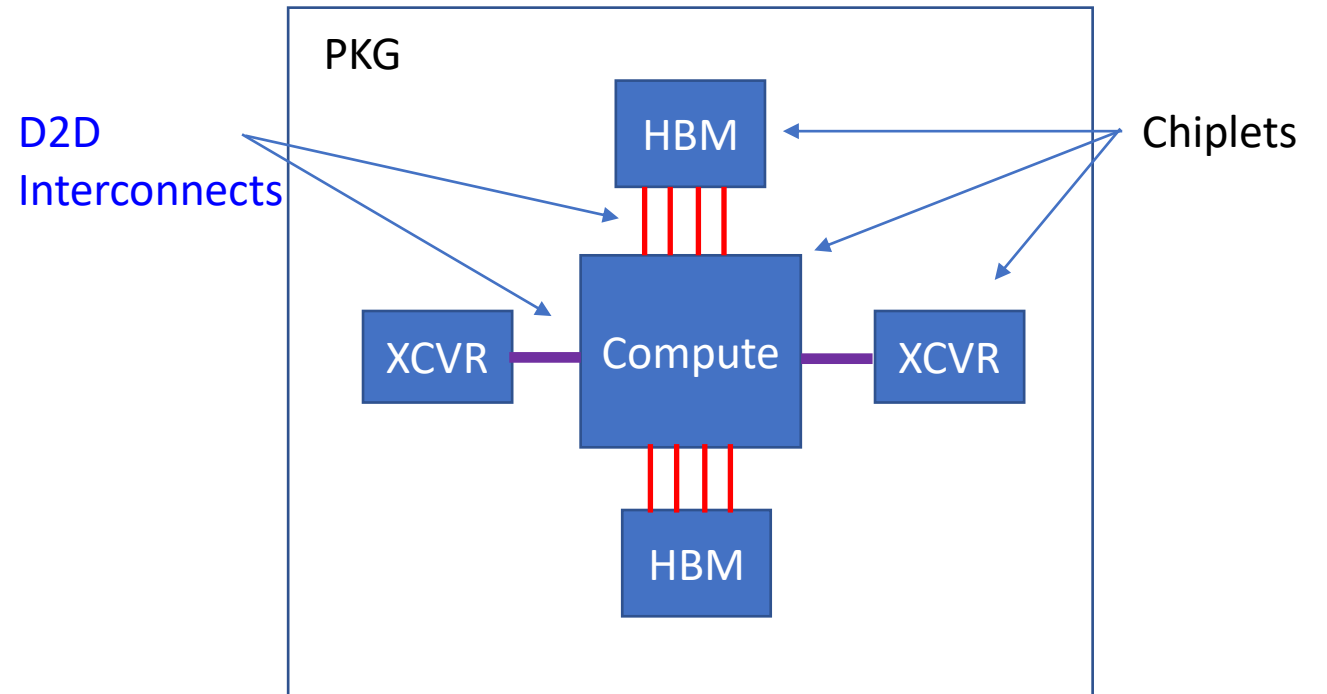
# Outline



# What are Die-to-Die Interconnects?

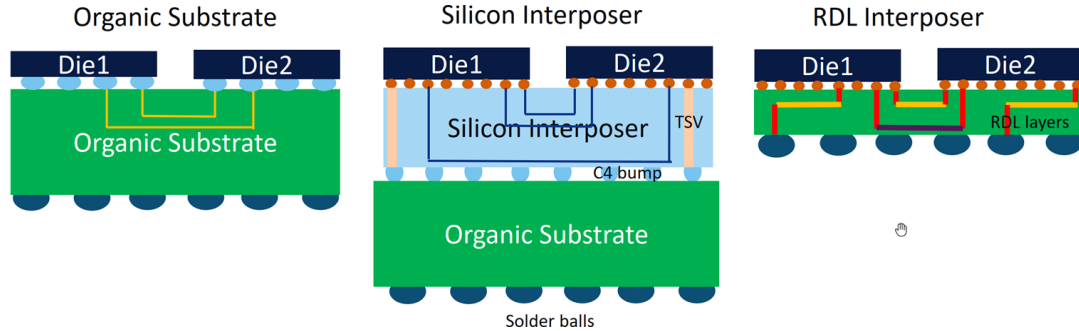


Top-level view of a monolithic SoC



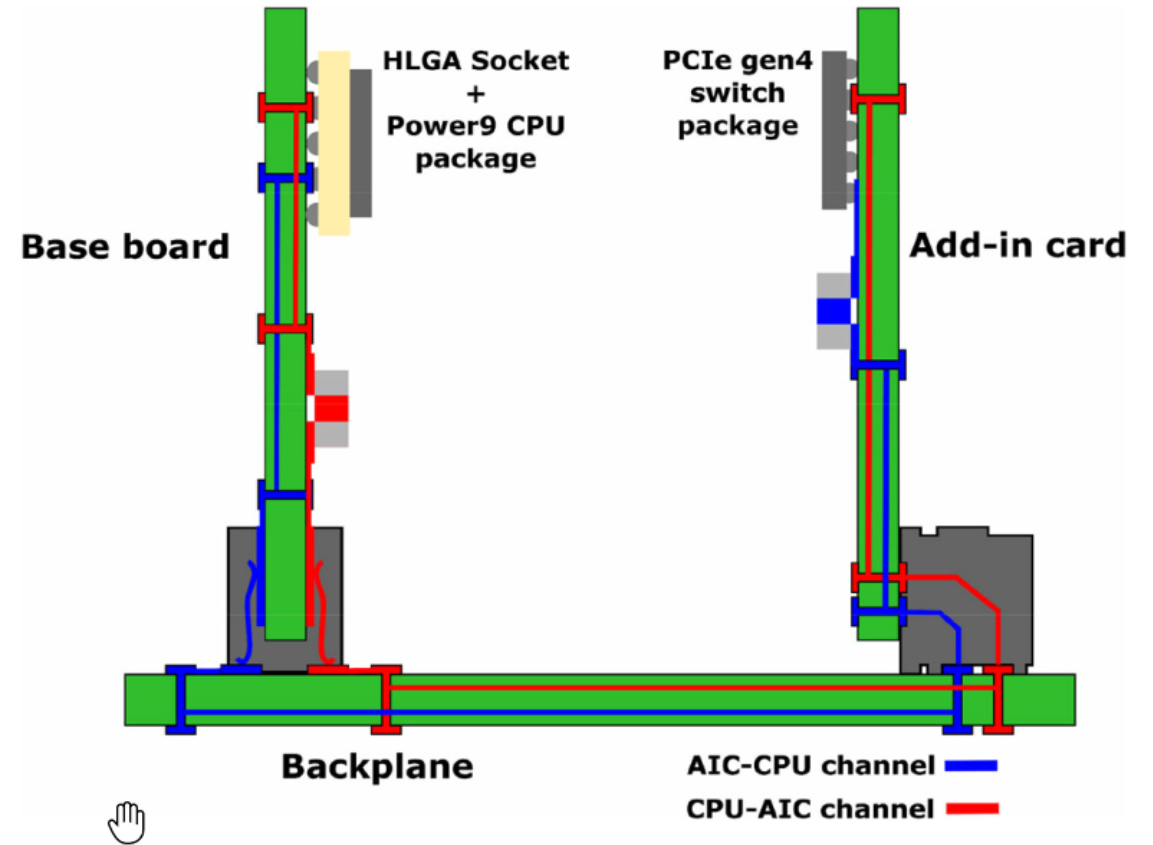
Top-level view of a chiplet-based System

# They are Different from Traditional Chip-to-Chip Interconnects (1/2)



A couple of D2D Interconnect configurations

[A. Ramamurthy, Chiplet Technology and, Heterogeneous Integration, June 2021](#)



Topology of a PCIe link\*  
(traditional chip-to-chip interconnects)

\*E. Orekhov et al, "Signal Integrity Analysis and Peripheral Component Interconnect Express Backplane Link Compliance Assessment," Engineering Reports, Feb. 2022

# They are Different from Traditional Chip-to-Chip Interconnects (2/2)

## **D2D Interconnects**

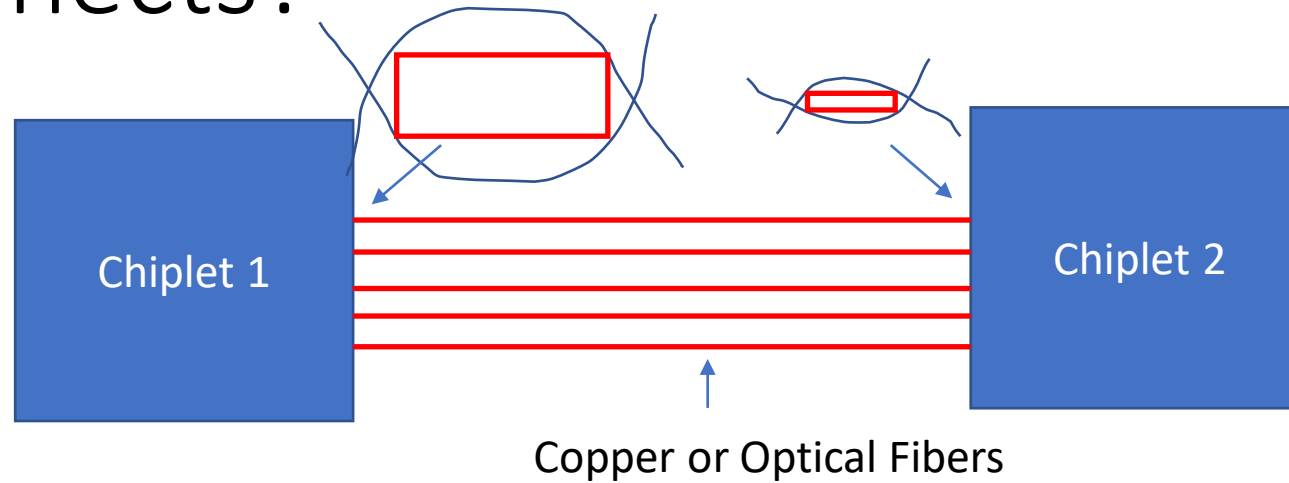
- Lie inside package
- Both org. & Si interposers/bridges
- Mostly stripline
- Shorter in reach (2-50 mm)
- Mostly parallel
- Terminated or Unterminated
- Examples:
  - Parallel: UCIe, BoW, AIB, OpenHBI
  - Serial: XSR

## **Traditional chip-to-chip Interconnects**

- Go outside the package
- Mostly organic substrates
- Mostly microstrip
- Longer in reach
- Both parallel and serial
- Usually terminated
- Examples:
  - Parallel: DDRx, PCIe
  - Serial: USB, HDMI



# Why Signal Integrity (SI) for D2D Interconnects?



D2D Interconnects degrade signal transmitted, leading to logic failure

Quantity	Signal Integrity Effects
Lossy lines	Intersymbol interference
Densely-spaced Parallel Lines	Crosstalk
Termination	Data rate
Transmit and Receiver Jitter	Reduced Eye margin

# SI Analysis: Predictive Vs. Post-Layout

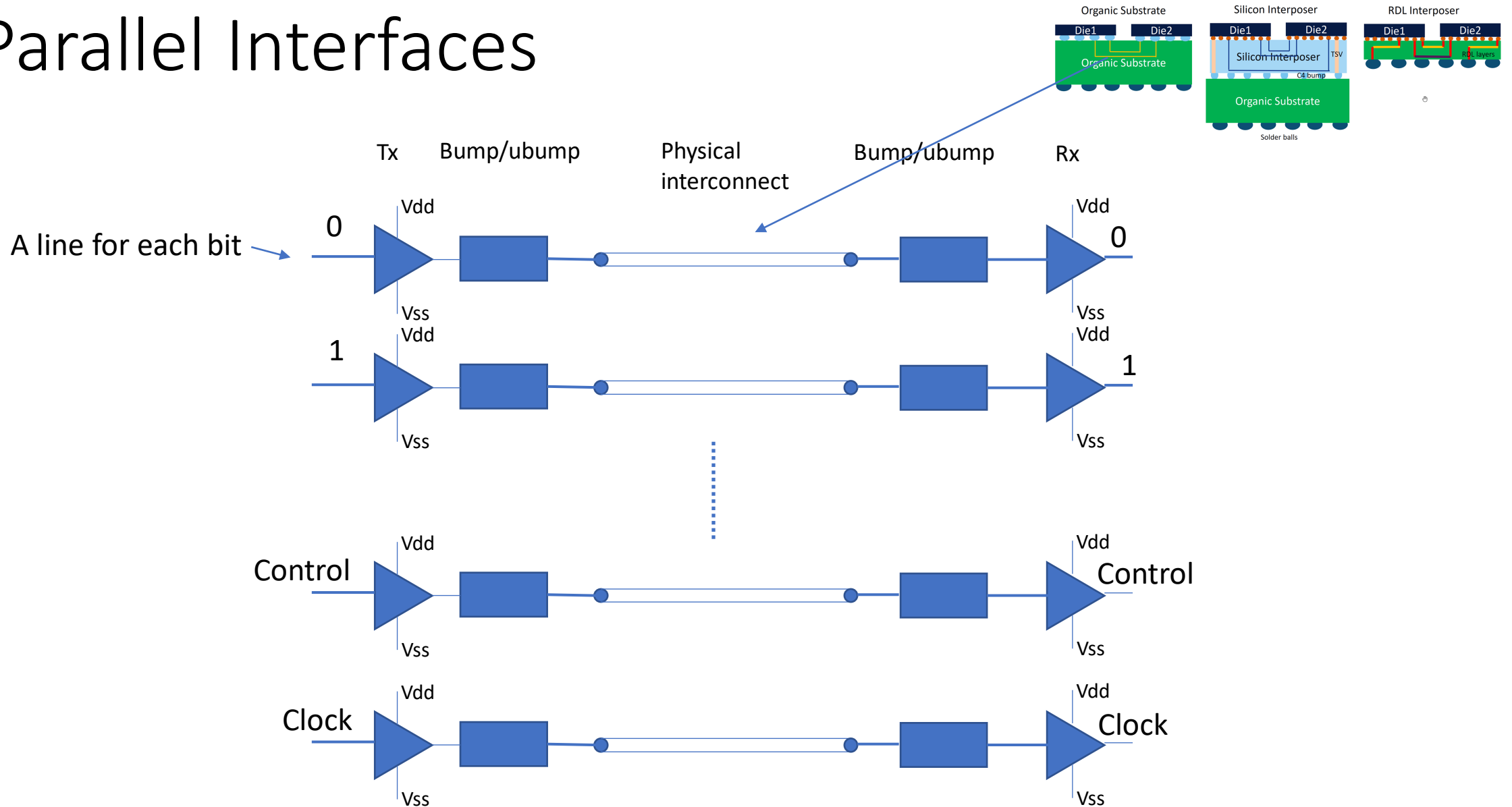
## **Predictive**

- Done for planning
  - Limited info. or only estimates available
- Decide packaging architecture
- Decide interconnect type
- Decide Protocol
- Design space exploration

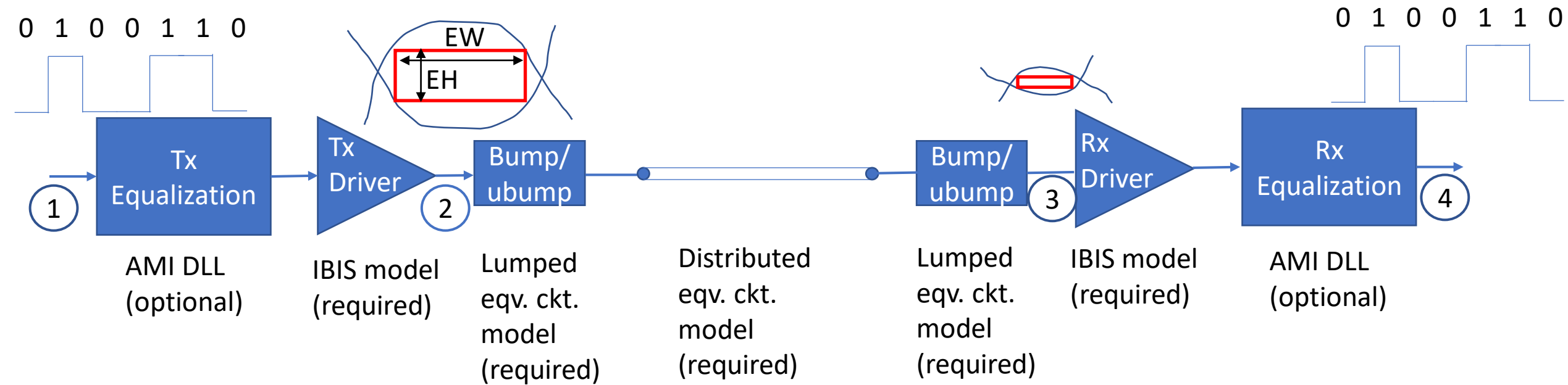
## **Post-Layout**

- Done for sign off
  - Full information available
- Very limited choices

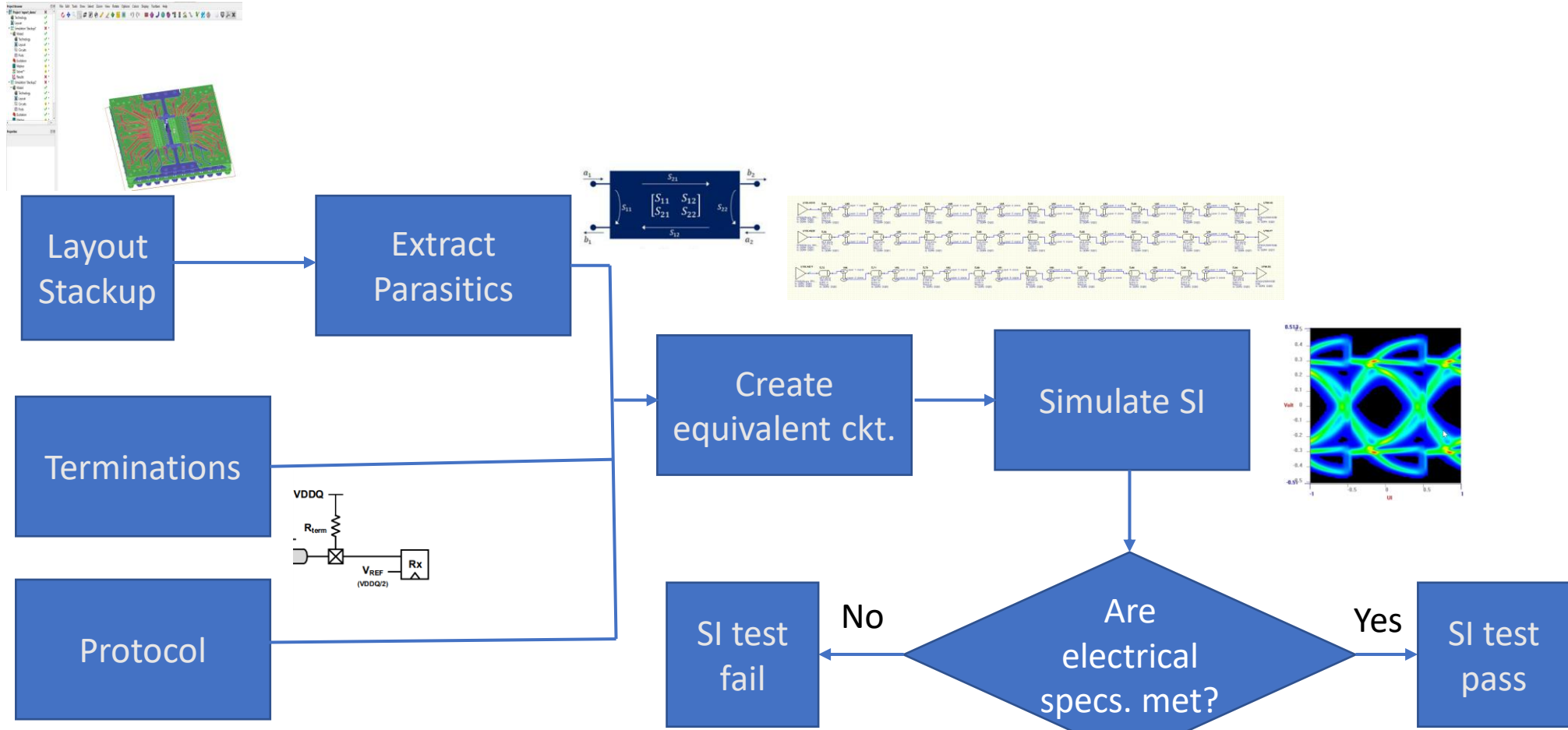
# Predictive SI Simulation Set up for Parallel Interfaces



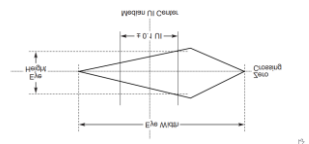
# Predictive SI Simulation Set up for Serial Interfaces



# Post-Layout SI Simulation Workflow

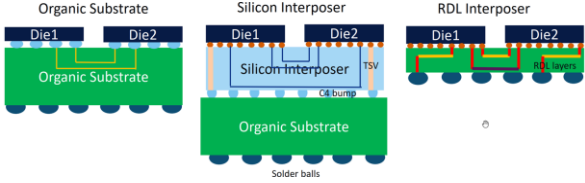


e.g., USB, PCIe, HDMI, DDR



# Predictive SI Simulation Workflow

D2D interconnect geometry  
Stackup  
Constraints

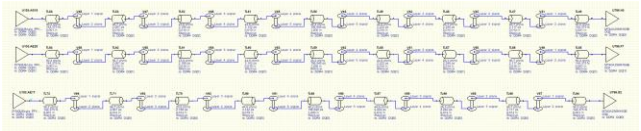
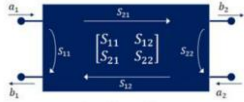


Terminations

Create variations

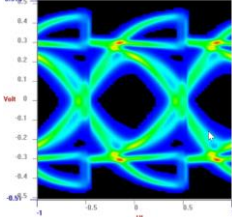


Extract Parasitics



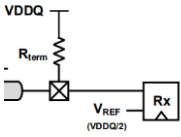
Create equivalent ckt.

Simulate SI



Protocol

Ex: UCIe, BoW, XSR

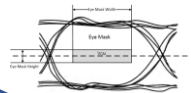


Identify config. w/ best SI

SI test fail

Are electrical specs. met?

SI test pass



# Conclusions

- D2D Interfaces require SI compliance testing.
- SI analysis for D2D interfaces similar to that for traditional chip-to-chip interfaces.
- Predictive SI analysis needed for D2D interfaces given the limited information known.
- Predictive SI analysis workflow for D2D interfaces adapted from the existing workflow for traditional chip-to-chip interfaces.
  - Key change is the design space exploration