Using Predictive SI Analysis to Ensure Successful Chiplet Integration

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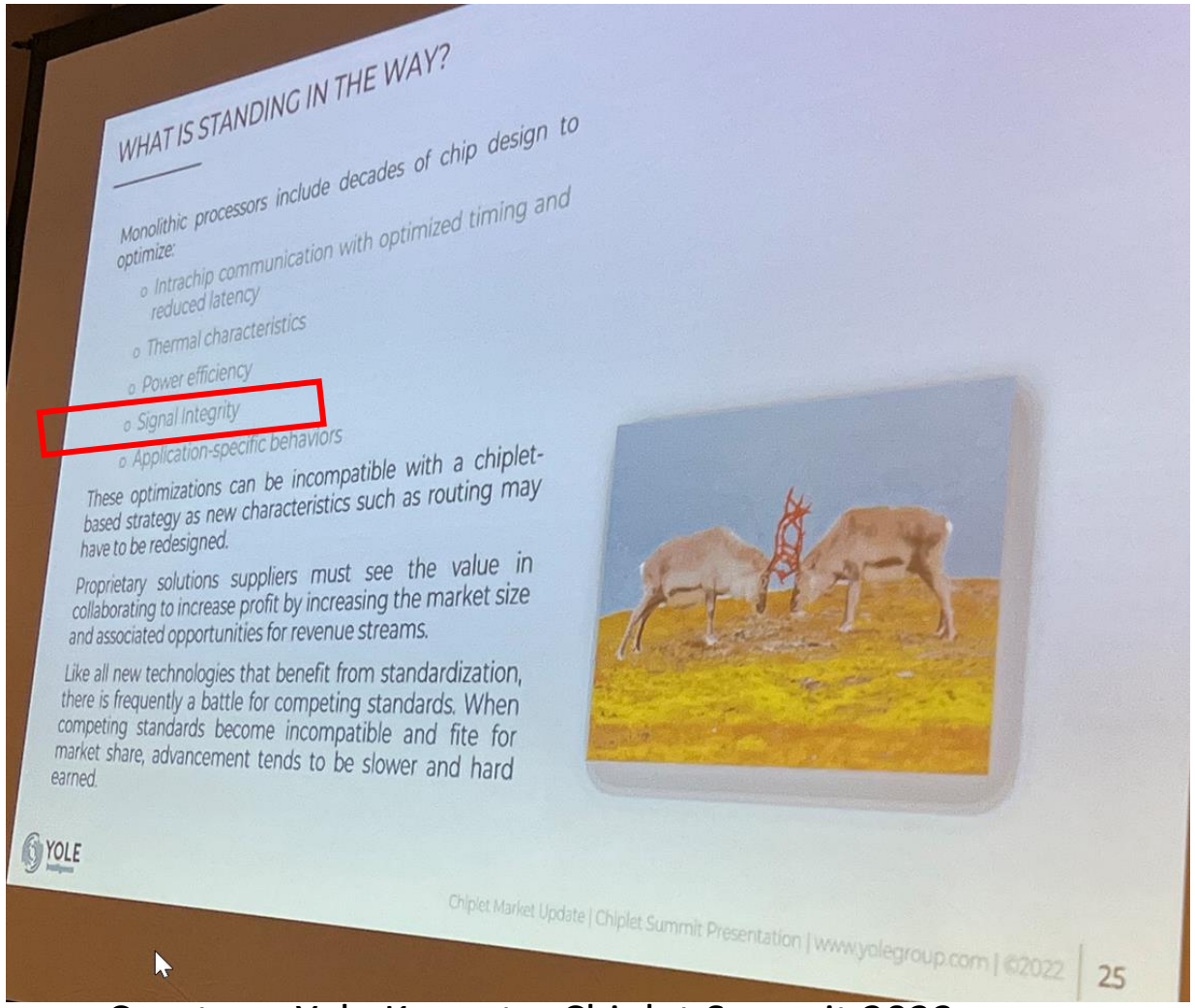
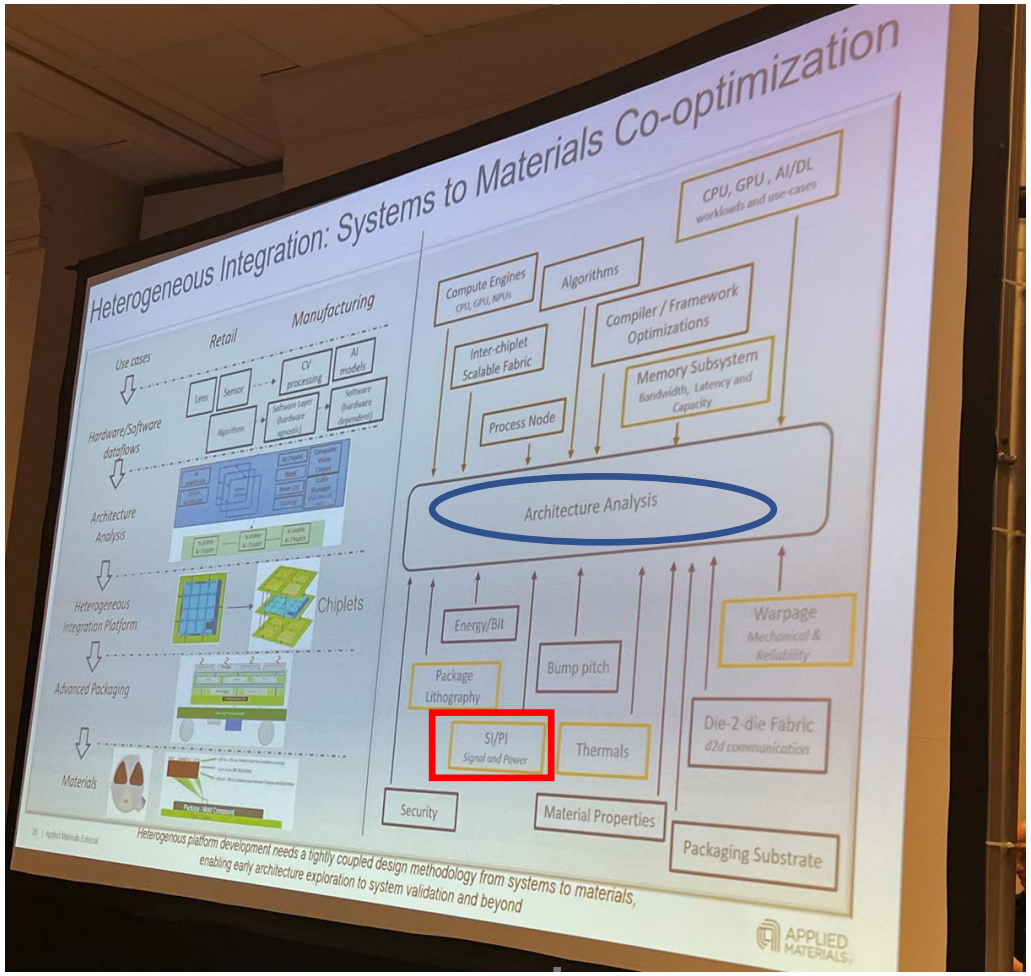
Importance of Signal Integrity for Chiplet Integration (1/2)



Courtesy: Yole Keynote, Chiplet Summit 2023

Importance of Signal Integrity for Chiplet Integration (2/2)

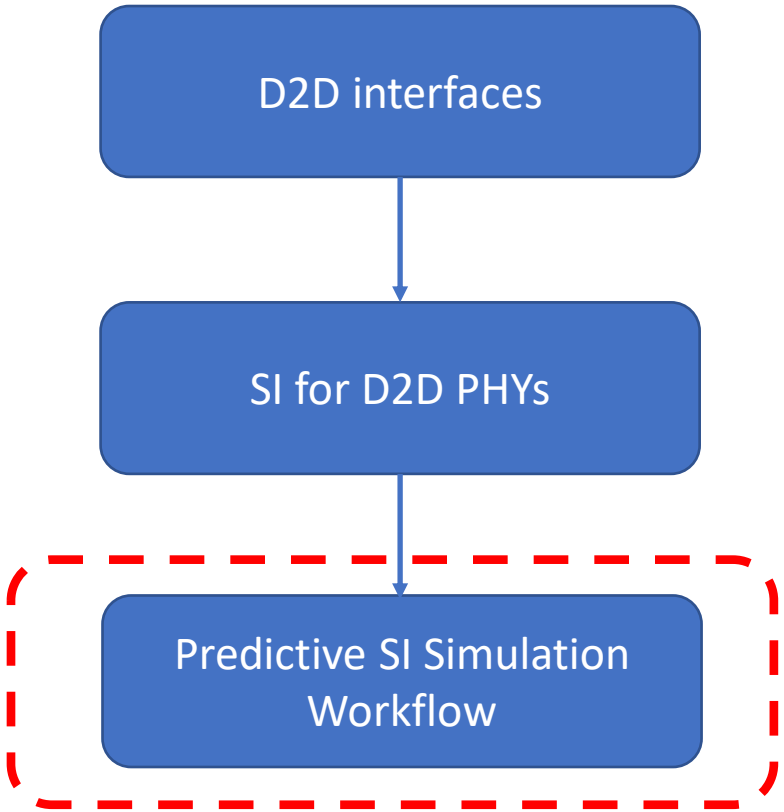


Courtesy: Applied Materials Keynote, Chiplet Summit 2023

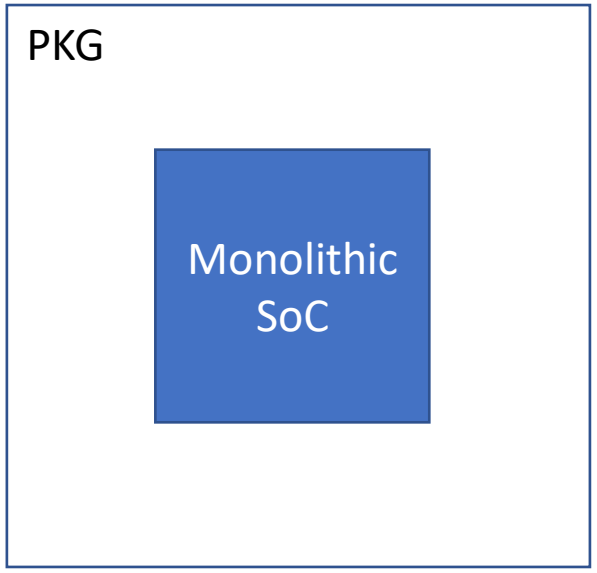
What is Predictive SI Analysis?

Predictive SI Analysis = Traditional SI analysis + D2D Interconnects + Architectural Analysis Stage

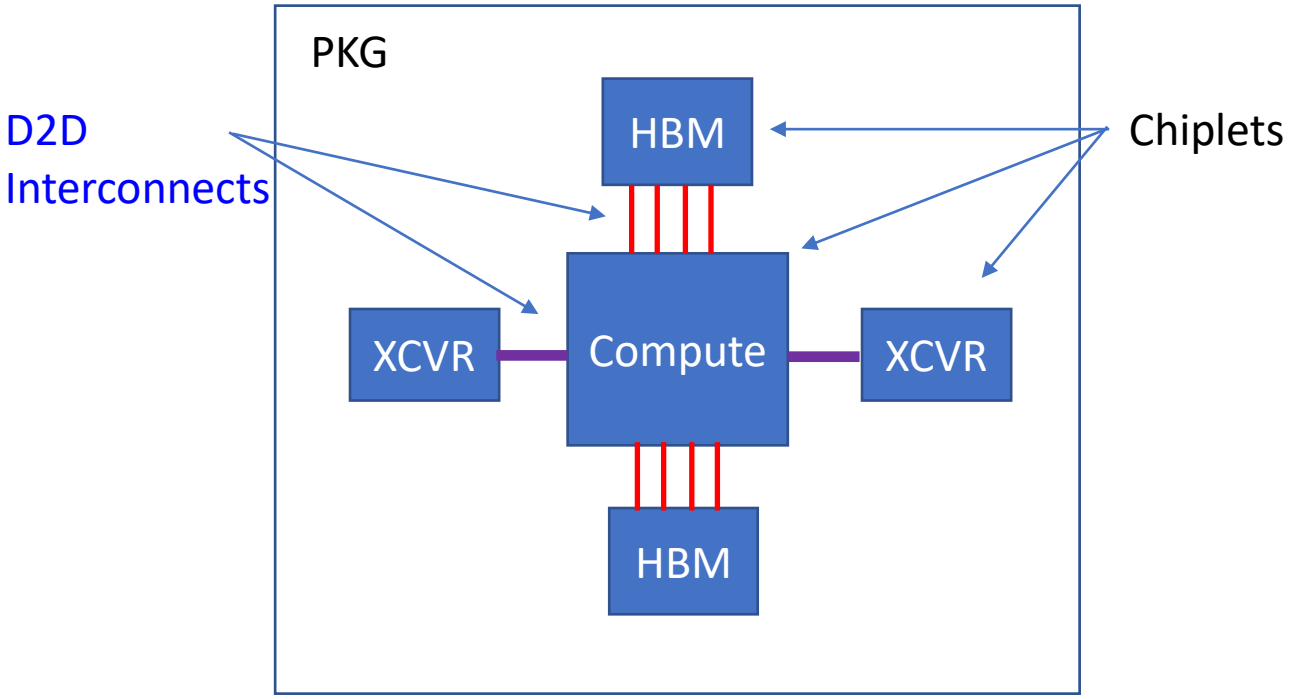
Outline


D2D interfaces
SI for D2D PHYs
Predictive SI Simulation Workflow

What are Die-to-Die Interconnects?

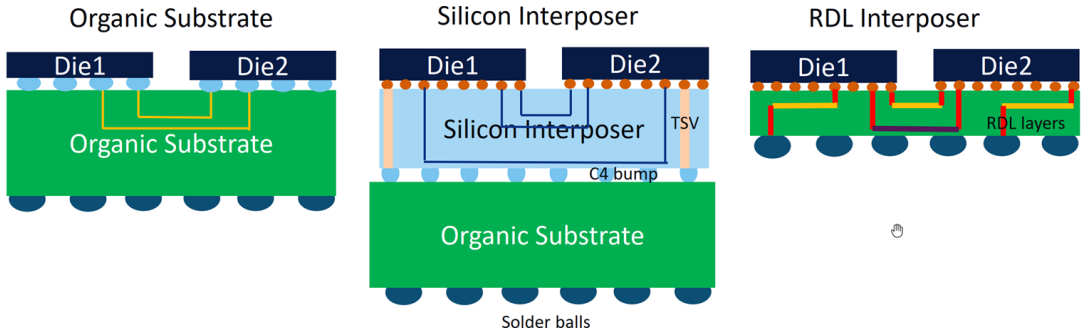


Top-level view of a monolithic SoC



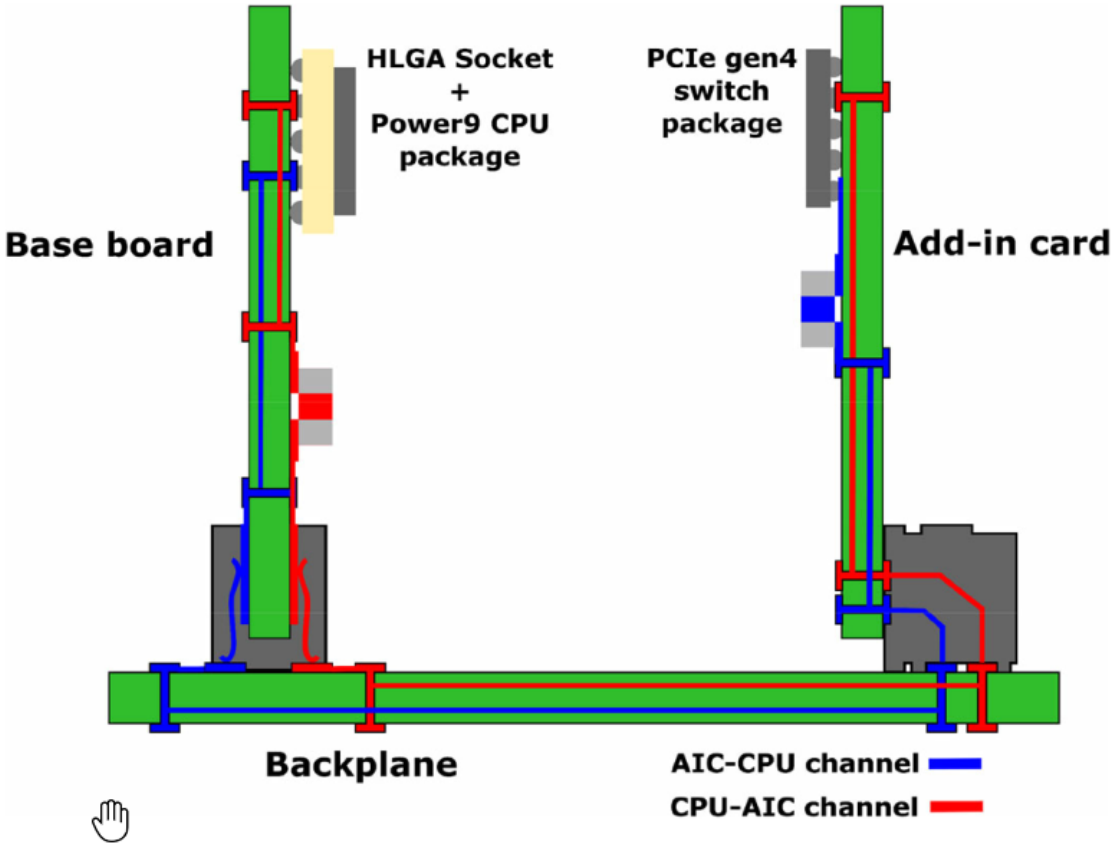
Top-level view of a chiplet-based System

They are Different from Traditional Chip-to-Chip Interconnects (1/2)



A couple of D2D Interconnect configurations

A. Ramamurthy, *Chiplet Technology and, Heterogeneous Integration*, June 2021



Topology of a PCIe link*
(traditional chip-to-chip interconnects)

*E. Orekhov et al, *"Signal Integrity Analysis and Peripheral Component Interconnect Express Backplane Link Compliance Assessment,"* Engineering Reports, Feb. 2022

They are Different from Traditional Chip-to-Chip Interconnects (2/2)

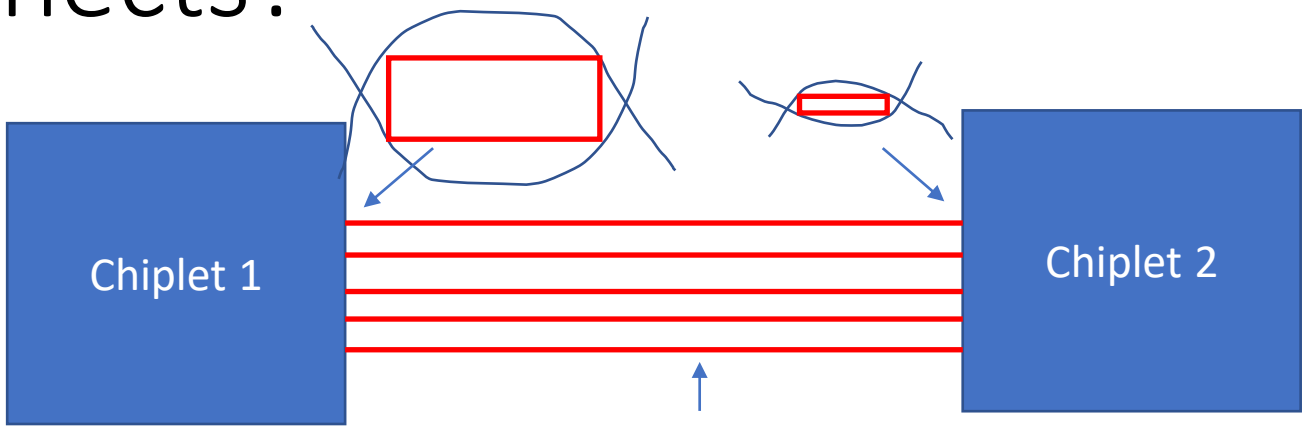
D2D Interconnects

- Lie inside package
- Both org. & Si interposers/bridges
- Mostly stripline
- Shorter in reach (2-50 mm)
- Mostly parallel
- Terminated or Unterminated
- Examples:
  - Parallel: UCIe, BoW, AIB, OpenHBI
  - Serial: XSR

Traditional chip-to-chip Interconnects

- Go outside the package
- Mostly organic substrates
- Mostly microstrip
- Longer in reach
- Both parallel and serial
- Usually terminated
- Examples:
  - Parallel: DDRx, PCIe
  - Serial: USB, HDMI

Why Signal Integrity (SI) for D2D Interconnects?



Copper or Optical Fibers

D2D Interconnects degrade signal transmitted, leading to logic failure

Quantity	Signal Integrity Effects
Lossy lines	Intersymbol interference
Densely-spaced Parallel Lines	Crosstalk
Termination	Data rate
Transmit and Receiver Jitter	Reduced Eye margin

SI Analysis: Predictive Vs. Post-Layout

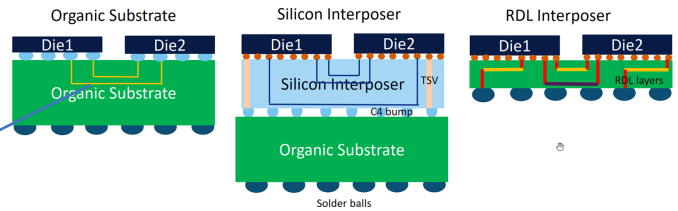
Predictive

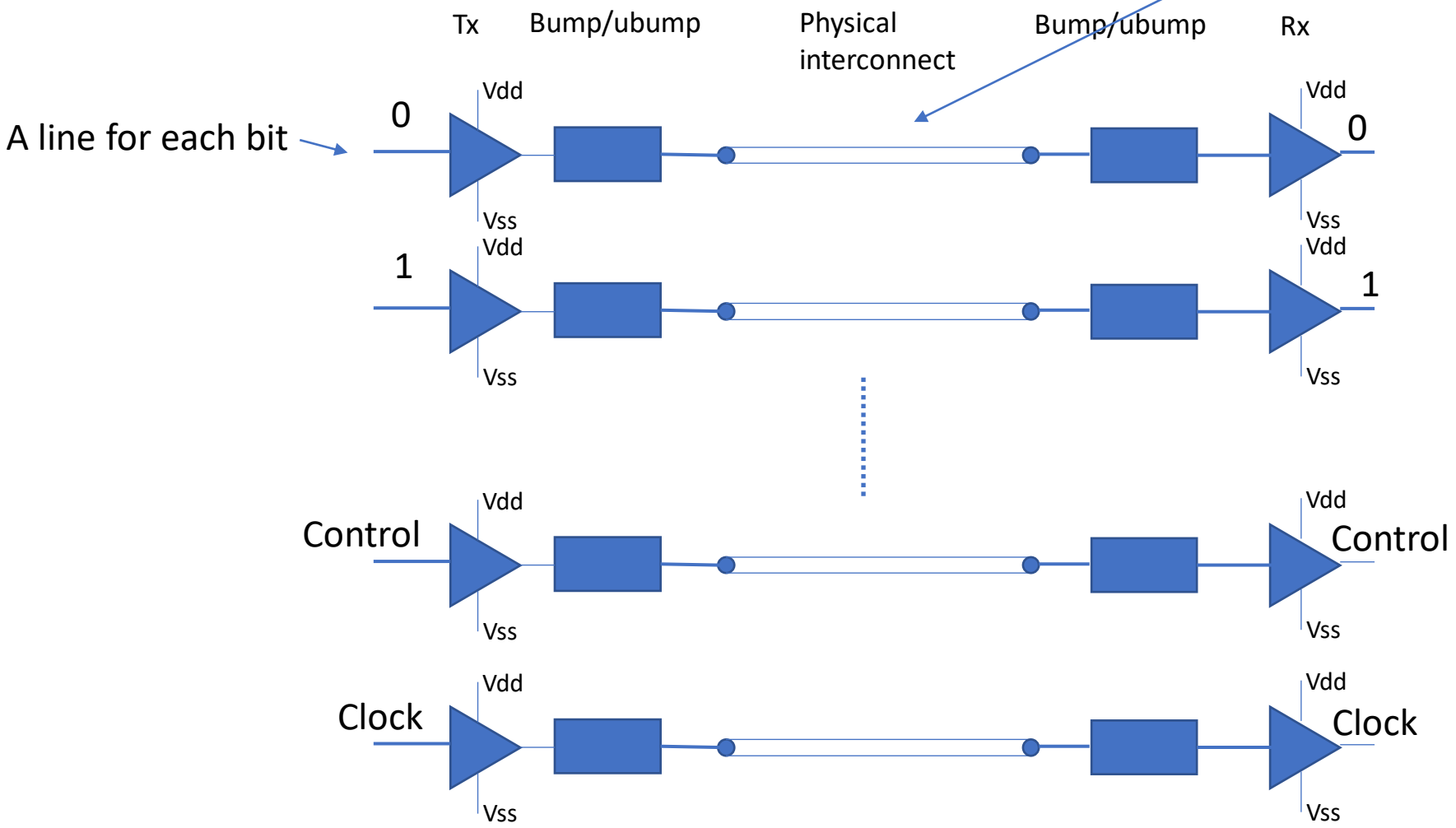
- Done for planning
  - Limited info. or only estimates available
  - Decide packaging architecture
  - Decide interconnect type
  - Decide Protocol
  - Design space exploration

Post-Layout

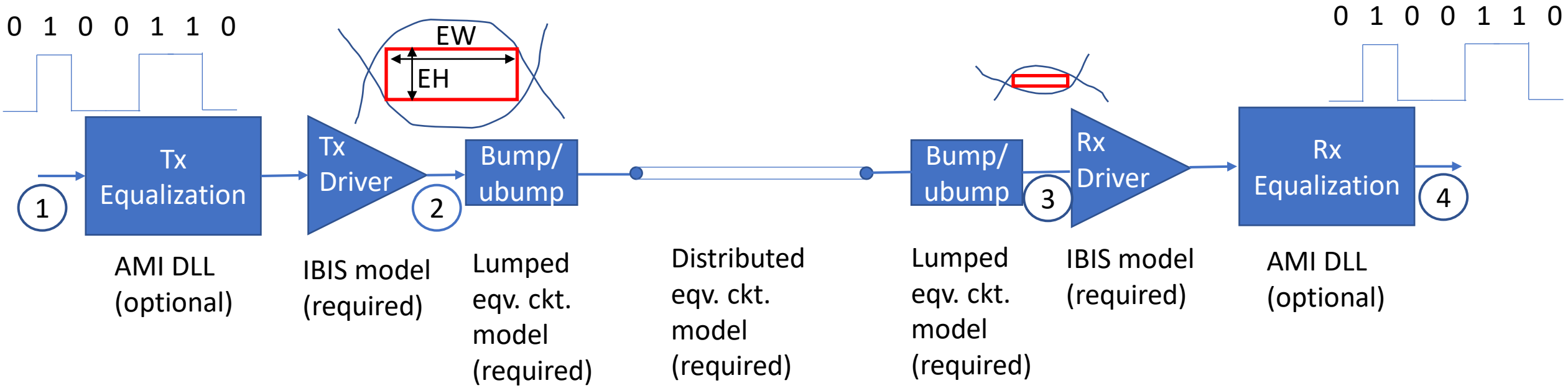
- Done for sign off
  - Full information available
  - Very limited choices

Predictive SI Simulation Set up for Parallel Interfaces

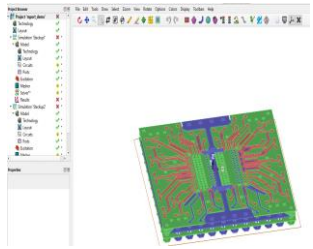




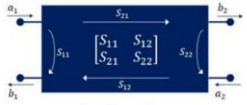
Predictive SI Simulation Set up for Serial Interfaces



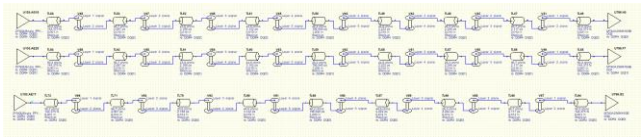
Post-Layout SI Simulation Workflow



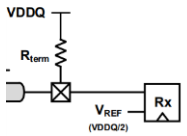
Layout Stackup



Extract Parasitics



Terminations

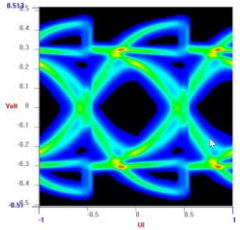


Protocol

e.g., USB, PCIe, HDMI, DDR

Create equivalent ckt.

Simulate SI



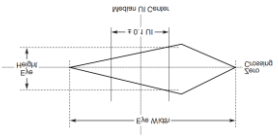
Are electrical specs. met?

No

SI test fail

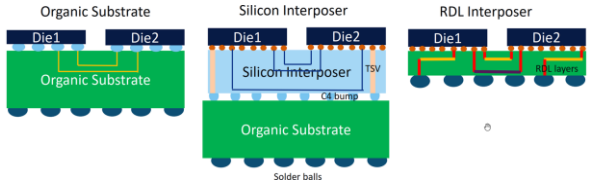
Yes

SI test pass

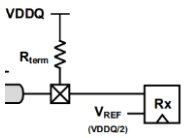


Predictive SI Simulation Workflow

D2D interconnect geometry Stackup Constraints

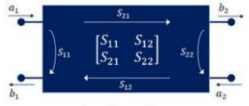


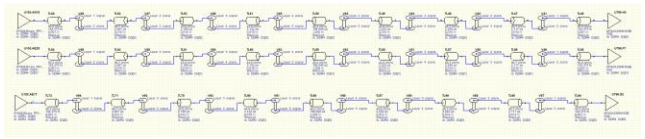
Terminations



Create variations

Extract Parasitics



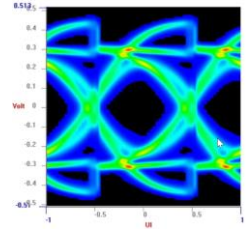


Protocol

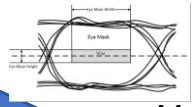
Ex: UCIe, BoW, XSR

Create equivalent ckt.

Simulate SI



Identify config. w/ best SI



Are electrical specs. met?

No

SI test fail

Yes

SI test pass

Conclusions

- D2D Interfaces require SI compliance testing.
- SI analysis for D2D interfaces similar to that for traditional chip-to-chip interfaces.
- Predictive SI analysis needed for D2D interfaces given the limited information known.
- Predictive SI analysis workflow for D2D interfaces adapted from the existing workflow for traditional chip-to-chip interfaces.
  - Key change is the design space exploration