



January 24 - 26, 2023
DoubleTree by Hilton San Jose
ChipletSummit.com

Developing and Managing System Netlists for Chiplets Integration

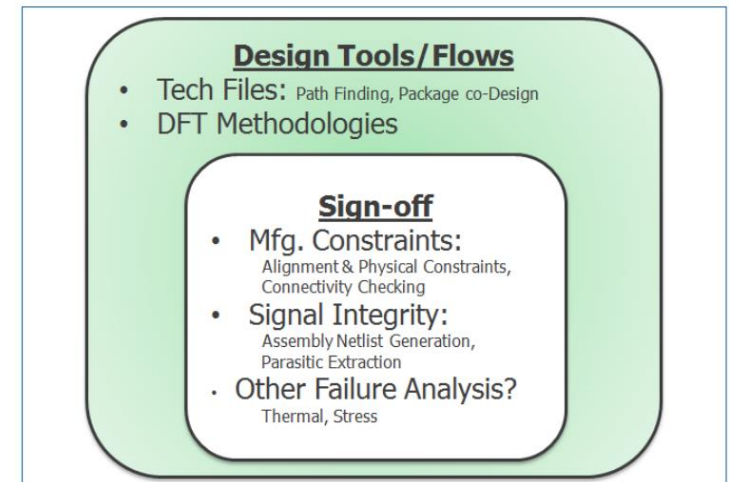
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Agenda

- Introduction
- System Level Connectivity
- Cross Domain Assembly Verification
- Conclusion
- Q&A

Introduction

- Heterogeneous Integration is gaining significant traction
 - Chiplets: “mix and match” IPs as dies
 - Silicon interposer-based
- Designers need to ensure:
 - Acceptable yield
 - Correct functionality (as intended)



- For “full assembly” physical verification ... what is required?
 - Confirm that the full assembly is connected as “intended”
- How can the designer capture the “intended” connectivity?
 - Multiple substrates (for ex: interposer + organic package)

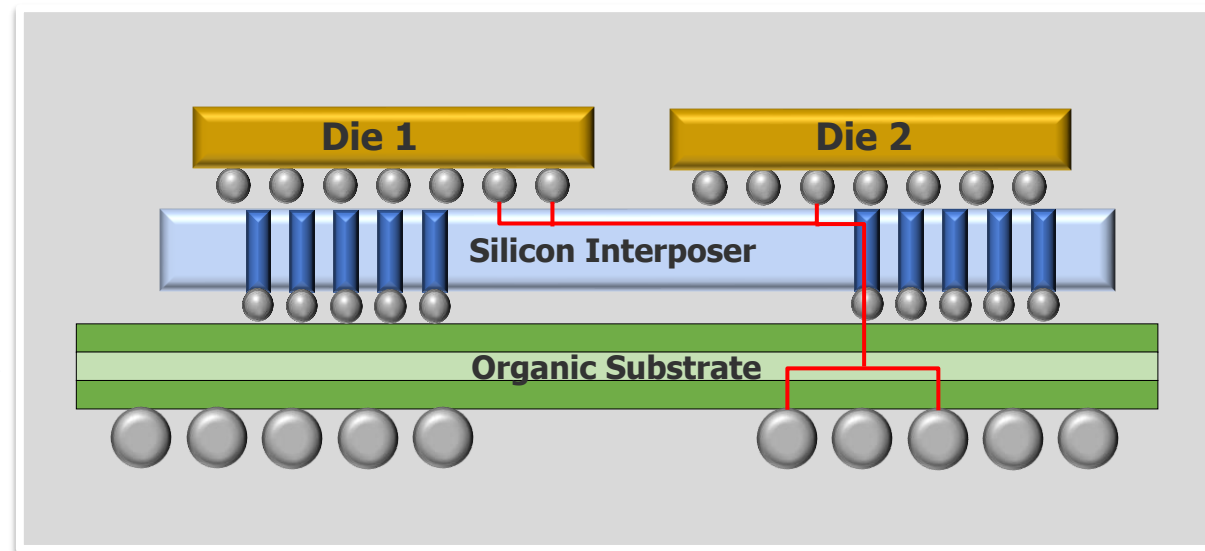
System Level Connectivity

- Designer needs to aggregate connectivity from different design teams/formats
 - Silicon Interposer → IC design team/IC design background/IC EDA tools
 - Organic substrate → Pkg design team/traditional packaging background/PCB like EDA tools

Verilog is common

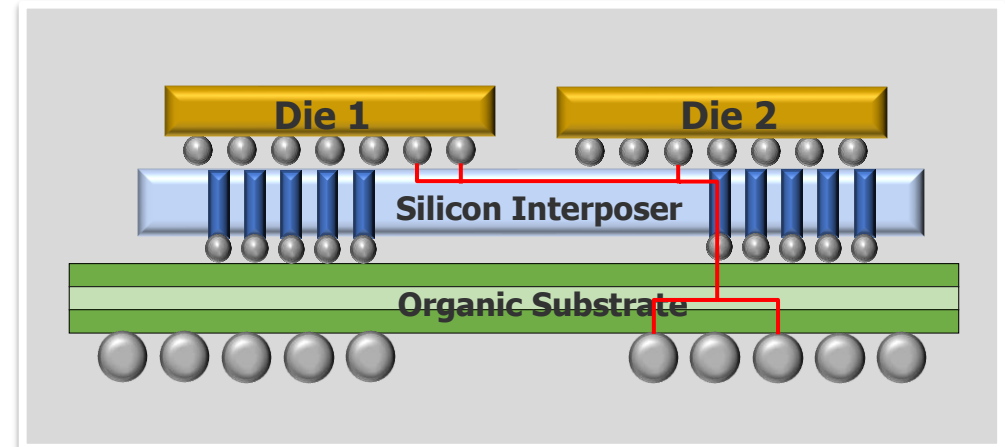
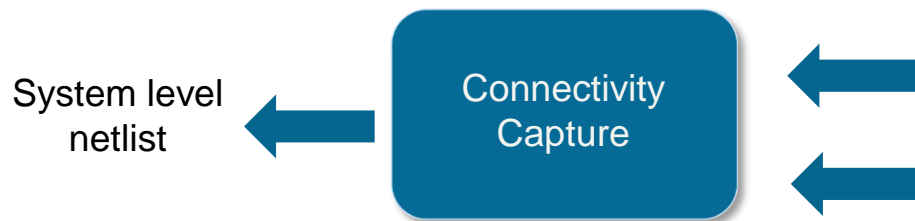


CSV is common



System Level Connectivity

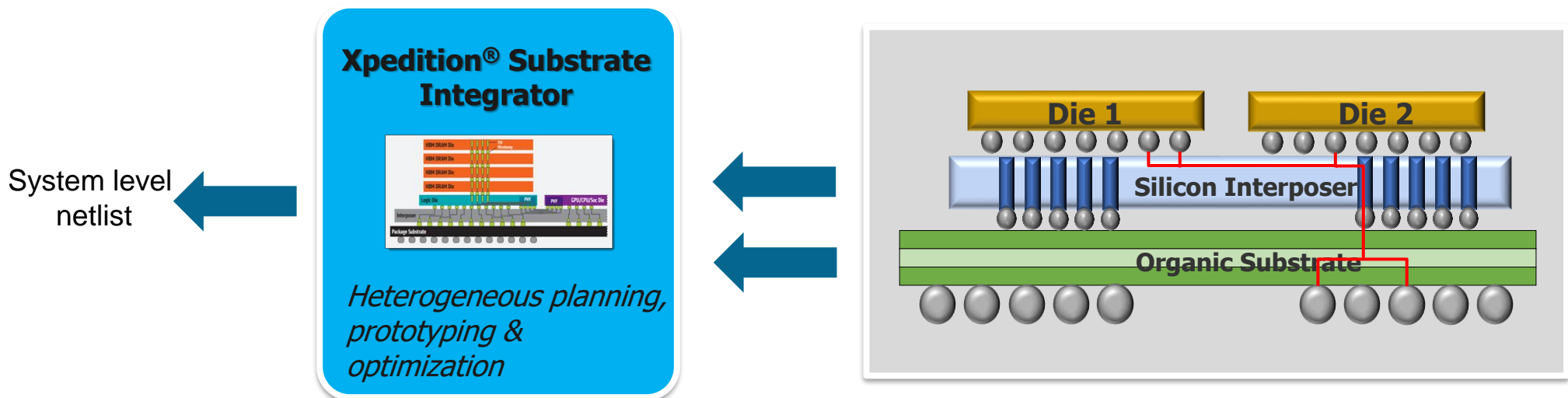
- Designers need a connectivity aggregation EDA platform
 - Connectivity planning, optimization and management
 - Imports and exports connectivity with multiple formats (mix and match)
 - Allows interactive and manual assignments and modifications



System Level Connectivity

Siemens EDA

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System Level Connectivity

Siemens EDA

- Aggregates heterogeneous data into full system model
 - Utilizing standard formats like ODB++, CSV, LEF/DEF, Verilog and GDS
- Generates the system netlist for LVS/STA
- Manages device transformations and scaling differences
- Comprehensive connectivity visualization and reporting
- Scales with design complexity (can handle millions of pins)

The screenshot displays the 'Instance Level Netlist' window in Siemens EDA software. The window contains an 'Export Preview' table with the following data:

| Functional Signal | Instance Level Name | Die Internal Net | Design Name | Definition | Instance Name | Pin Number |
|-------------------|---------------------|------------------|-------------|------------|---------------|-------------|
| SCAN_INT_OUT[16] | SCAN_INT[21] | | BGA | C4 | C4 | B4 |
| SCAN_INT_IN[16] | SCAN_INT[21] | | BGA | C4 | C4 | T4 |
| SCAN_INT_IN[16] | SCAN_INT_IN[16] | | FOWLP | C4 | C4 | T4 |
| D_scan_out[16] | SCAN_INT_IN[16] | D_scan_out[16] | FOWLP | chip | chip1 | Bump_BUMP_9 |
| SCAN_INT_OUT[16] | SCAN_INT_OUT[16] | | FOWLP | C4 | C4 | B4 |
| D_scan_in[16] | SCAN_INT_OUT[16] | D_scan_in[16] | FOWLP | chip | chip2 | Bump_BUMP_9 |

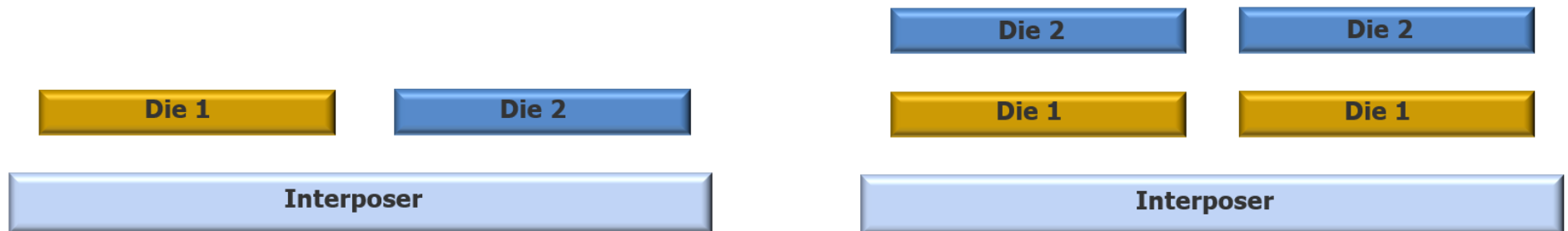
Below the table, the 'Parameters' section shows 'Show Power Nets' checked and 'Export File' set to 'D:\WDIR\Sandbox\ISO_PROJECTS\demo\flow_demo\SystemNetlist.csv'. The background shows a complex connectivity visualization with numerous pins and connections.

The 'Project - [KIT] [DieInterposer]' window is also visible, showing a tree view of the design hierarchy:

- DieInterpo...
 - interposer interposer I1
 - gdieR gdieR A3
 - gdieL gdieL A2
 - gdie gdie A1
 - U2 U2 U2
 - U1 U1 U1

Cross Domain Assembly Verification

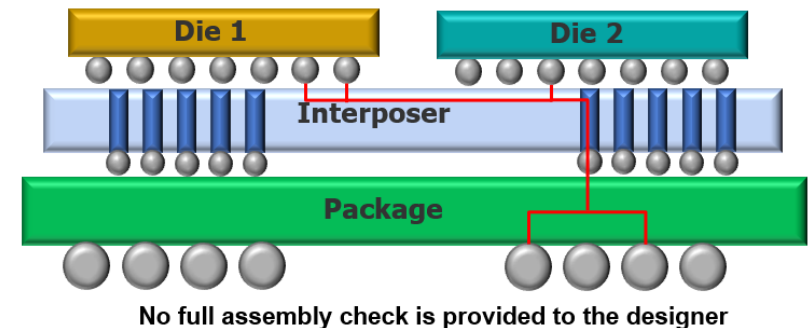
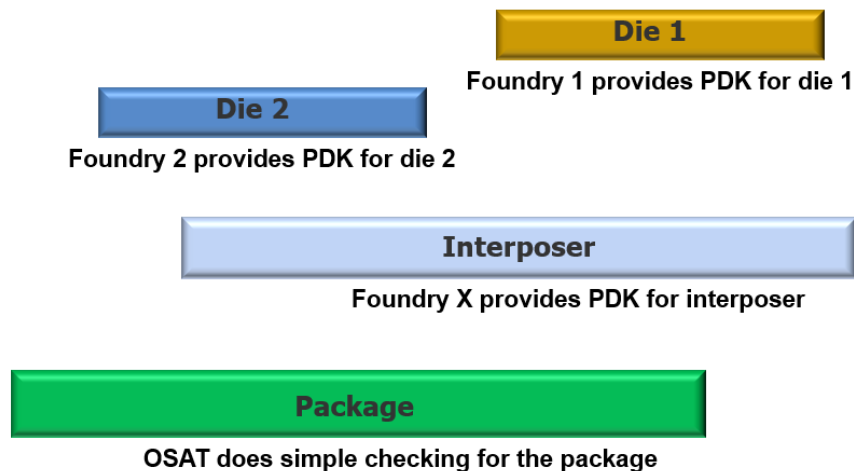
- PV sign off for a silicon interposer assembly requires:
 - Individual die(s) DRC and LVS
 - Silicon interposer DRC and LVS } Standard PDK from the foundry
- Die(s) alignment and inter-connectivity to the interposer
 - Foundry support is challenging!
 - Die's location and orientation can change from one design house to another and from one project to another



Assembly Description is required

Cross Domain Assembly Verification

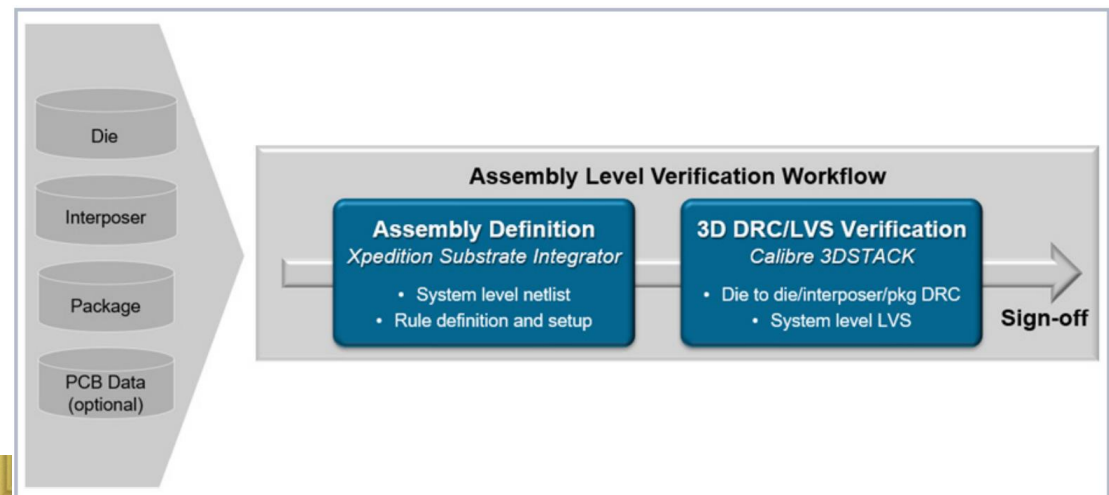
- What happens in case of multiple substrates?
 - A silicon interposer (foundry)
 - An organic substrate (OSAT)



No single manufacturer can provide a “full system” PDK

Cross Domain Assembly Verification

- 3D-IC designers need a way to generate the PV setup files themselves
 - Account for the full, multi substrate assembly
 - Automated
- xSI includes a plug-in that enables the generation a complete Calibre 3DSTACK run set
 - Full assembly description and comprehensive assembly checks
 - Designer's centric verification



Conclusion

- Capturing the system-level connectivity in a multi-substrate 3D-IC can be a challenge
 - Especially true when each substrate is built using a different methodology, team, and/or format
- Designers need an EDA platform such as Xpedition Substrate Integrator (xSI) that can aggregate the different formats for a multi-substrate system and generate a system-level netlist
- Using xSI & Calibre 3DSTACK, the system level designer can automatically generate a complete assembly verification runset
 - A “designer-centric” approach since it is agnostic to the different die technology nodes and substrate manufacturers

Q&A



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