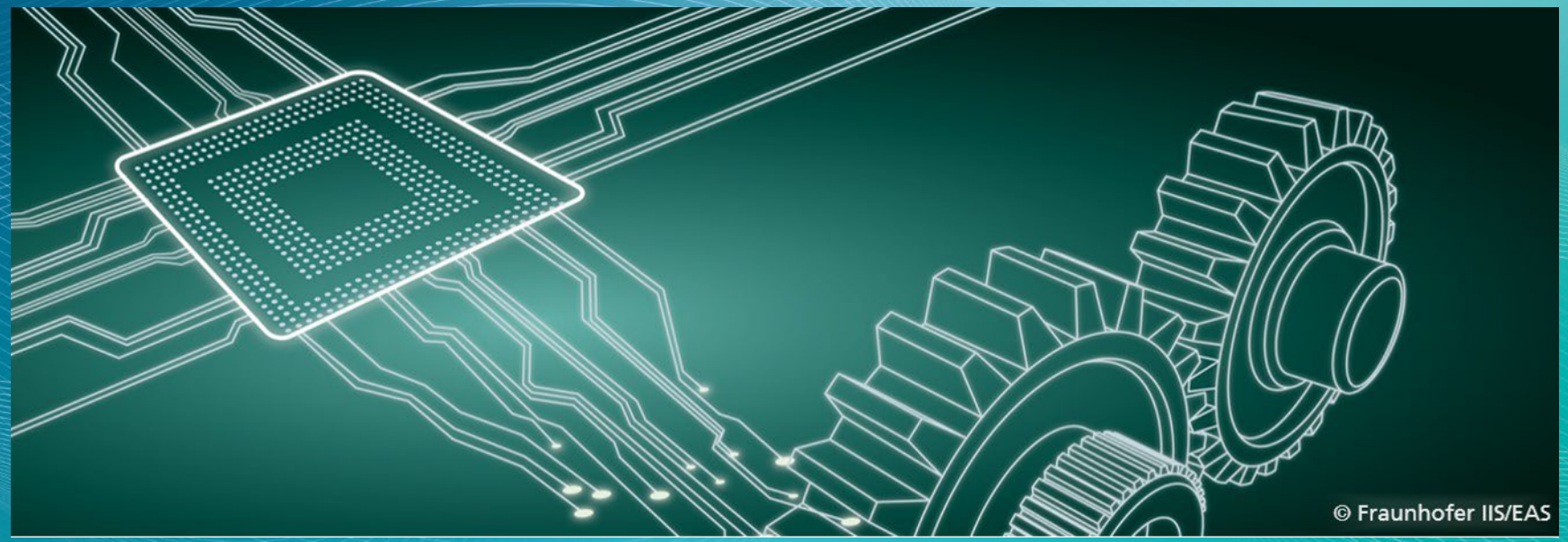
CHIPLET SUMMIT

January 24 - 26, 2023
DoubleTree by Hilton San Jose
ChipletSummit.com



Fraunhofer IIS/EAS Dresden

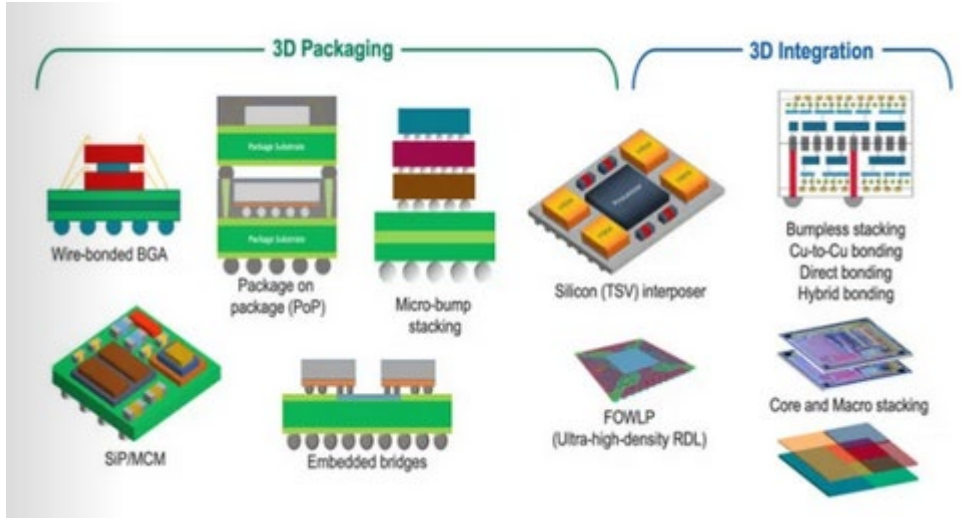
Annual Update on Packaging

Outline

- Introduction
- Packaging market share
- Roadmap
- Technology trends
  - High-End packaging
  - Wafer-Level Packaging
  - SiP Packaging
  - Hybrid Bonding
  - Chiplet Packaging

Introduction

- Wide range of potential packaging technologies available
- Many specific for certain domains



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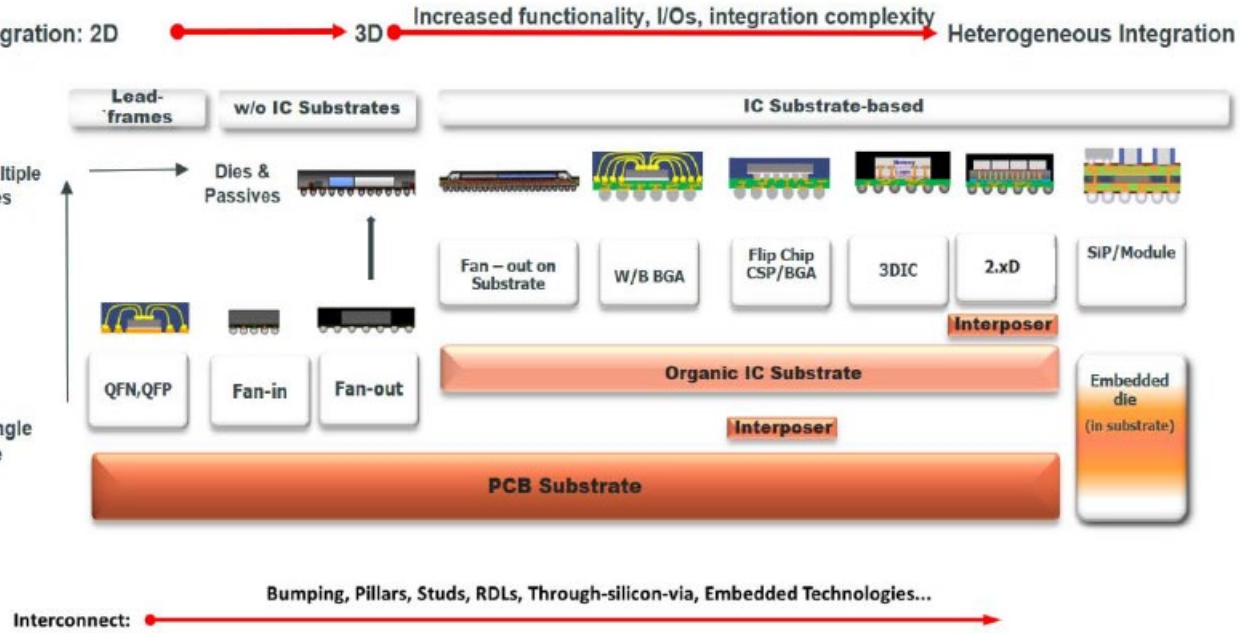

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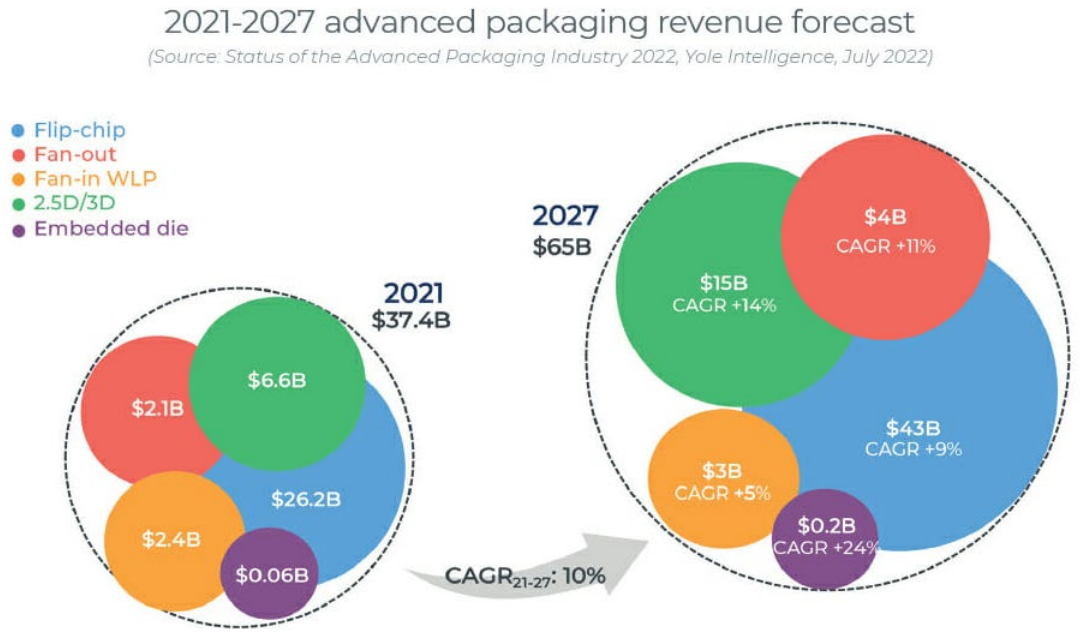
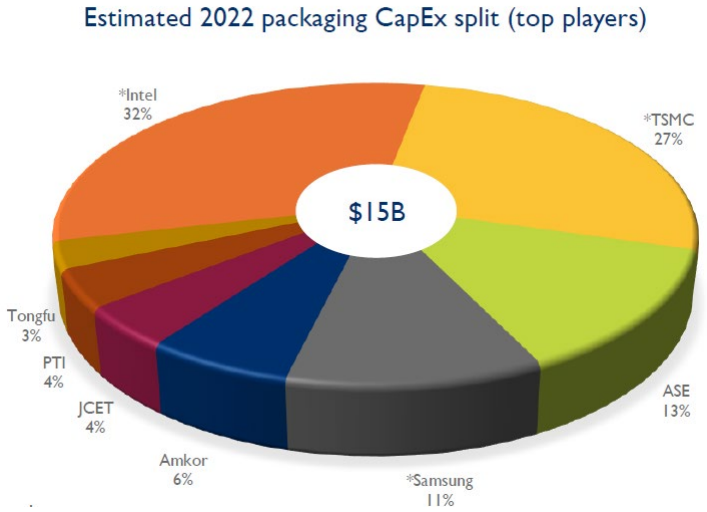
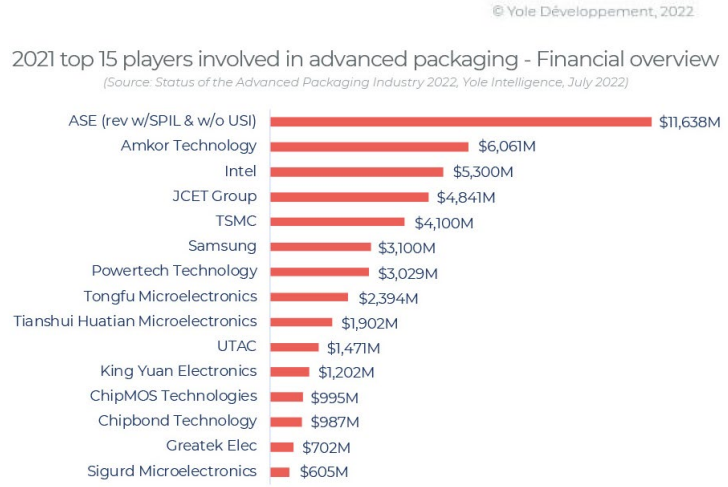
Packaging market share

Advanced Packaging

- Big market share in past and currently by OSATs like ASE and Amkor
- IDMs and Foundries like Intel and TSMC are gaining market share
- Largest investments are not from OSAT side with potentially disrupting the market
- Grow expected at around 10% per year



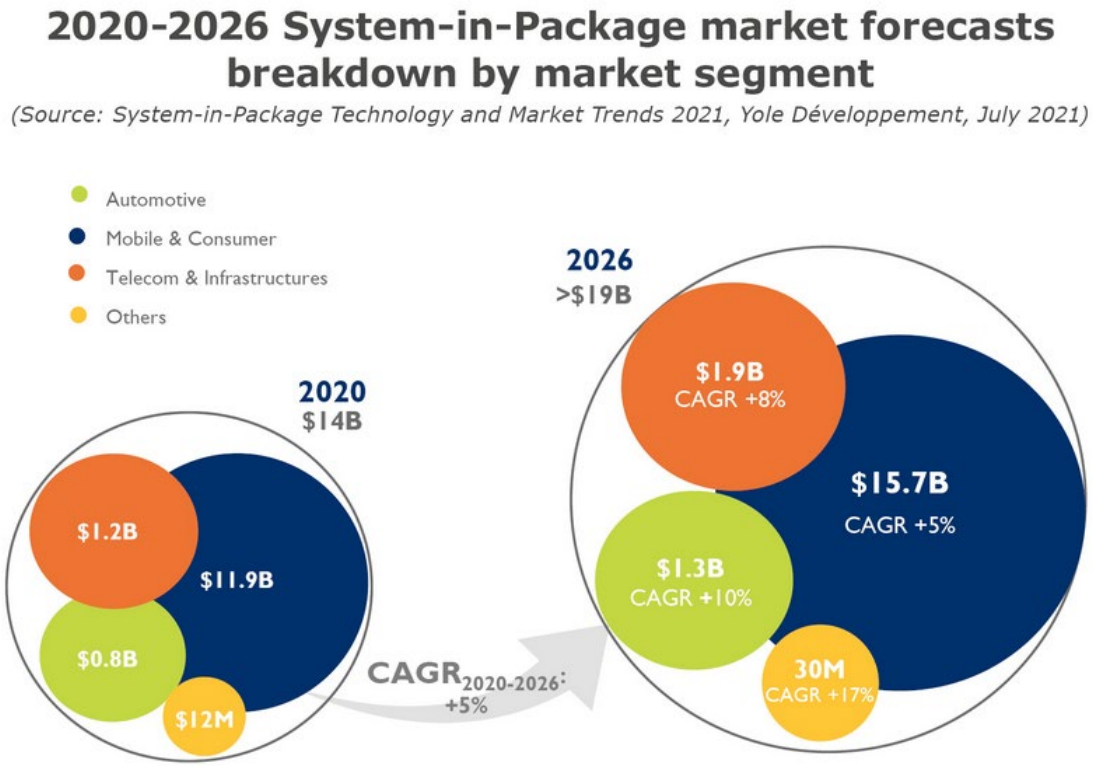




Packaging market share

System in package (SiP)

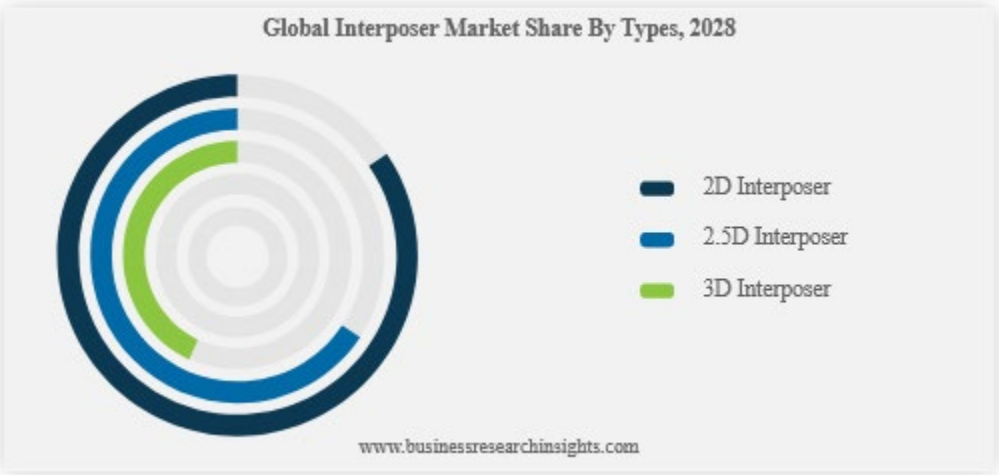
- Largest amount on market share in packaging is in respect to SiP
- Dominated by the mobile market, which will be the largest market for the upcoming years
- Grow is slightly smaller than packaging market in general
- Saturated market with spans across IDM, Foundries and OSATs

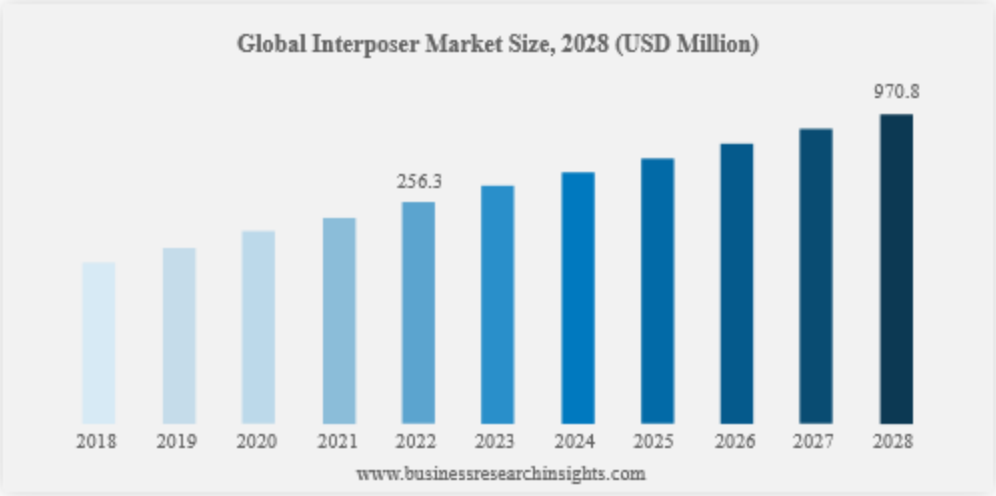


Packaging market share

Interposer

- Currently small market share in packaging with ~250M$
- But estimated high growth rate of around 20%
- North America dominated due to higher costumer demands
- “classical” 2D interposer have the largest market share

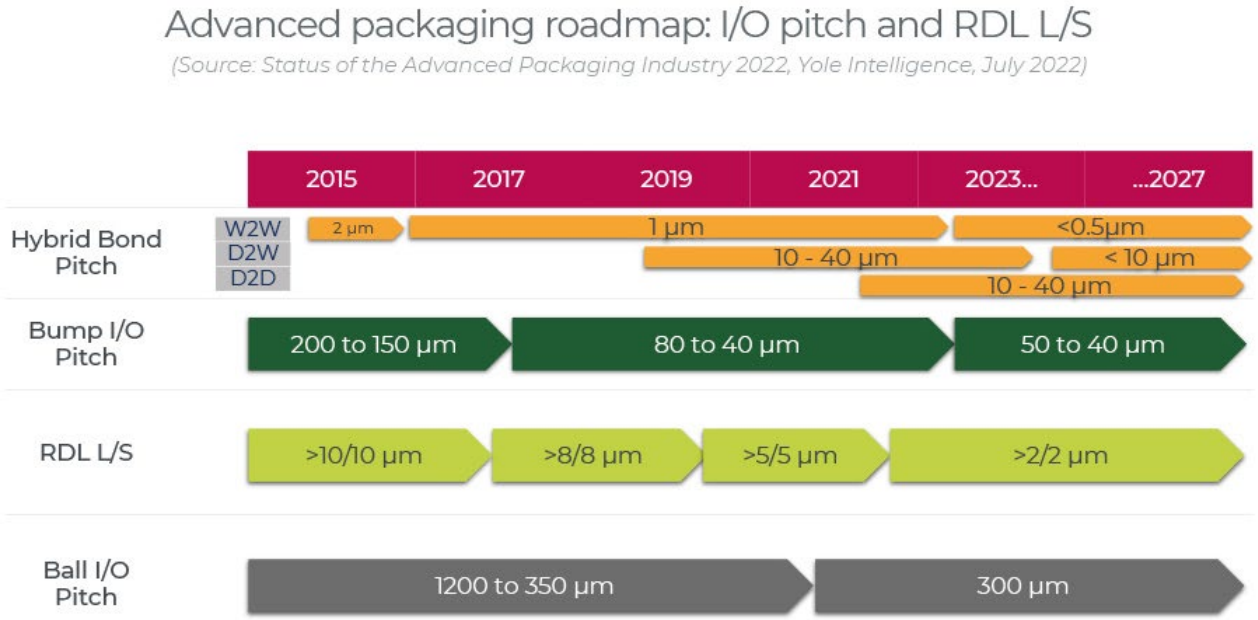




Packaging Roadmap

Pitch and spacing view

- Still ongoing trend to smaller feature sizes
- But only limited reduction expected in bump and ball pitch
- Largest achievements in pitch reduction are expected in Hybrid bonding
  - with wafer2wafer already mature for very fine pitches
  - And major advances are expected in die2wafer and also die2die bonding



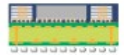
Packaging Roadmap

SiP

- Still ongoing trend to smaller feature sizes

2017-2025 SiP technology roadmap - key parameters

(Source: System-in-Package Technology and Market Trends 2021, Yole Développement, July 2021)

	Metrics	<2017	2019	2022	2025	SiP Advancement
Flip Chip (IC Substrate)	Substrate RDL L/S	30/30 to 10/10 µm	10/10 to 5/5 µm		8/8 to 5/5	FC BGA SiP 
	Substrate I/O Pitch	1200 to 350 µm			300 µm	
	Substrate I/O Ball	500 - 3000		>> 3000		
	Max Package Size	> 65x65 mm		>> 80x80 mm		Double-Sided FC SiP 
	Max no. of Dies/Passives	< 15	< 35	>> 35		
	Max level of RDLs	10 -16x RDL		>> 10x RDL		
Fan-Out	Substrate RDL L/S	15/15 to 8/8 µm	5/5 ! m to 2/2 µm		< 1/1 µm	FO on Substrate 
	Substrate I/O Pitch	400 µm	350 µm	200 µm		
	Substrate I/O Ball	< 300	600 -1300	>> 1500		
	Max Package Size	< 5x5 mm	< 25x25 mm		< 30x30 mm	HD FO SiP PoP 
	Max no. of Dies/Passives	≤ 2	≤ 4	≤ 6		
	Max level of RDLs	3x – 4x RDL		> 4x RDL		
Embedded Die	Substrate RDL L/S	> 25/25 µm	> 20/20 µm		> 15/15 µm	Embedded Interconnects 
	Die I/O Pitch	250-80 µm		50 µm		
	Die I/O Numbers	40-100	100-150		150-200	
	Max Package Size	<15x15 mm		< 25x25 mm		Embedded Multi-Dies 
	Max no. of Dies/Passives	≤ 2	≤ 3		≤ 4	
	Max level of RDLs	2x - 4x RDL		4x – 6x RDL		

Packaging Roadmap

Wafer Level Packaging

- In general two different types
  - Fan-in
  - Fan-Out

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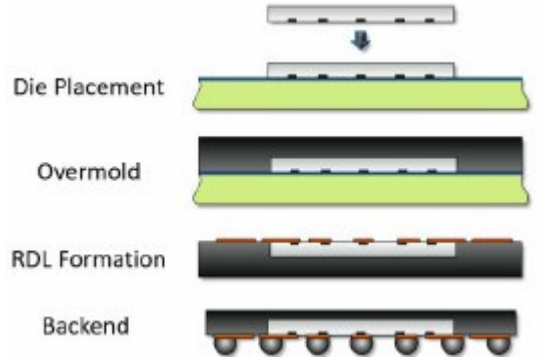
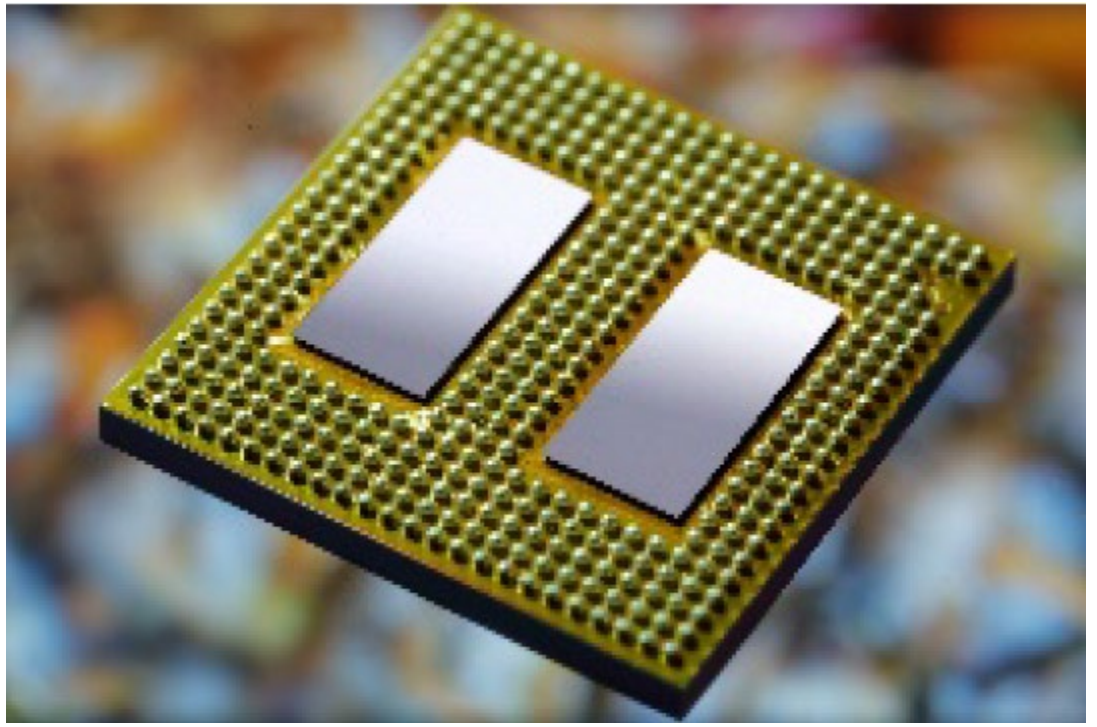
Packaging Processes

eWLB

- One variant of Fan-Out package
- Mostly for lateral communication
- Used by many packaging suppliers
  - E.g. ASE FOCoS

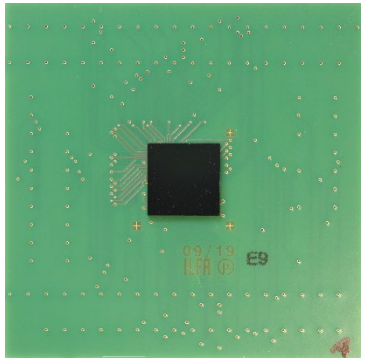


Packaging Processes



Face2Face IC assembly

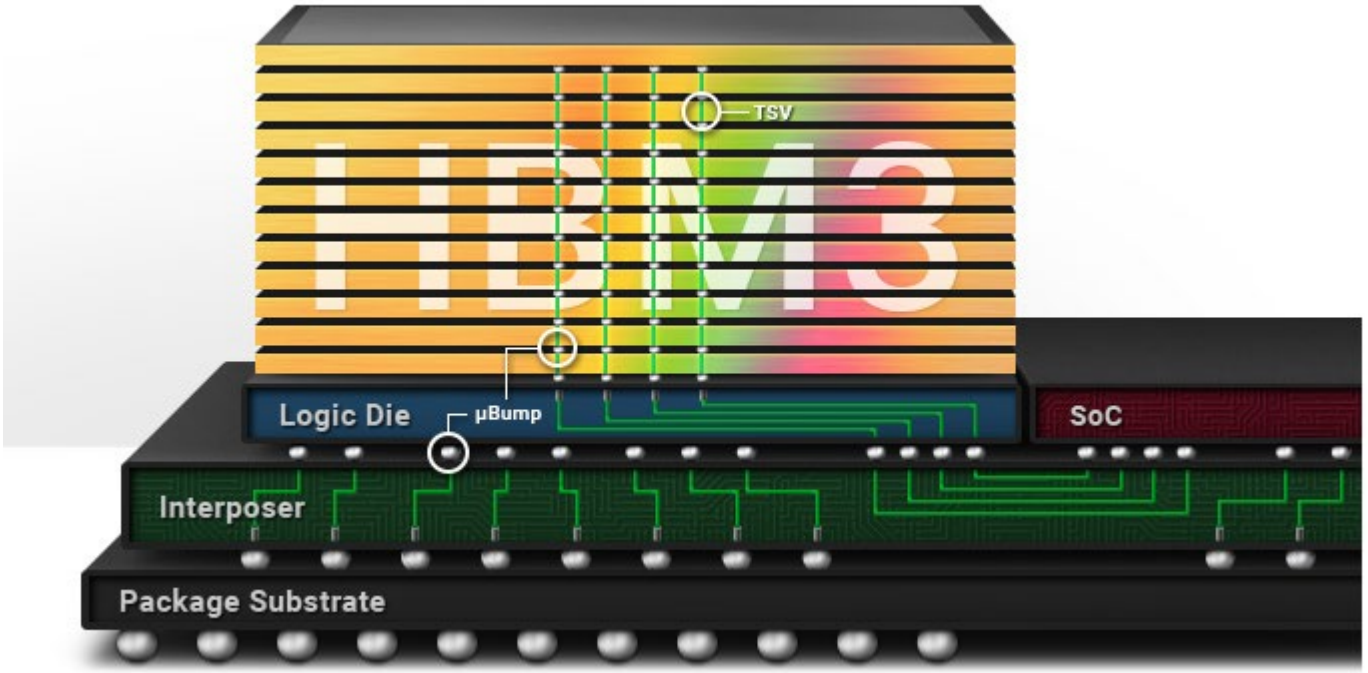
- Assembly of ICs to another IC to separate functions to different Processes (like compute and memory, or compute and logic
- Comprehensive design of system

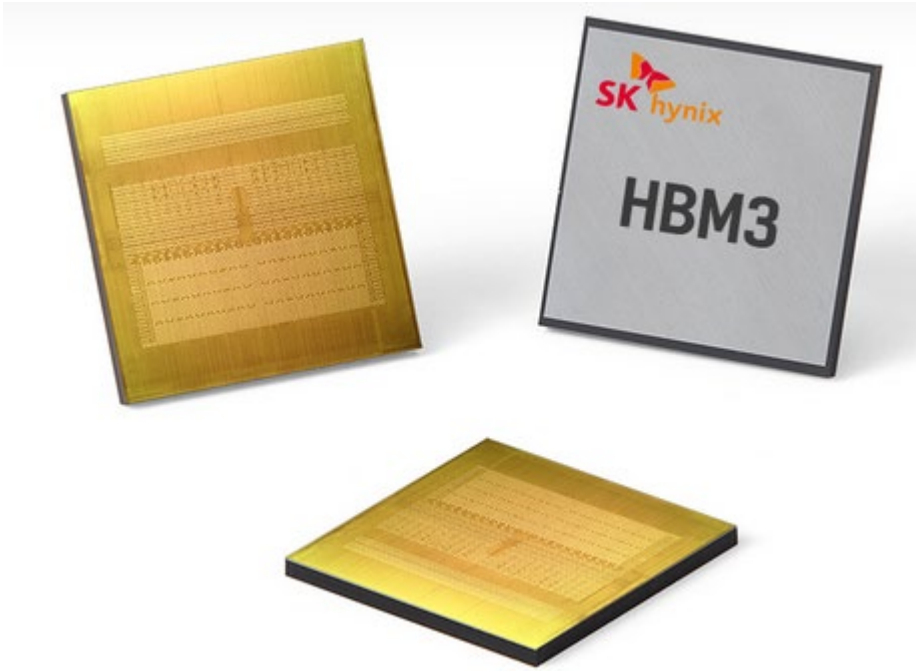


Packaging Processes

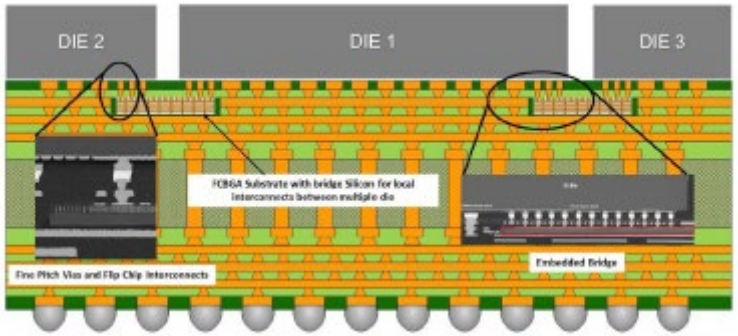
3D-Stacking

- E.g. HBM3 with up to 12 stacked dies from SK hynix





Packaging Processes



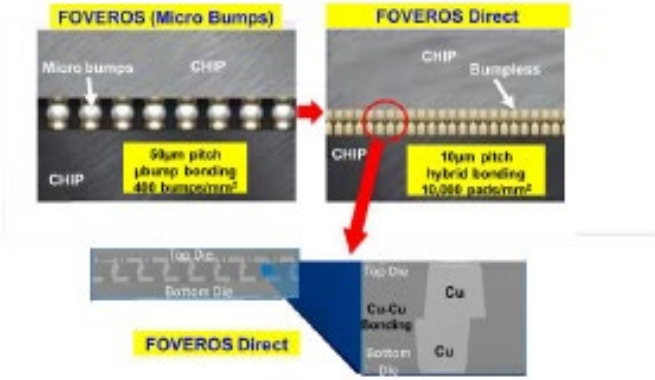
Intel EMIB

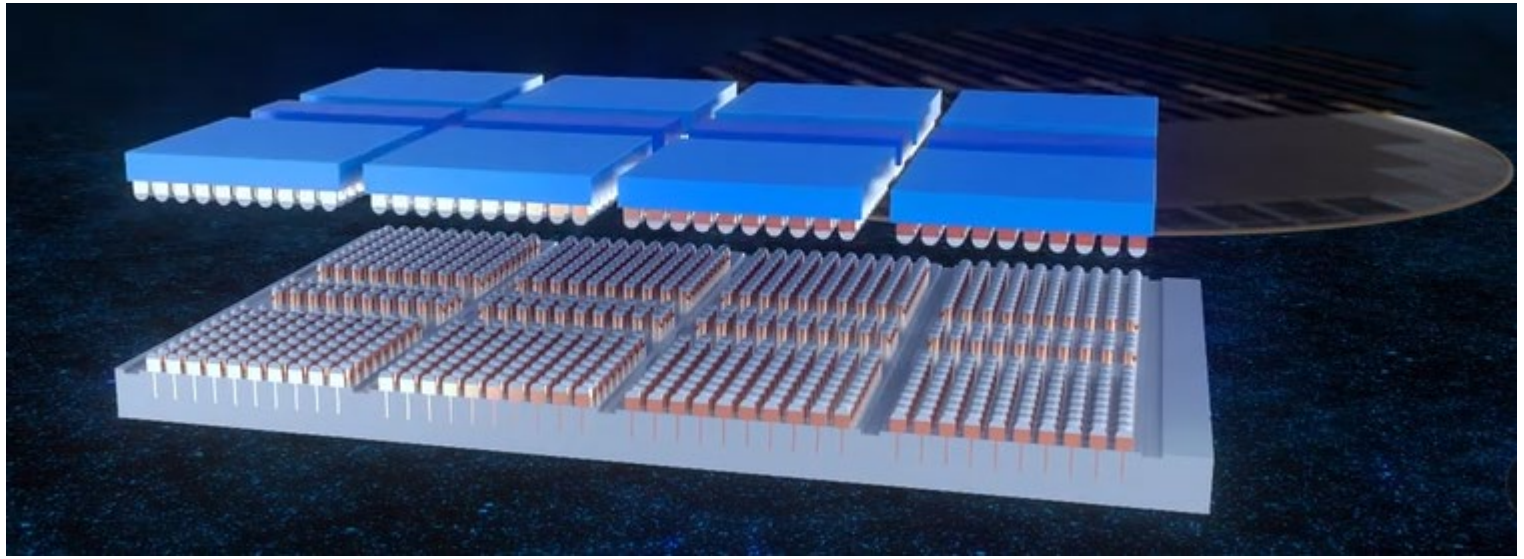
- Rigid bridge based on silicon with fine line and space for high density interconnect

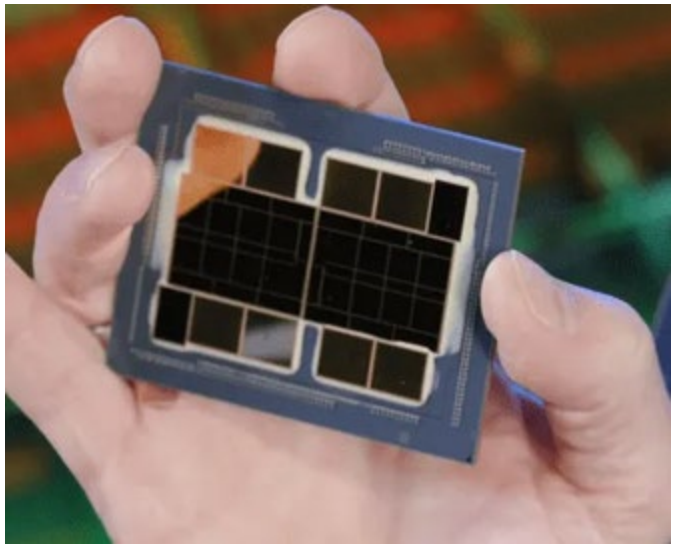
Packaging Processes

Intel Foveros

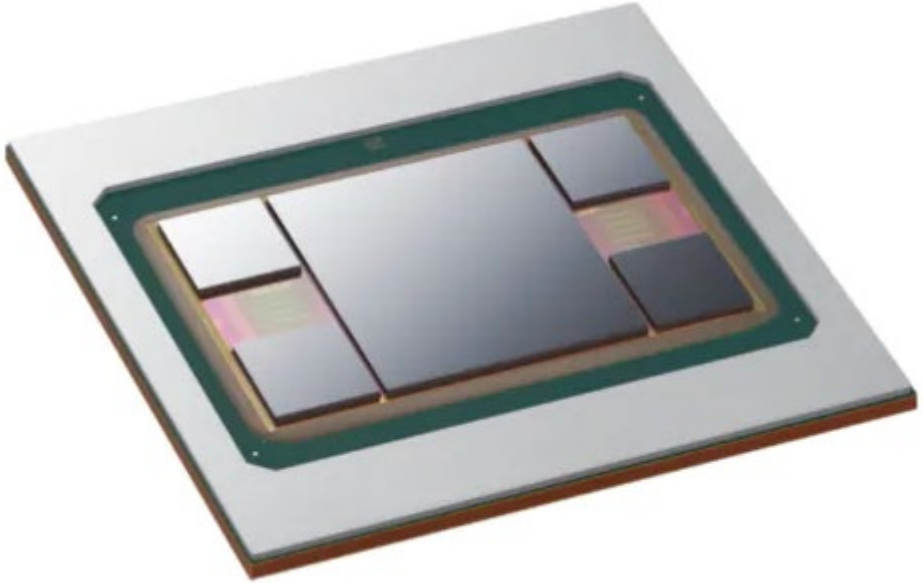
- First shipping in 2020 with "Lakefield" processor generation





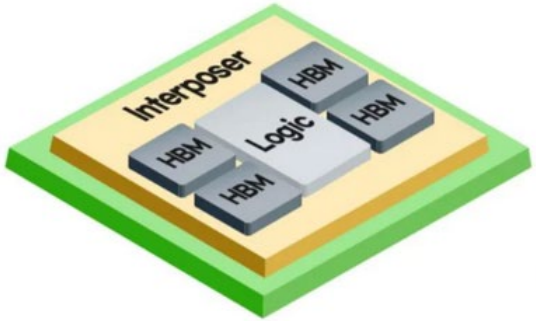


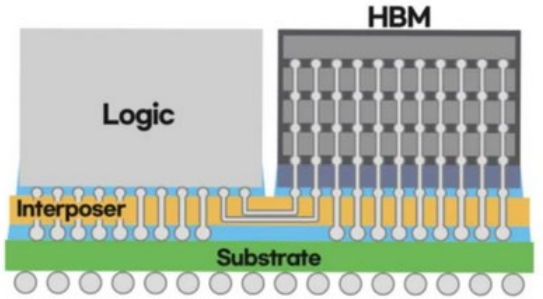
Packaging Processes



Samsung Foundry Cube Technologies

- I-Cube
  - 2.5D Si Interposer
  - Either wafer-level or substrate level
  - MiM and integrated stacked capacitor (ICP) embedded in interposer
  - Sizes up to 1600mm² qualified

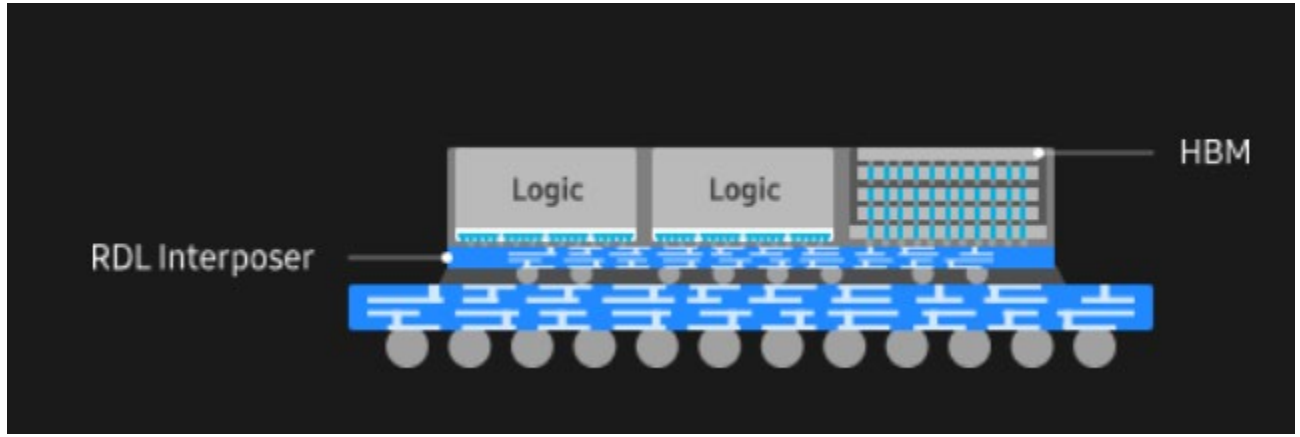




Packaging Processes

Samsung Foundry Cube Technologies

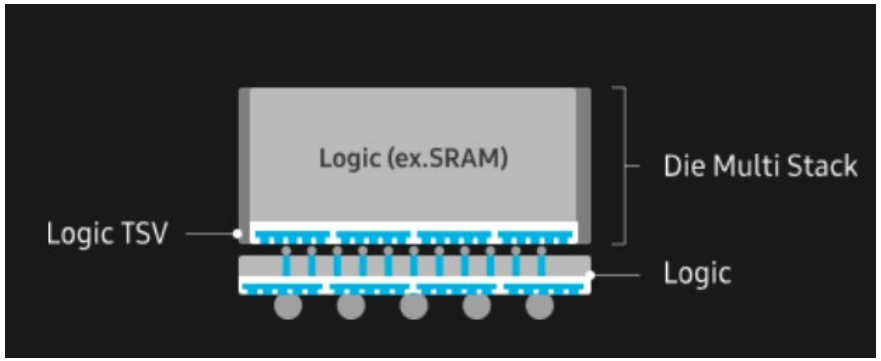
- R-Cube
  - Using RDL interposer
  - No TSVs
  - More flexibility
  - But not such fine line/space compared to silicon interposer

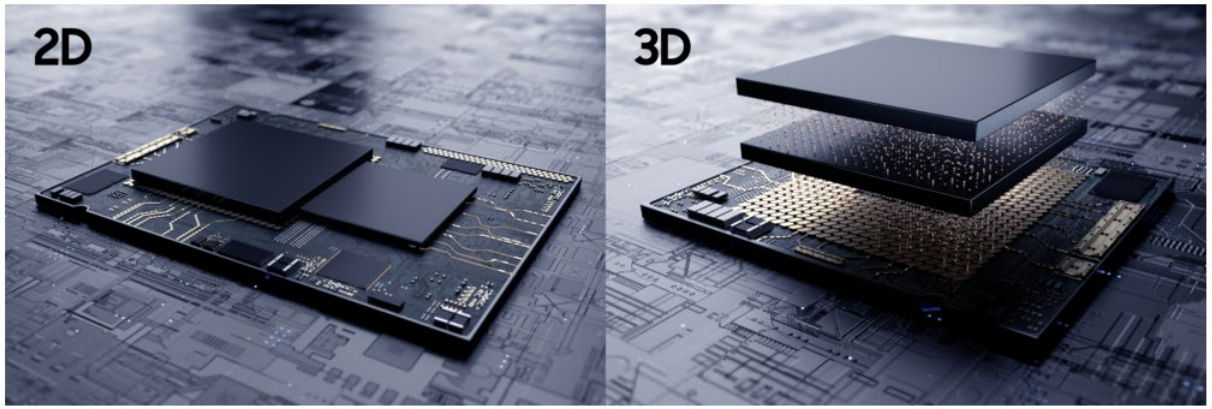


Packaging Processes

Samsung Foundry Cube Technologies

- X-Cube
  - Higher density due to 3D stacking
  - Higher bandwidth and lower latency
  - Less degree of freedom

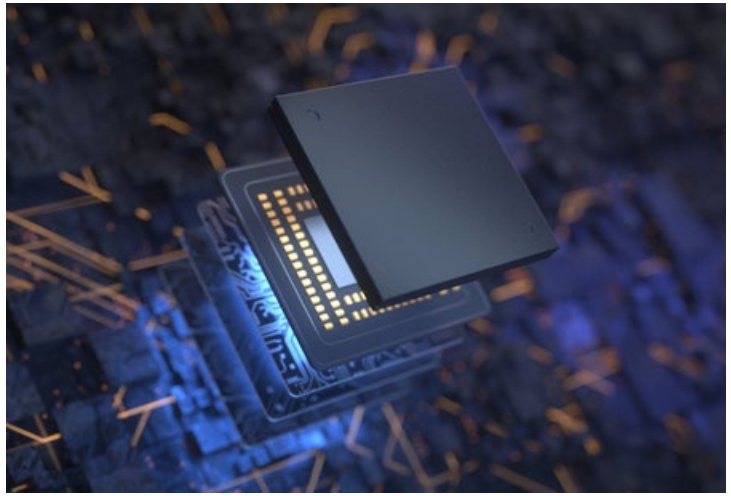


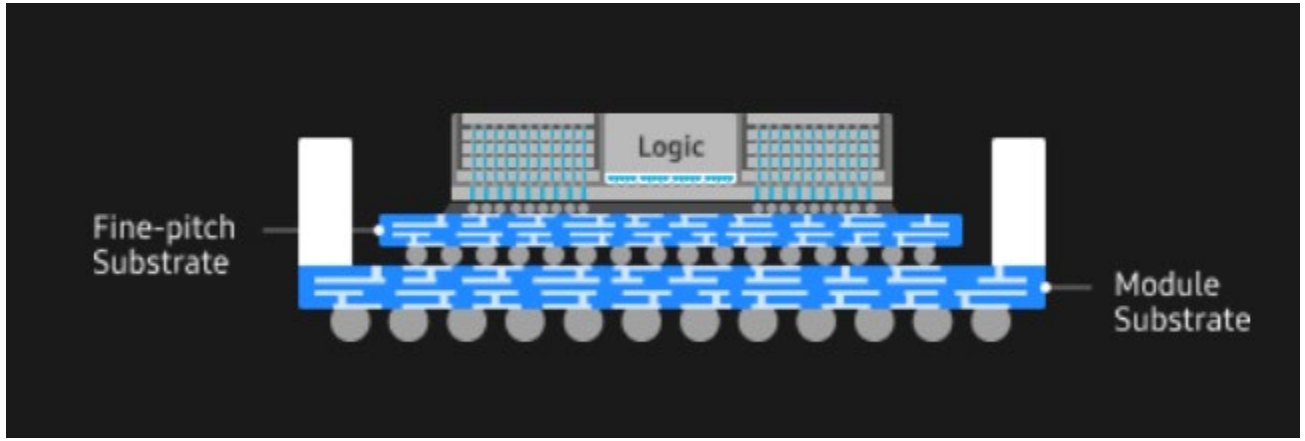


Packaging Processes

Samsung Foundry Cube Technologies

- H-Cube
  - Also called 5.5D system because 2.5D system stacked as 3d
  - Cost effective
  - Good scaling

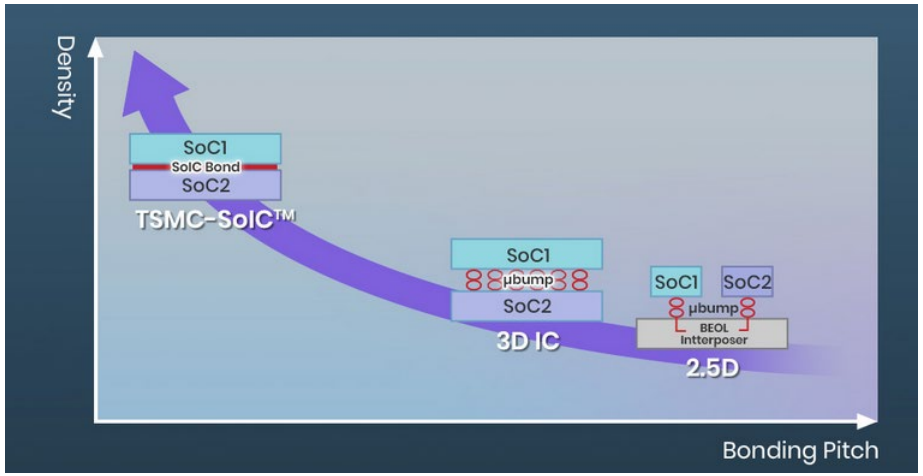


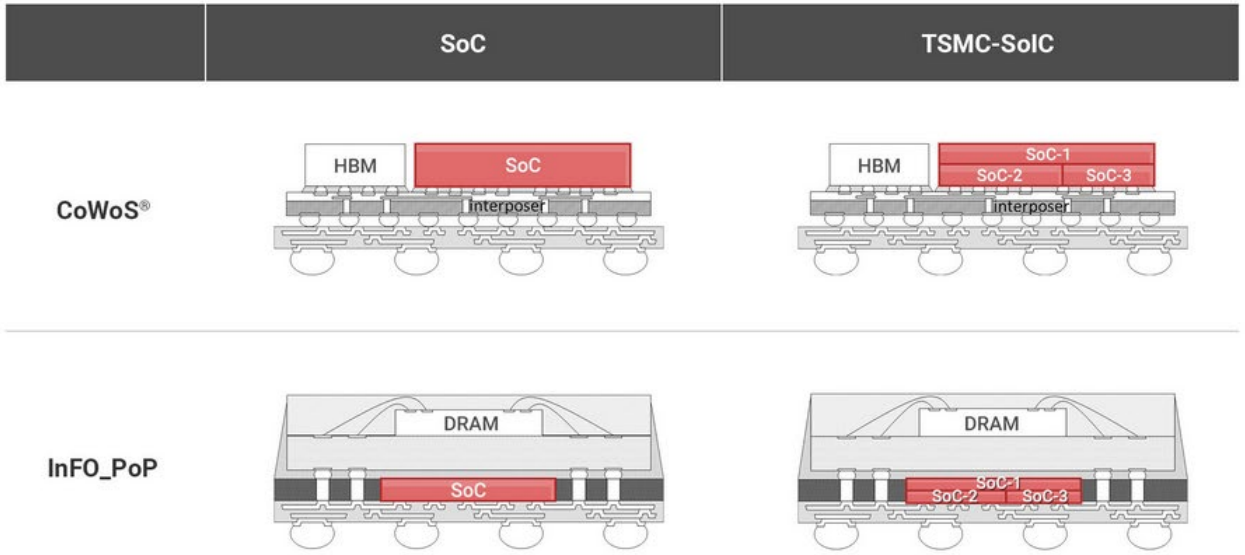


Packaging Processes

TSMC SoIC

- 3D inter-chip stacking technology
- Integration of chiplets portioned from SoC
- Meet increasing compute, bandwidth and latency requirements

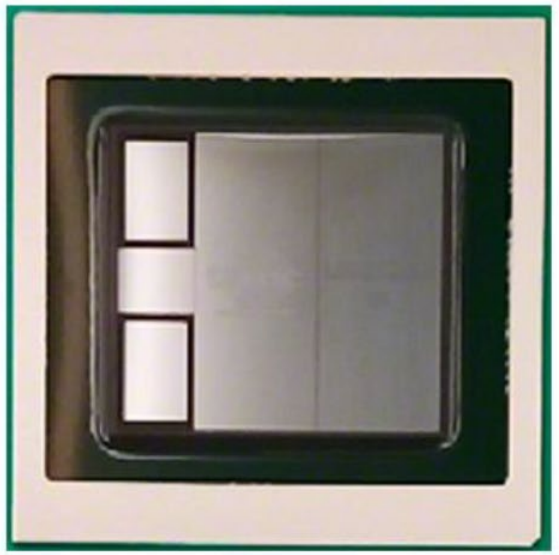


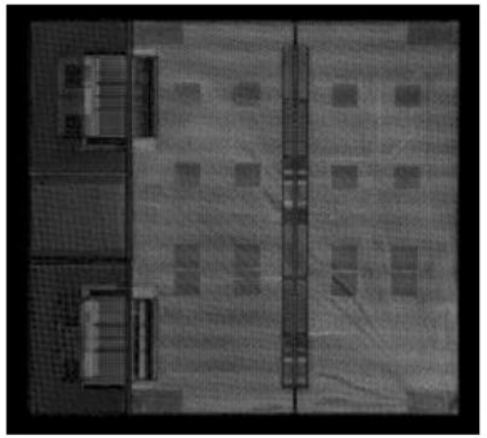


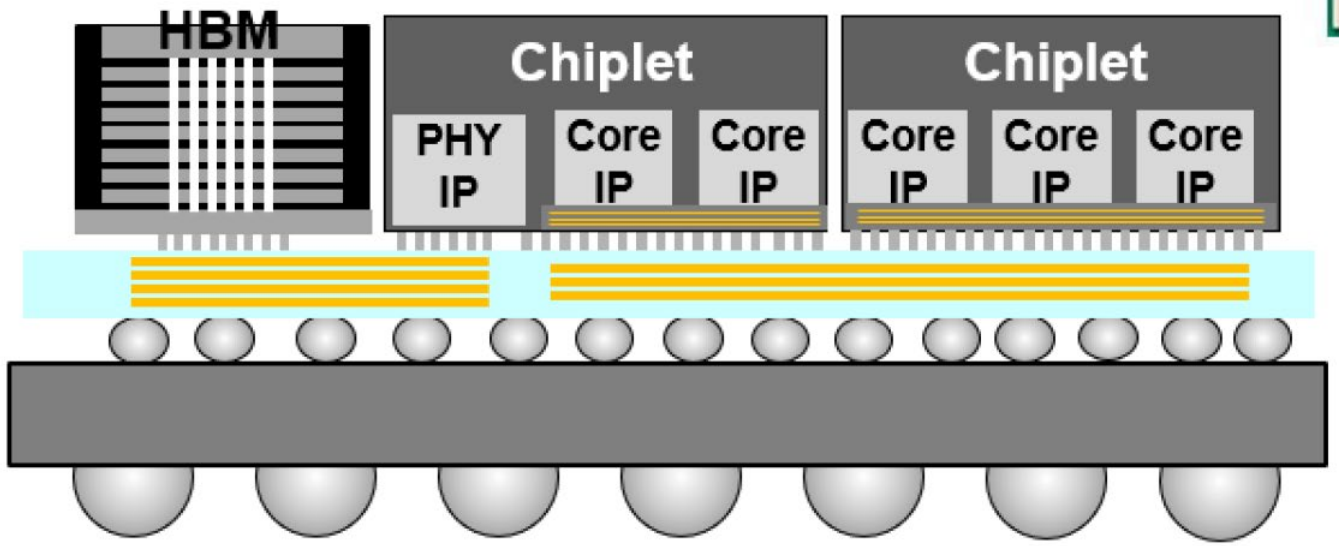
Packaging Processes

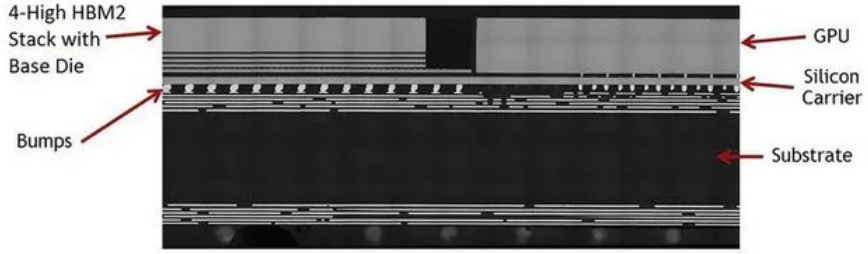
TSMC CoWoS

- As 2.5D package using RDL-based interposer CoWoS-R
- As 2.5D package using silicon-based interposer CoWoS-S





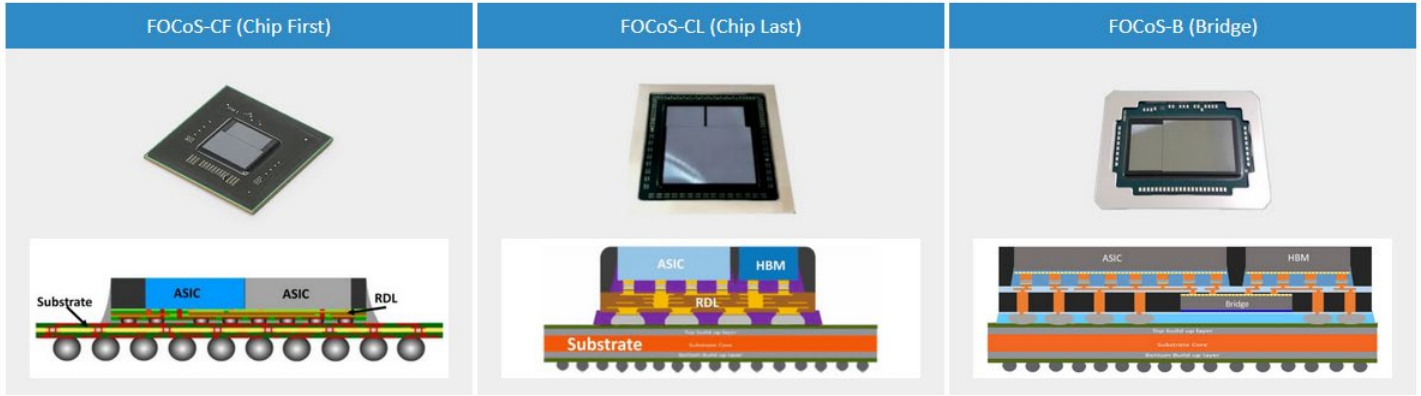


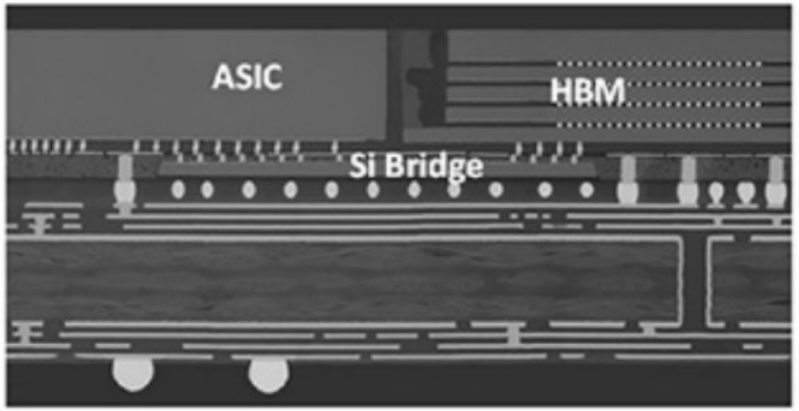


Packaging Processes

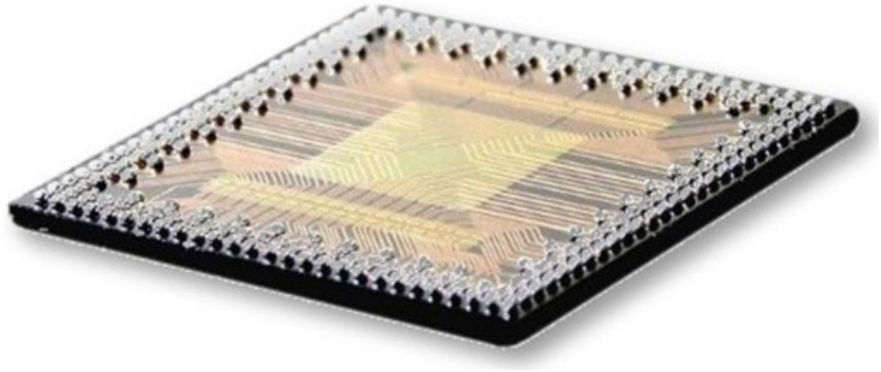
ASE

- FOCoS (Chip on Silicon)
  - Lower cost (vs. 2.5D)
  - Thinner package
  - Good electrical performance (shorter D2D connect)
  - High I/O counts (> 1000)
  - Time to market with existing Fan-Out/Flip



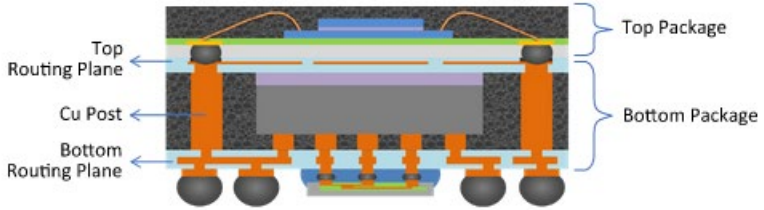


Packaging Processes

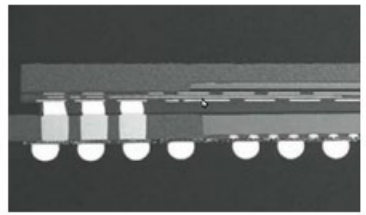


ASE

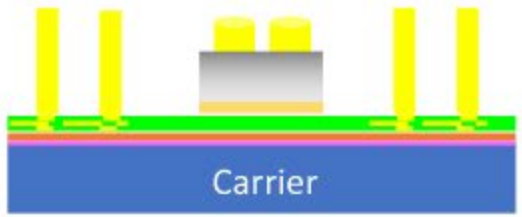
- FOPoP (Package on Package)
  - 3D integration of Memory device and Logic device
  - System size reduction and Board space savings
  - Memory architecture flexibility
  - Shorten signal routes
  - Compatible with current assembly technologies

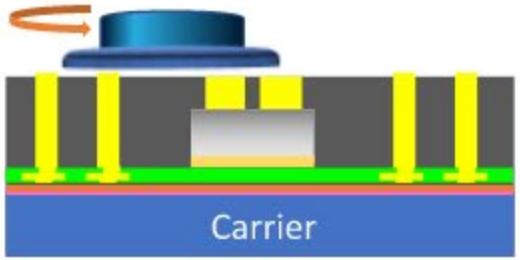


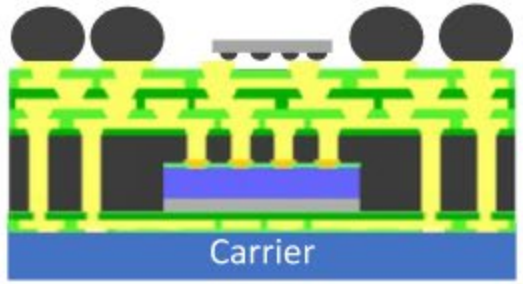
Fan-Out Package on Package (FOPoP)



Partial Cross-section view of FOPoP



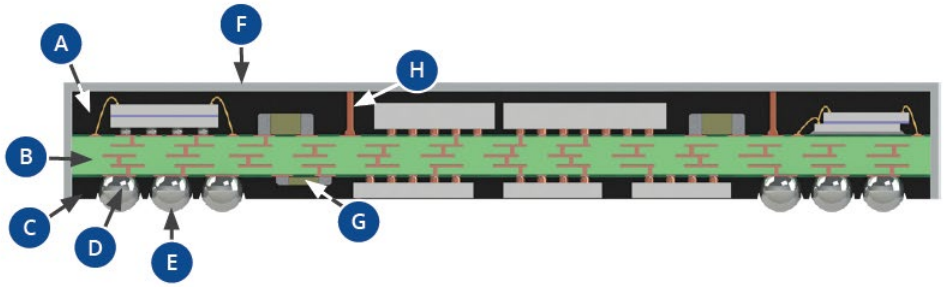




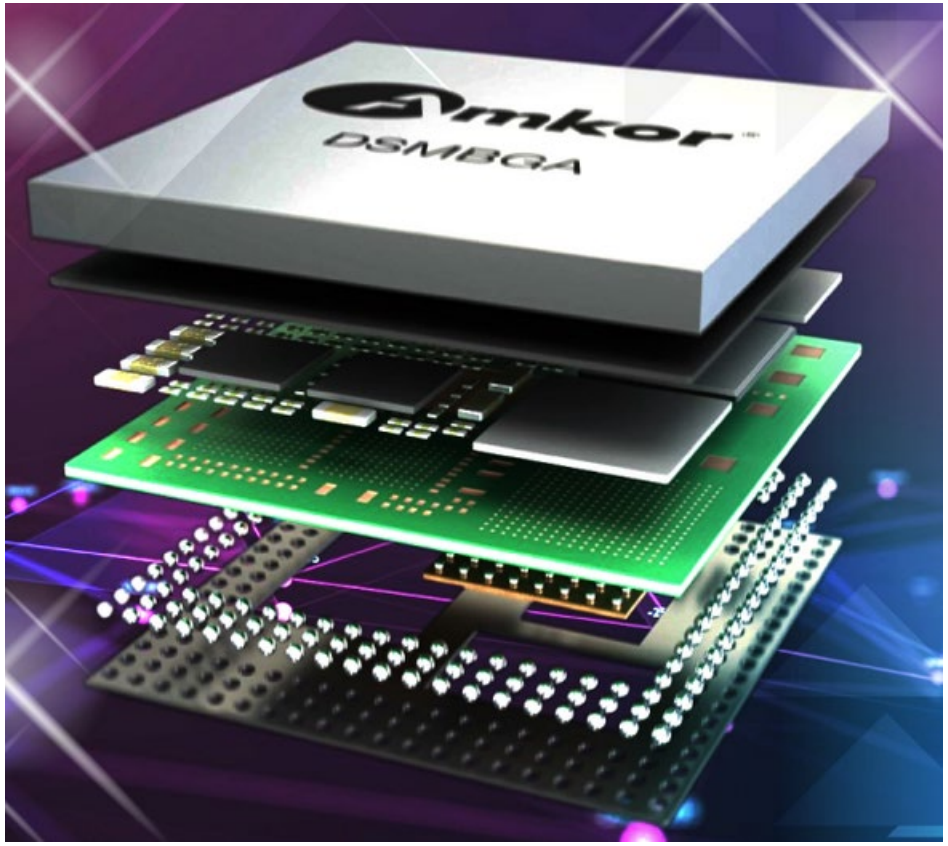
Packaging Processes

Amkor

- DSMBGA
  - Double-Sided Molded Ball Grid Array
  - Especially for RF front-end modules



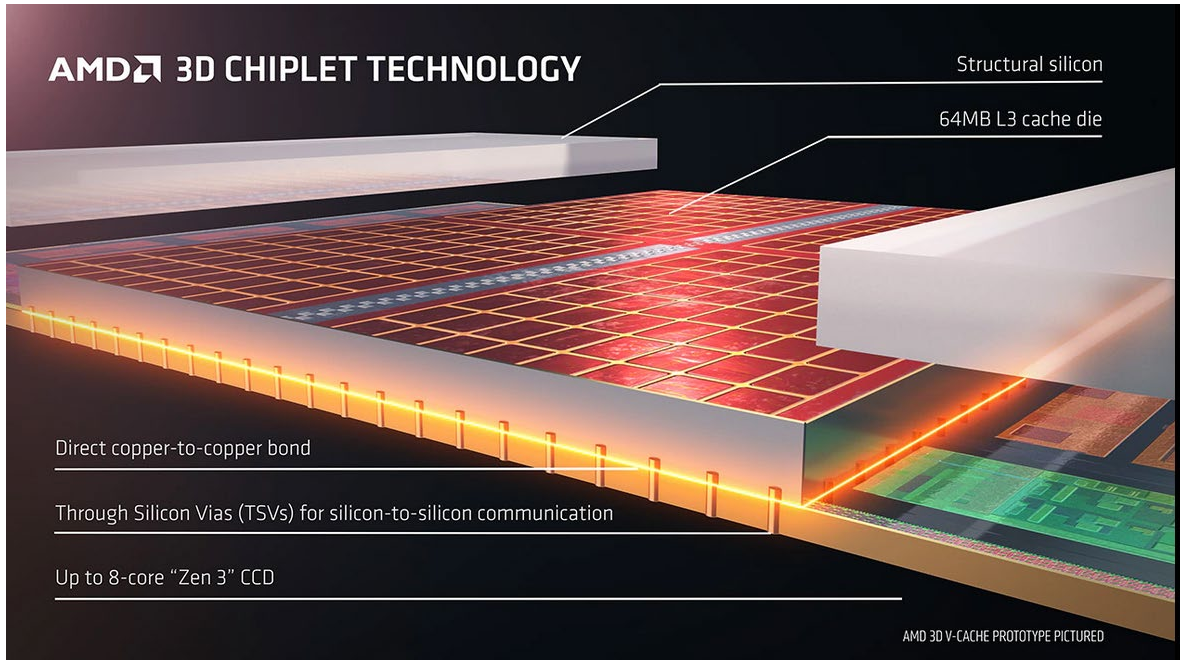
A Top mold (MUF)
B PCB (core, coreless)
C Bottom mold (MUF)
D Protruded BGA
E Laser ablation & reflow (protruded ball)
F 5 Side conformal shield
G Land side component
H Compartment shield (wire cage, wire fence, vertical wire)

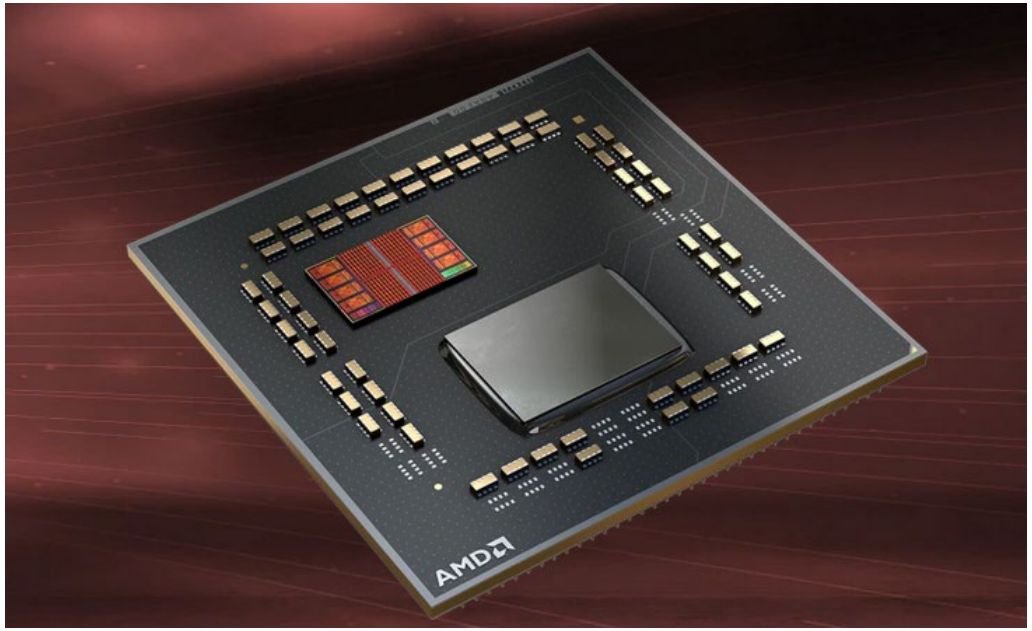


Packaging System Samples

AMD 3D V-Cache

- TSMC 7nm CPU combined with SRAM cache using chiplets and hybrid bonding
  - Minimum pitch at 9um

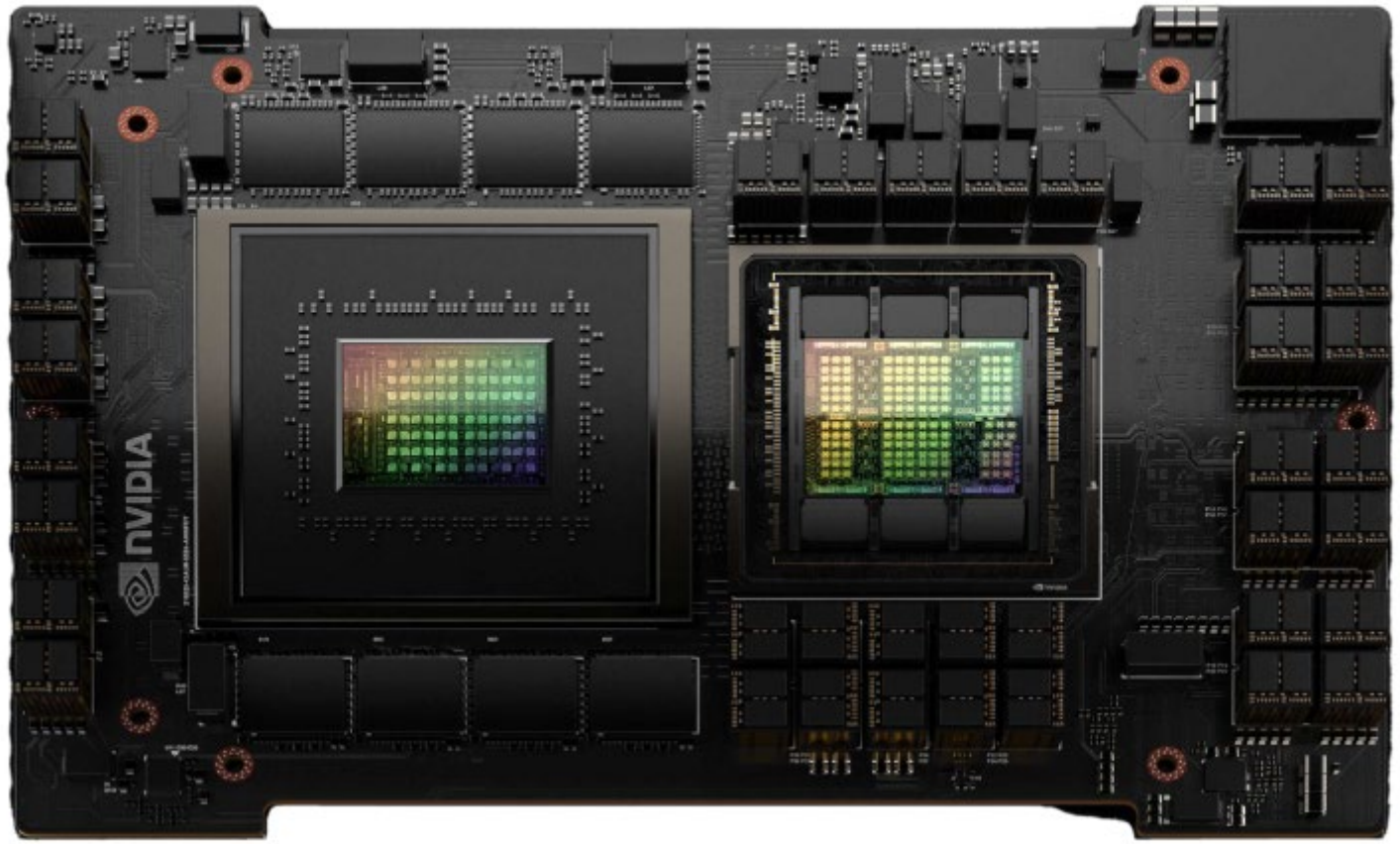




Packaging System Samples

Nvidia Grace Hopper

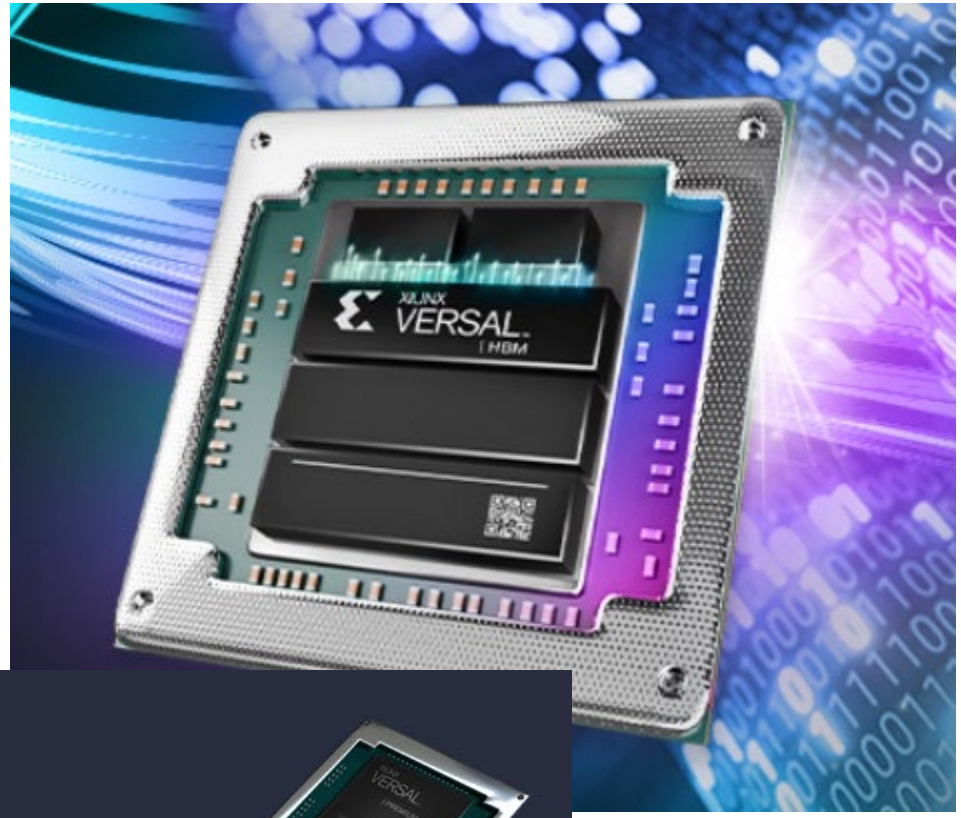
- 72 CPUs connected to 512GByte LPDDR5 memory
- 128 GPUs connected to 96GGbyte HBM
- Packaging view
  - CPUs and GPUs on separate interposers
  - Package substrate for complete system

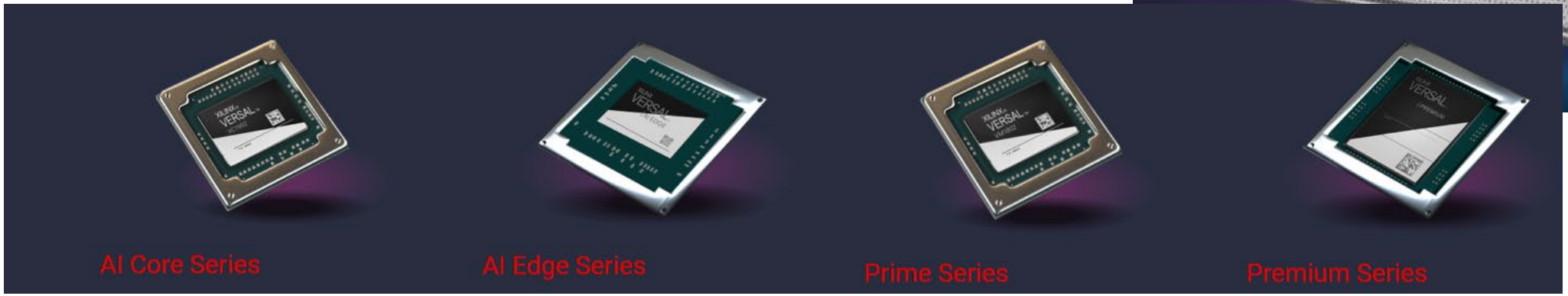


Packaging System Samples

Xilinx VERSAL

- Adaptive Compute Acceleration Plattform (ACAP)
- With leading edge VERSAT HBM system
- Based on stacked silicon integration

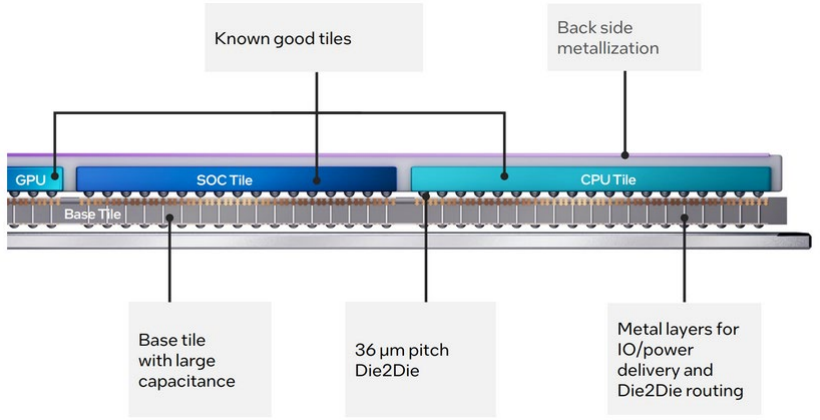


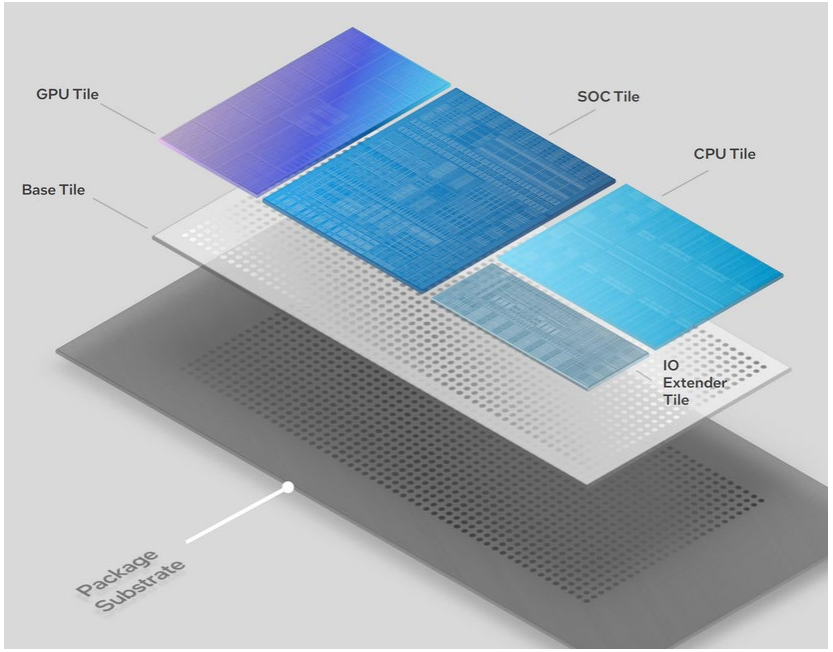


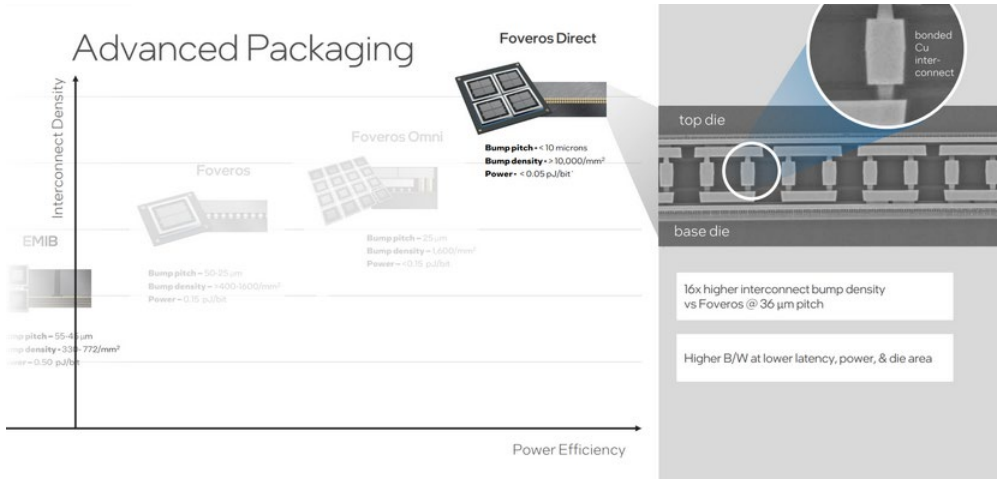
Packaging System Samples

Intel Meteor Lake

- Using Foveros Direct (Cu-Cu hybrid Bond)



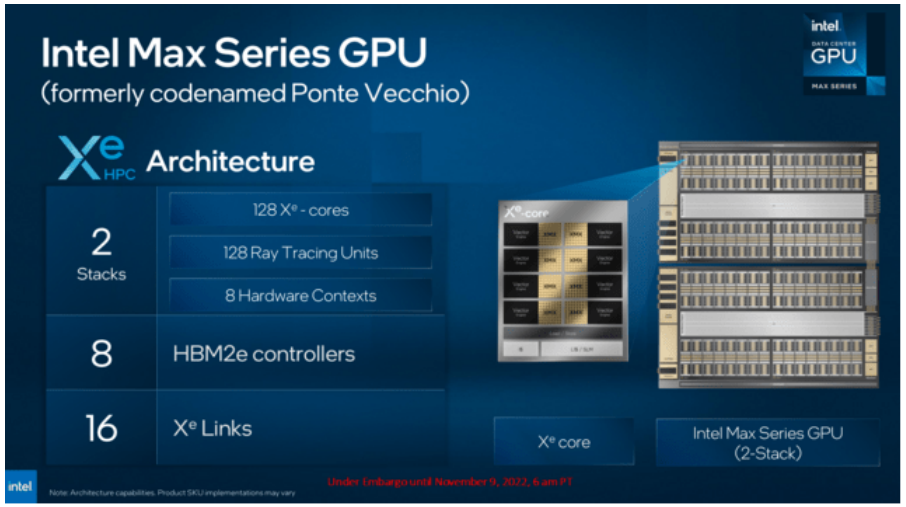


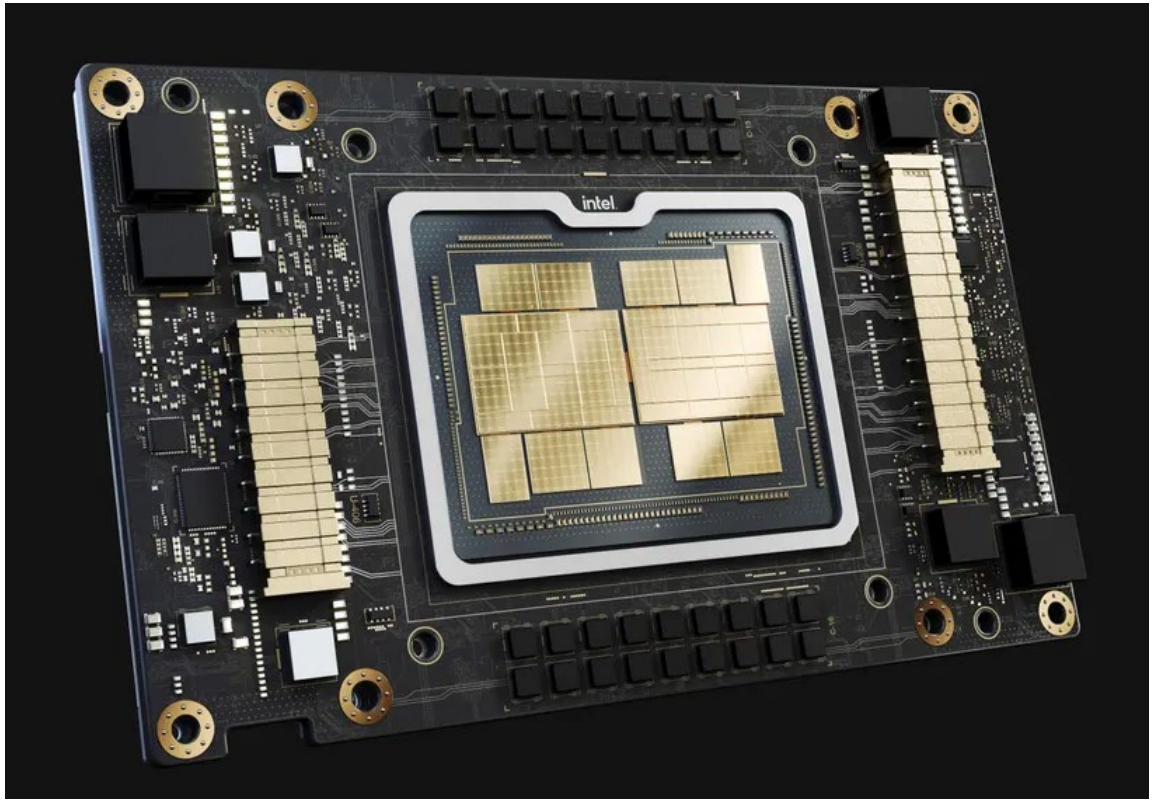


Packaging System Samples

Intel Ponte Vecchio

- 47 chiplets with a sum of 100 billion transistors
- Combined 2.5D and 3D technology
- 3100mm² of silicon
- Using Co-EMIB
- Purpose: for super computer in three variants (with 300, 450 and even 600 Watt)



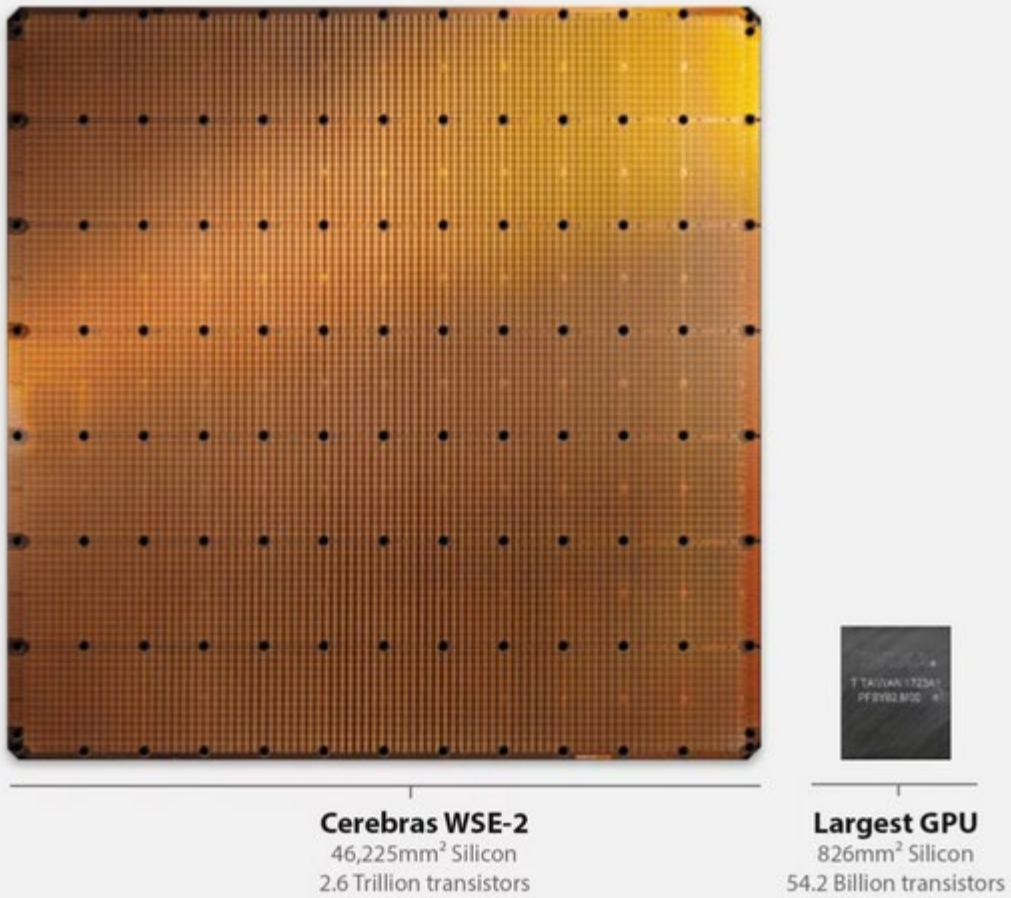


Packaging System Samples

Large Scale ICs

- Example from Cerebras
  - Almost wafer-scale
  - 850,000 cores
  - Bandwidth 220 Pb/s

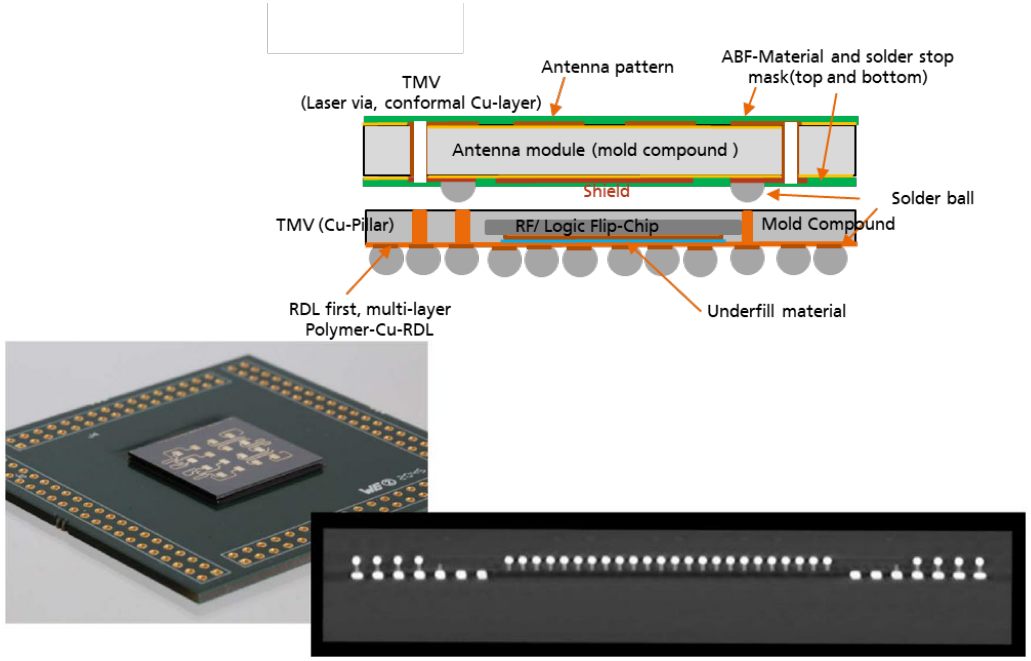
	WSE-2	A100	Cerebras Advantage
Chip Size	46,225 mm2	826 mm2	56 X
Cores	850,000	6912 + 432	123X
On-chip memory	40 Gigabytes	40 Megabytes	1,000 X
Memory bandwidth	20 Petabytes/sec	1.6 Terabytes/sec	12,733 X
Fabric bandwidth	220 Petabits/sec	4.8 Terabits/sec	45,833 X

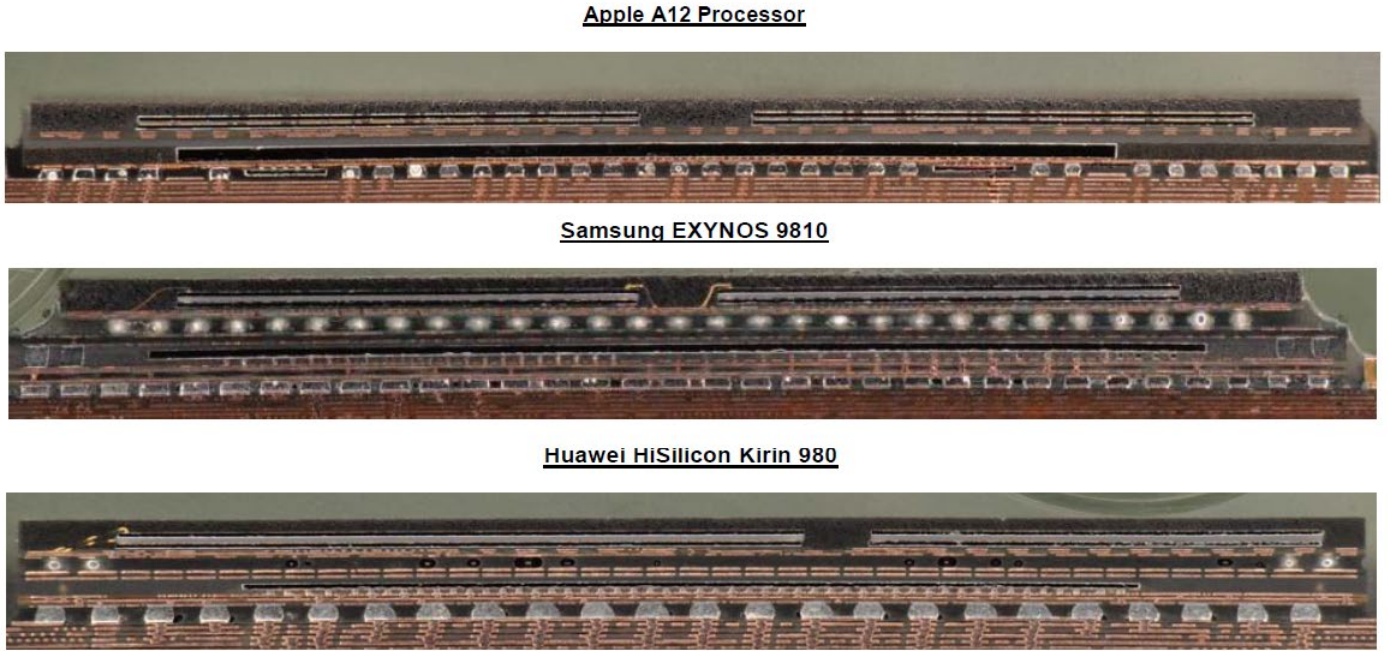


Packaging System Samples

Package-on-Package

- For instance for RF applications

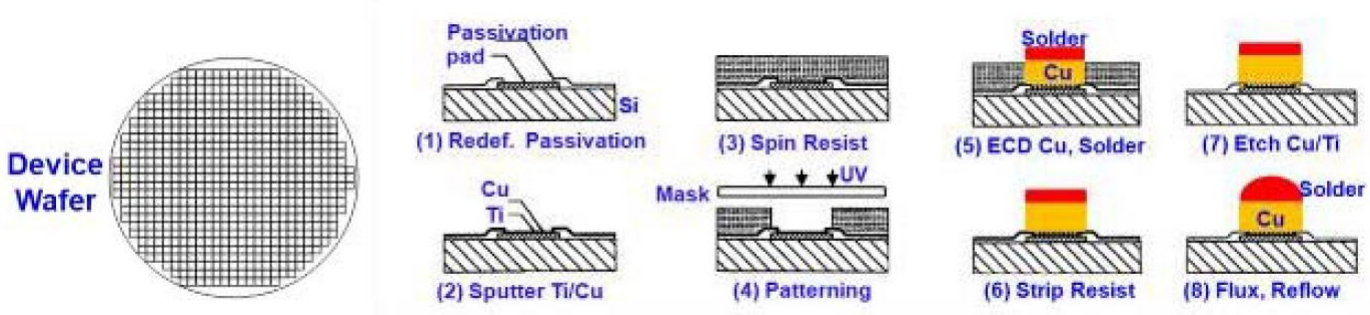




Recent Advances

Bumping

- Almost all advanced packages are related to bumped devices or hybrid bonding
- Different options, like Au or Ni bumps, Cu studs, solder bumps
- C4 (controlled collapse chip connection) most common one today
- C2 (chip connection), like copper pillars for very high-density and fine pitch



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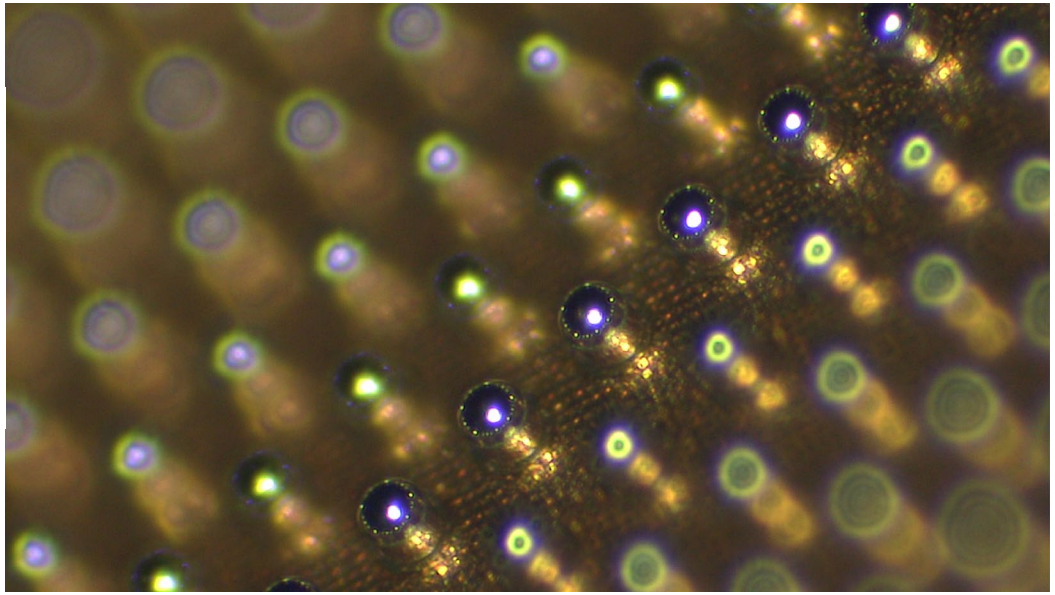
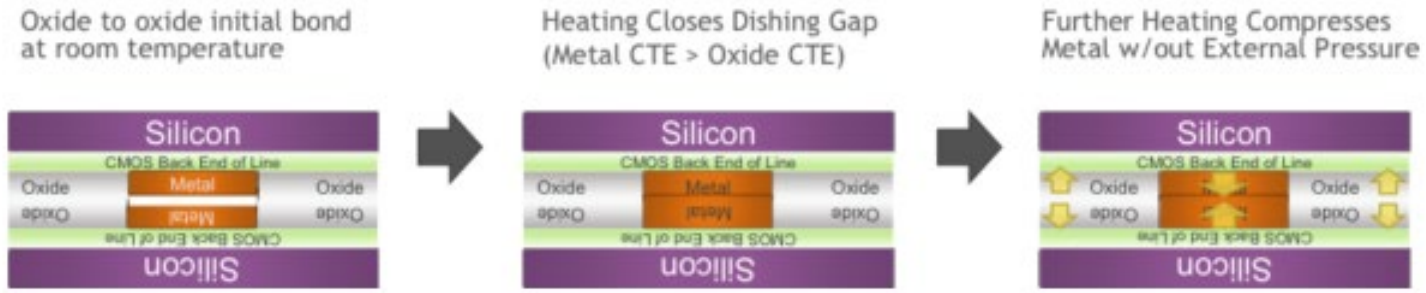
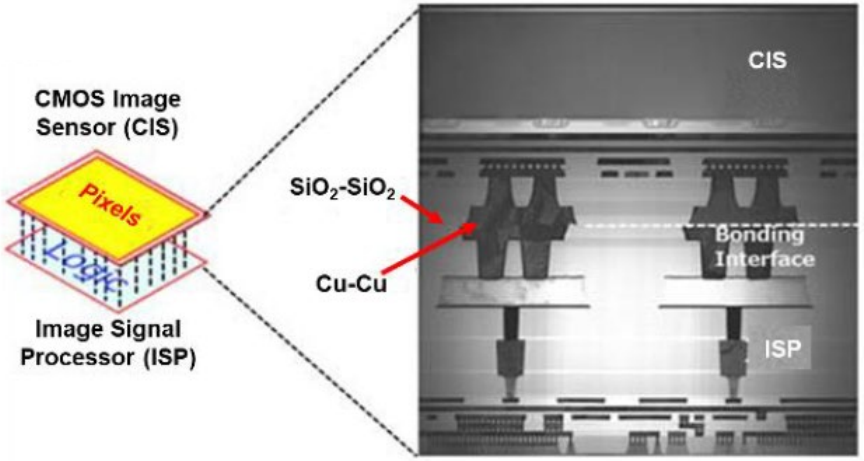


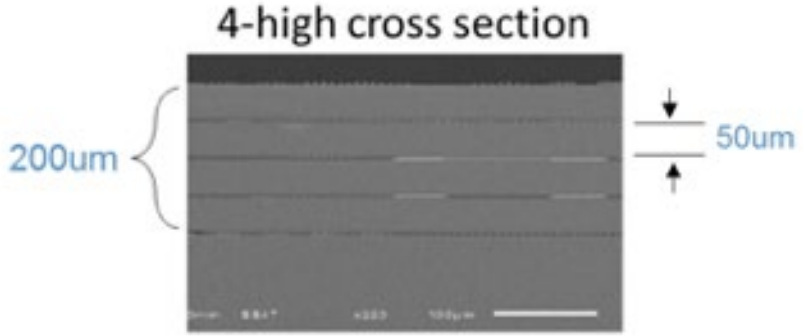
Recent Advances

Hybrid Bonding

- Also known as direct bond interconnect (DBI)
- Either Wafer2Wafer, Die2Wafer or Die2Die
- Optimizing CMP condition main factor to create suitable surface
- First image sensors using W2W
- Pitch currently 1-2u for W2W and ~10u for D2X



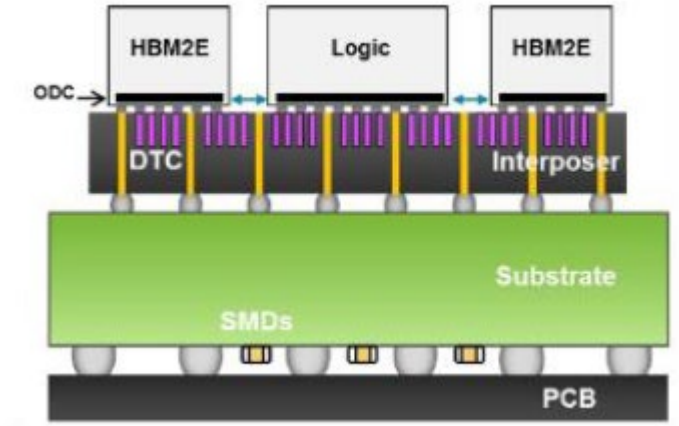




Recent Advances

Interposer or 2.5D Integration

- Either RDL interposer or silicon interposer depending on system requirements
- High volume expected to be on silicon interposer due to better performance but higher cost (especially on design side)
- Organic or RDL interposer expected more in mid-volume due to more flexibility and easier design usage (in terms of signal and power integrity)
- Supported by many vendors
- Arising option to embedded capacitors as MiM or deep-trench capacitor to allow decoupling or basic capacitance function, that are more expensive on ICs
- Expected almost-passive interposers (with very few active parts on specialized technologies) in upcoming years

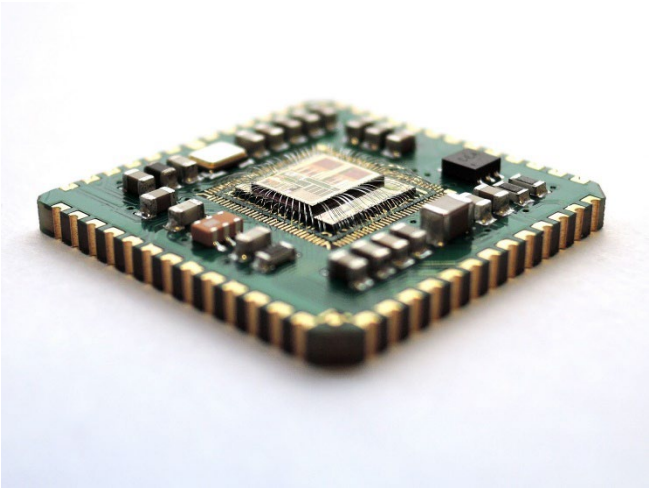


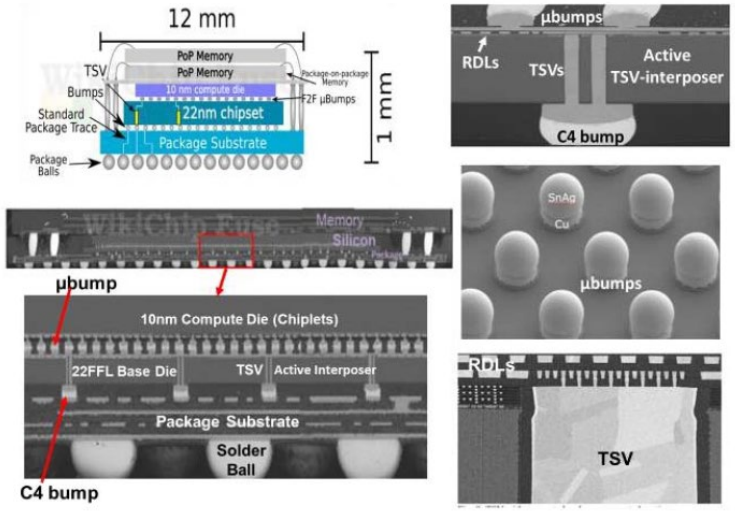
https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9684894

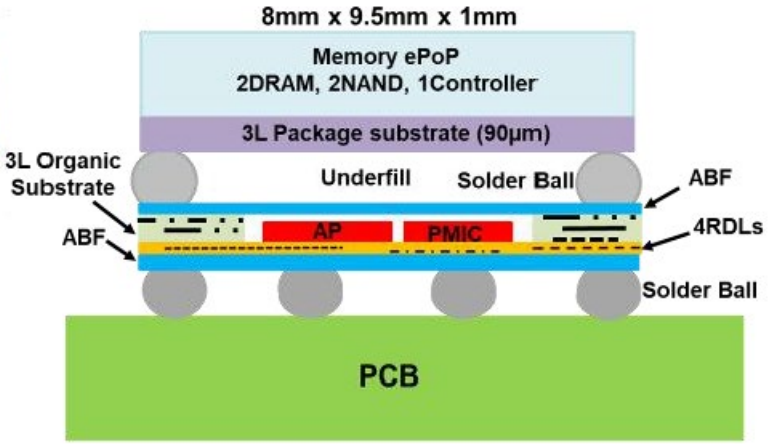
Recent Advances

3D Integration

- Multiple variants
  - Form stacked dies using wirebonds
  - Package-on-Package (e.g. Smartwatch)
  - 3D IC Stacking



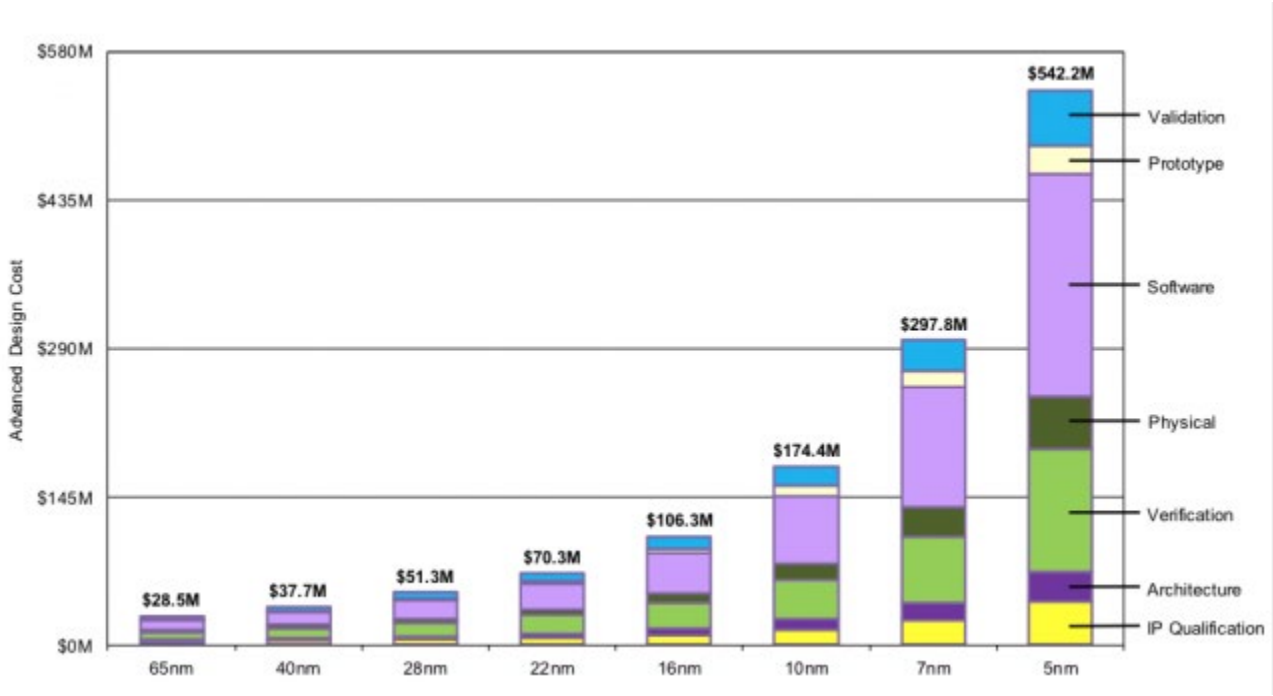




Recent Advances

Chiplets

- Cost perspective
  - Development cost show large rise with going to smaller nodes
  - Chiplets are one way to reduce this cost by not transferring all functionality to smaller nodes

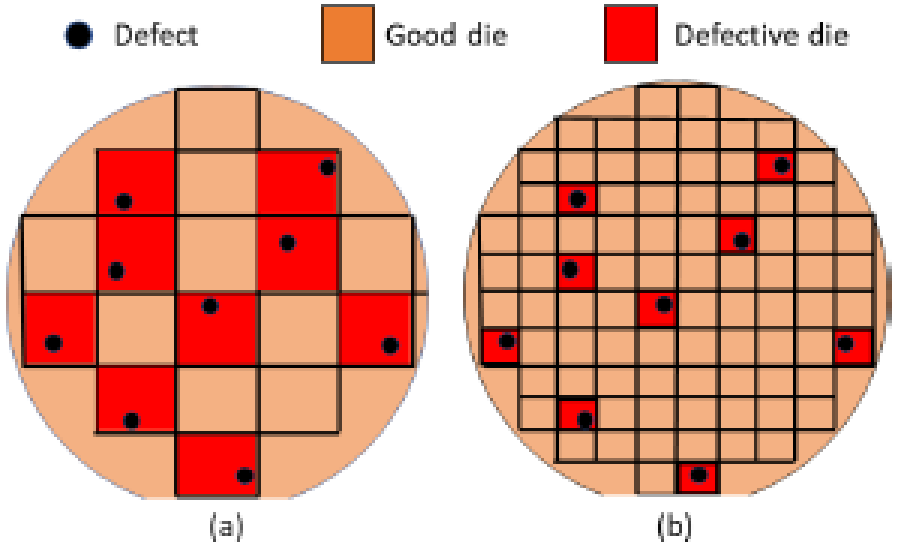


https://www.extremetech.com/computing/272096-3nm-process-node

Recent Advances

Chiplets

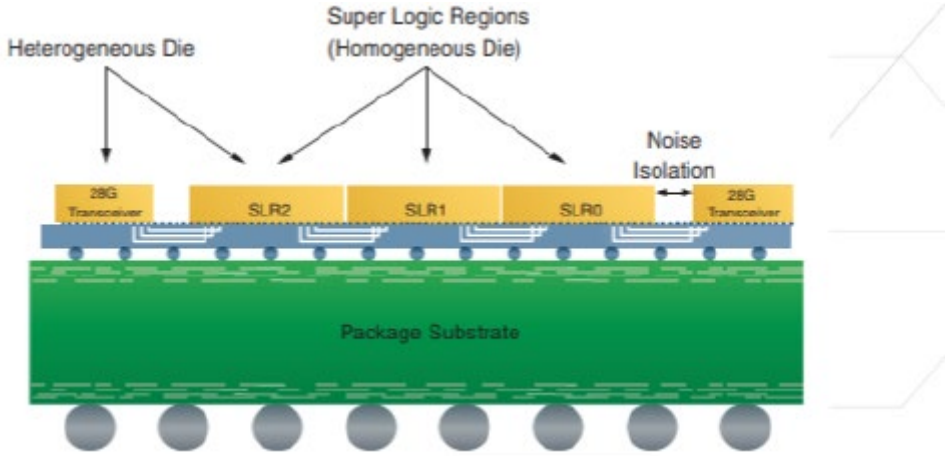
- Yield perspective
  - Currently most defective dies are coming from spot defects
  - Spot defects have a known probability for known processes
  - Large SoC suffer more from spot defects
  - Therefore yield per wafer could be increased by reducing die size



Recent Advances

Chiplets

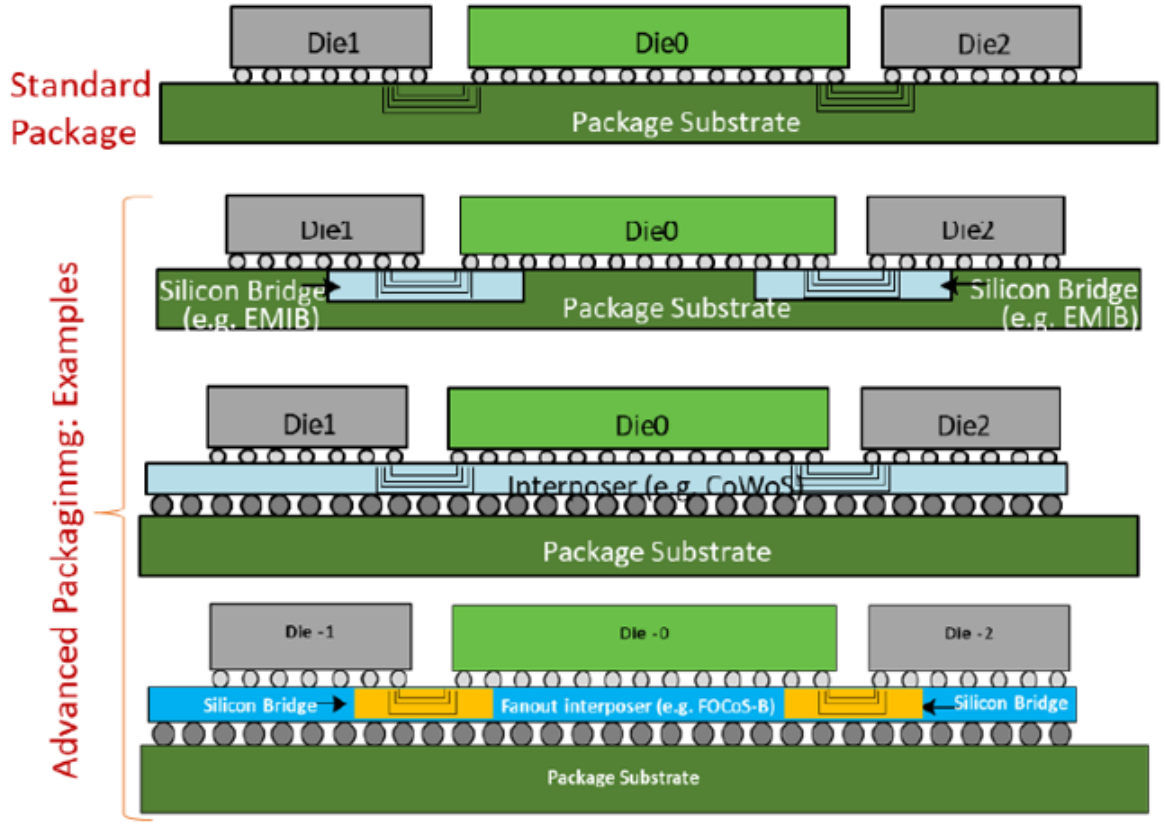
- Packaging perspective
  - Chiplets could gain advantage by all the available packaging options presented
  - Many available options
    ->many potential system solutions
    -> new applications enabled
  - Xilinx was one of the first due to regularity of FPGAs and therefore good scalability
  - Multi-core CPUs are to follow
  - Separation of core and memory



Recent Advances

Chiplets

- Interoperability
  - Most current system are using components from one vendor
  - To combine small functional blocks from different vendors, standardized interfaces are required
  - Like UCIe driven by Intel
  - Bunch-of-Wires or Open HBI
  - Most of the proposed interfaces are scalable in terms of IC pitch and package technology used

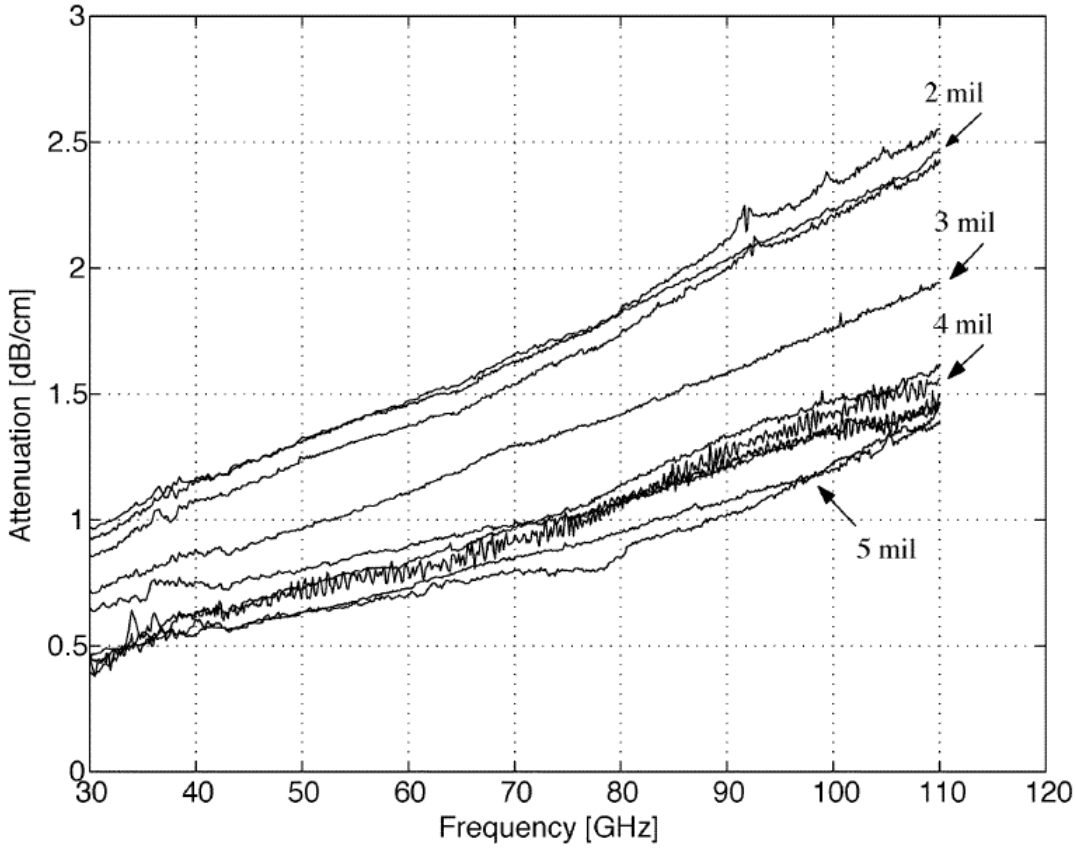


Universal Chiplet Interconnect Express (UCIe)®: Building an open chiplet ecosystem

Recent Advances

Materials

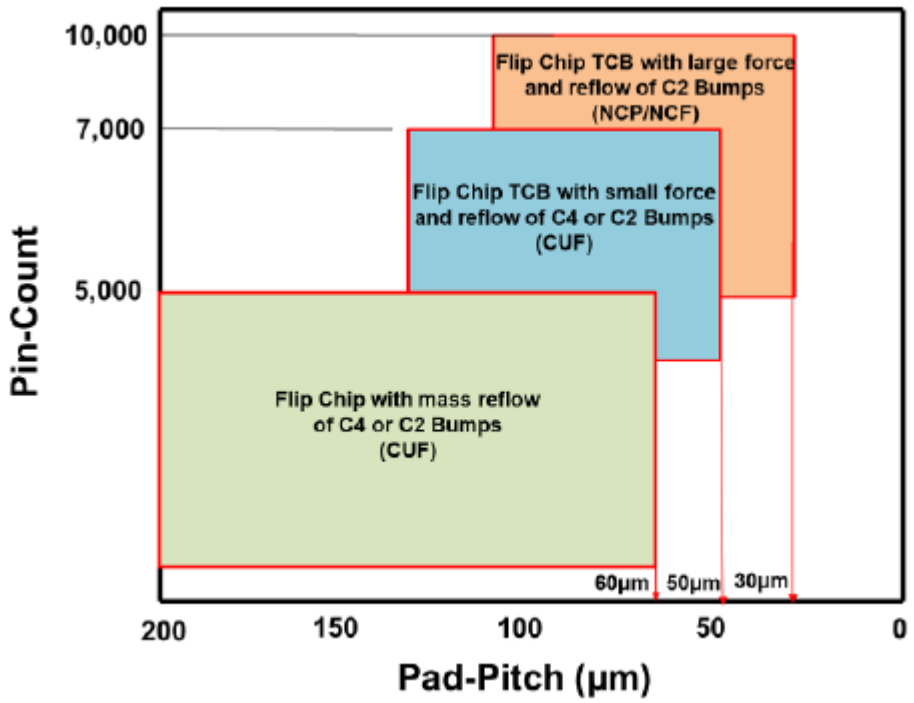
- Package developments are also related to material development
- One main driver is higher speed for signal transmission and wireless applications
- This brings the demand for materials with low-loss dissipations factor and low dielectric constant like liquid crystal polymer (LCP)



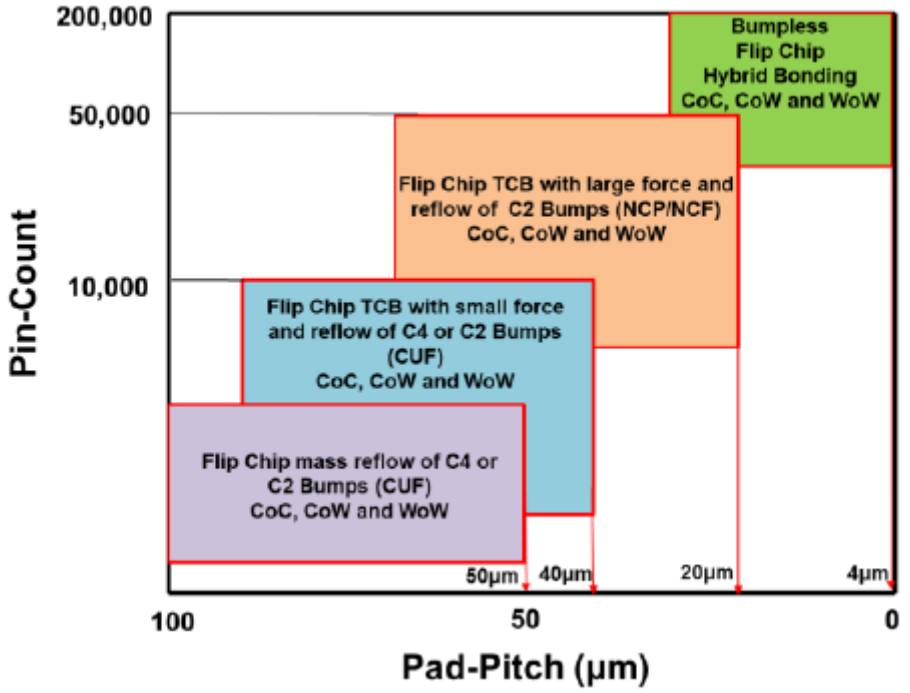
Recent Advances

Roadmap

- For organic substrates



for silicon-based integration



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Summary

- Packaging is a market with rising market size
- Large amount of investments ongoing to create capabilities and volume
- Many packaging solutions available for mass production
- Diversity and many options available
- Many of the solutions are expected to be apparent the next years
- No technology foreseen to rule out all other

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