



January 24 - 26, 2023  
DoubleTree by Hilton San Jose  
ChiplletSummit.com

# Chipllet Market Update





INTRODUCING YOLE GROUP

WHAT CONSTITUTES A “CHIPLET”

CREATING OPPORTUNITIES

SIZING THE MARKET FOR CHIPLET PLATFORMS

END SYSTEMS MOST RELEVANT FOR CHIPLETS

BREAKING INTO THE MARKET

EXAMPLES IN THE MARKET TODAY

SIZING UP THE PROCESSOR MARKET FOR CHIPLET PLATFORMS

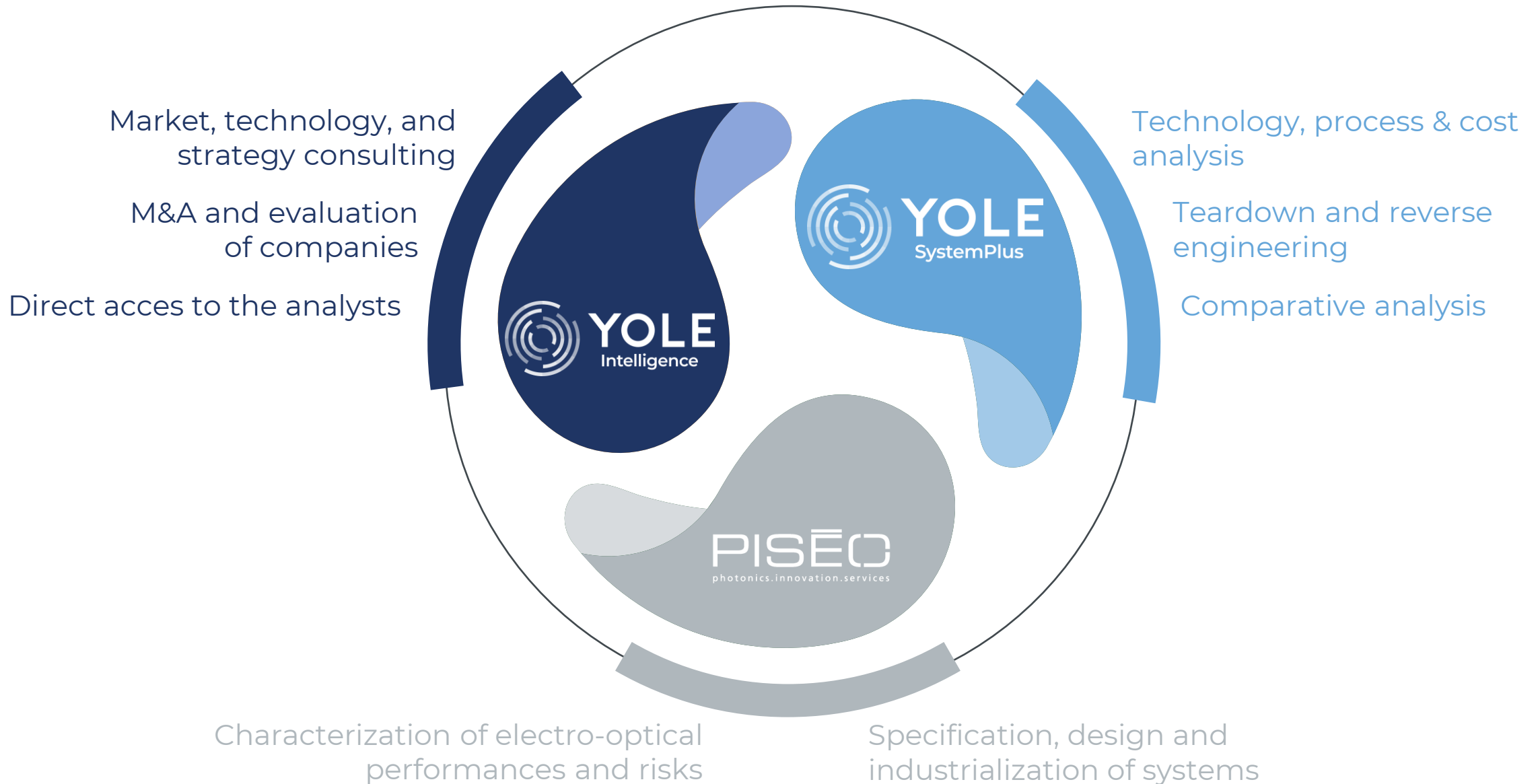
CHIPLET MARKET LONG TERM

CHIPLETS FROM A MANUFACTURING PERSPECTIVE

MARKET DYNAMICS

ON THE CUSP OF THE NEXT EVOLUTIONARY STEP FOR IC INTEGRATION

# YOLE GROUP'S MAJOR ACTIVITIES PER ENTITY



# FIELDS OF EXPERTISE COVERING THE SEMICONDUCTOR INDUSTRY



- Semiconductor Packaging
- Semiconductor Manufacturing
- Memory
- Computing and Software

- Photonics & Lighting
- Imaging
- Sensing & Actuating
- Display



- Radio Frequency
- Compound Semiconductors
- Power Electronics
- Batteries

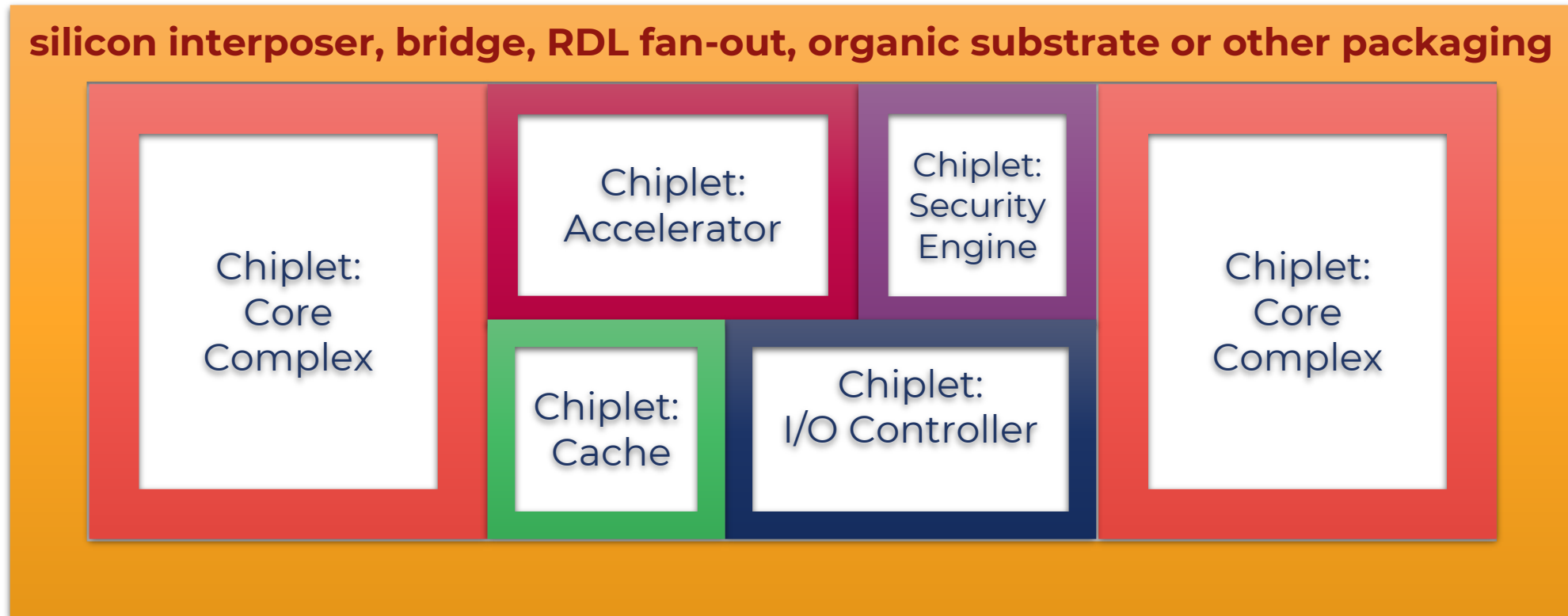


- Electronic Systems
- Emerging Technologies



## Yole Group definition of a Chiplet

A Chiplet is a discretely manufactured physical piece of hardware designed to be integrated in the manufacture of a heterogeneous integrated circuit so that the completed IC is functionally equal to or greater than that of a complete system designed on a single monolithic die. The chiplet is physically or economically optimized to perform a specific functional and interoperable subset of the complete heterogeneous system IC.





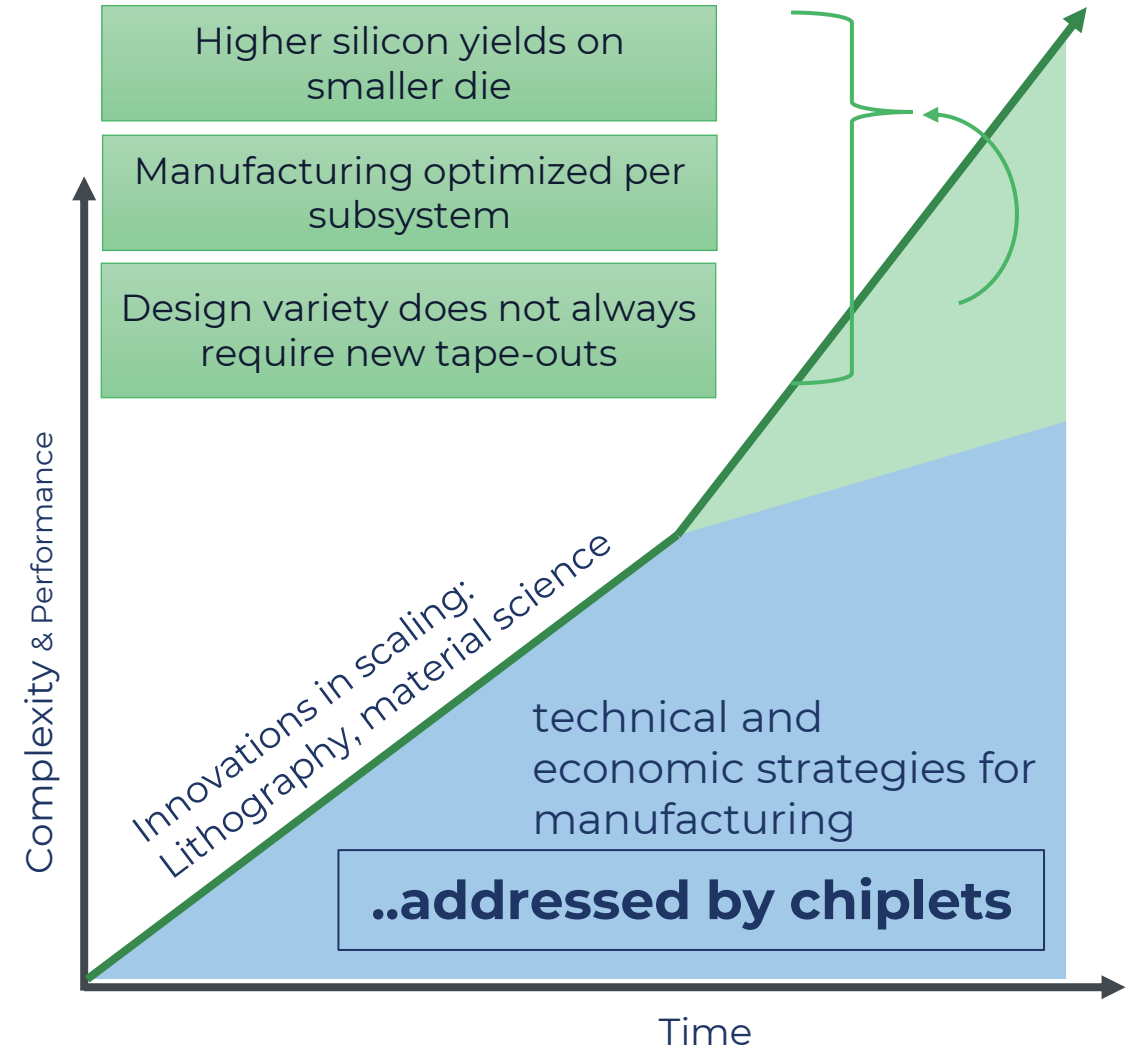
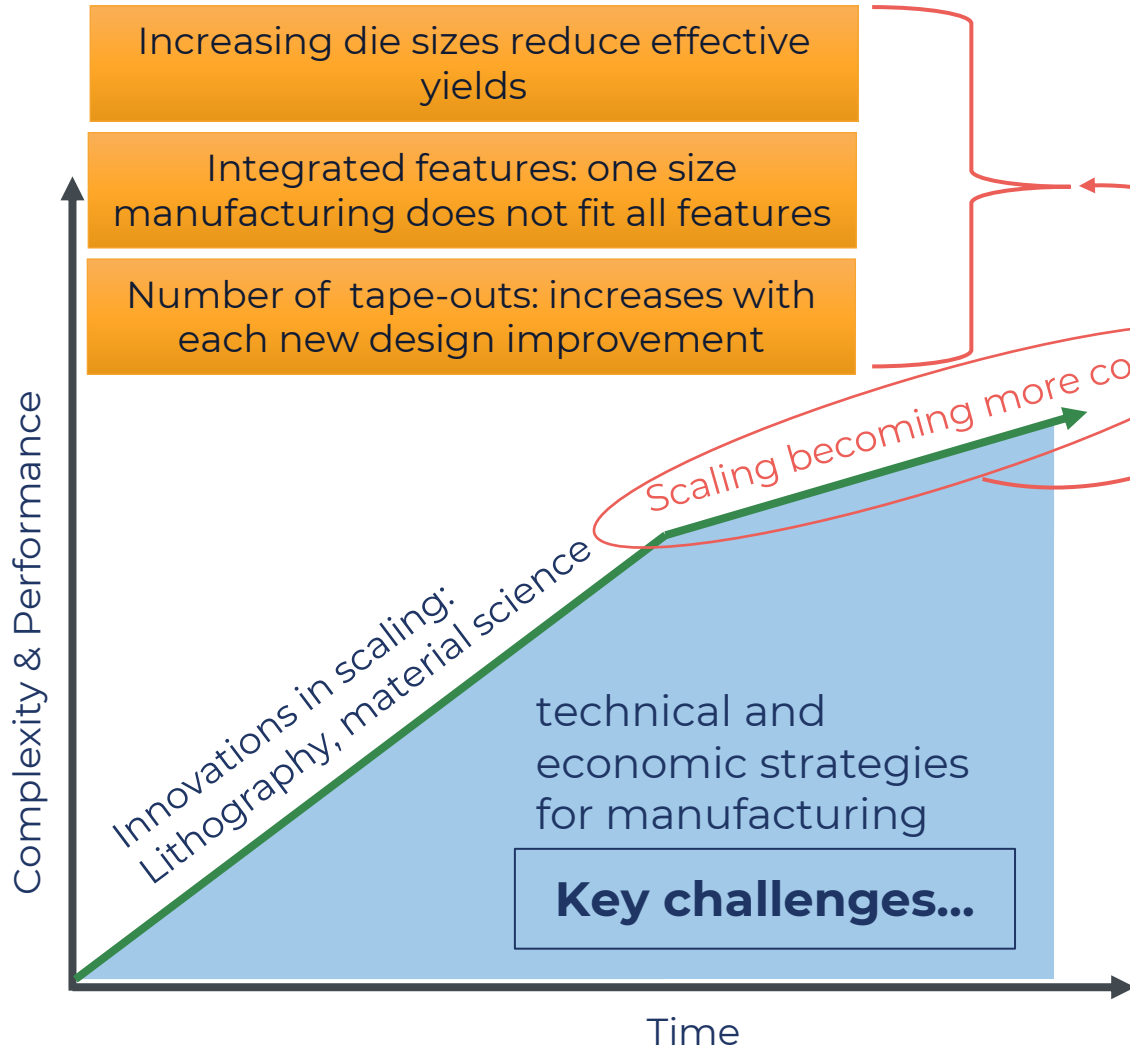
## Some key characteristics

- **Chiplet is not a technical specification**, it is a general term in much the same way as processor, accelerator, memory, analog IC, logic IC, and other terms are used to describe a useful collection of attributes. This enables a common understanding of an IC’s purpose and characteristics.
- **The term chiplet is simply a semantic tool** used to describe a new feature of advanced packaging techniques. Integration has evolved from device, to board, to module, and finally to chip-level integration. The key purpose in the development of this term is to focus on the collective physical and logical characteristics inherent in developing this manufacturing strategy at market scale.
- **A chiplet is commonly manufactured in a process suitable for the physical and economical attributes for its function.** This includes wafer characteristics, process geometry, material, size, cost, and other attributes. The chiplet platform can be suitable for the integration of application processor cores, coprocessors, sensors, transceivers, memory, storage, interfaces, and other subsystems. It could include something other than a silicon-based die so long as its function becomes intrinsic to the final system-level IC. In theory, chiplets could be integrated in stages such that two or more highly interrelated functions combined to make a larger chiplet.
- **The term chiplet is currently only applied when the die is integrated into an IC constituting a complete heterogeneous system IC.** Most ICs identified as chiplets will be uniquely suitable to SoCs or SiPs, including those functioning as microprocessors, applications processors, field programmable gate arrays, coprocessors, and similar heterogeneous processors. However, no design restriction is assumed to say that a physical product could not also perform its function discretely as a companion chip on a board or module. The term chiplet does not apply to the discrete use case, only the integrated IC use case. The value of the term is in focusing on the integration processes (before and after integration), high-end die-to-die communications, physical and logical restrictions, and other characteristics required of a subsystem in a system IC comparable to a monolithic die.

# POSSIBILITIES ARE EXPANDED BY CHIPLETS, CREATING OPPORTUNITIES FOR NEW MARKETS



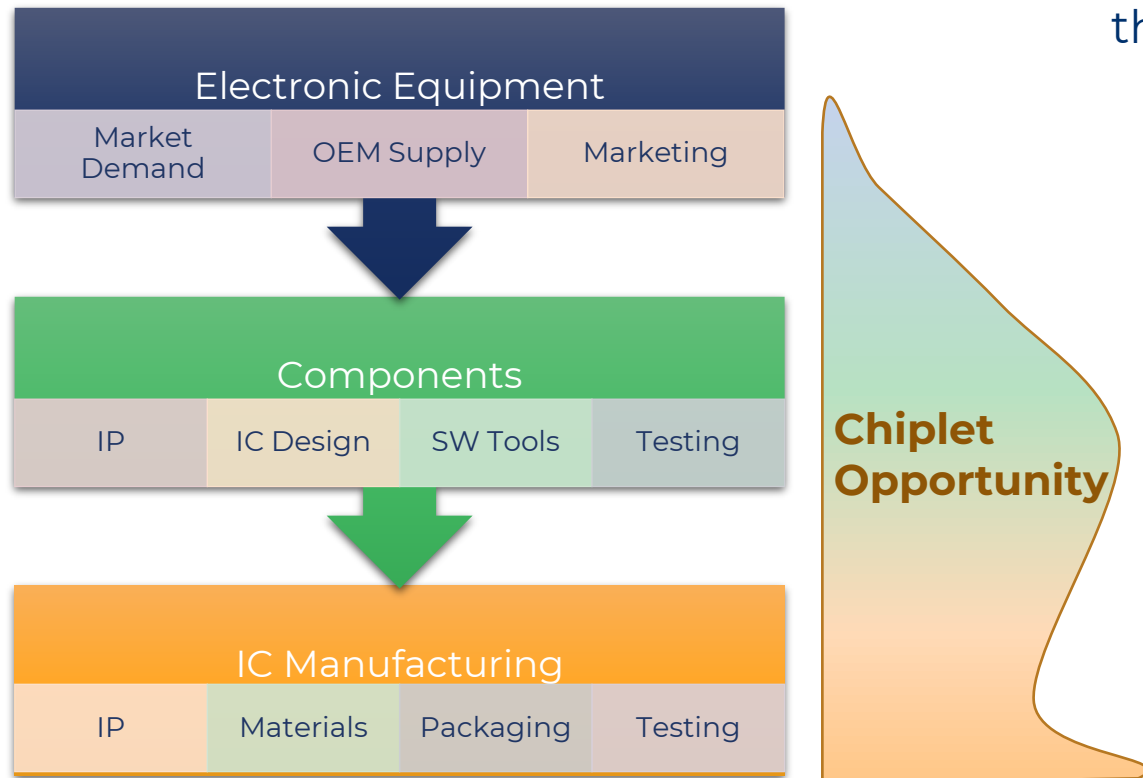
Enabled by chiplet advanced packaging and interconnect techniques, IP, and standardization



# HOW WE ARE TREATING CHIPLETS FOR THE PURPOSES OF MARKET SIZING



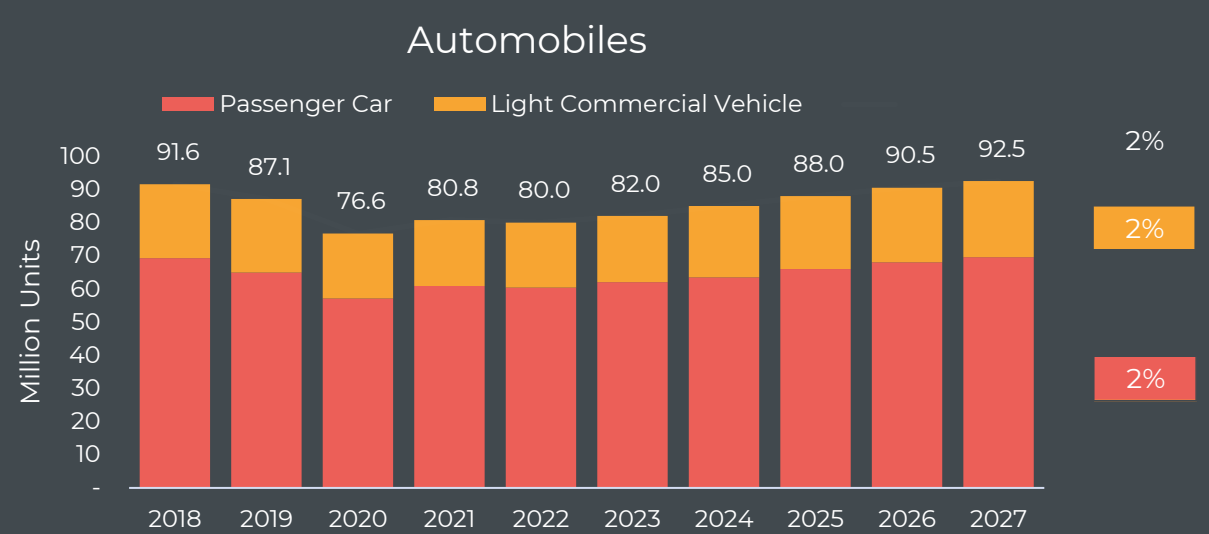
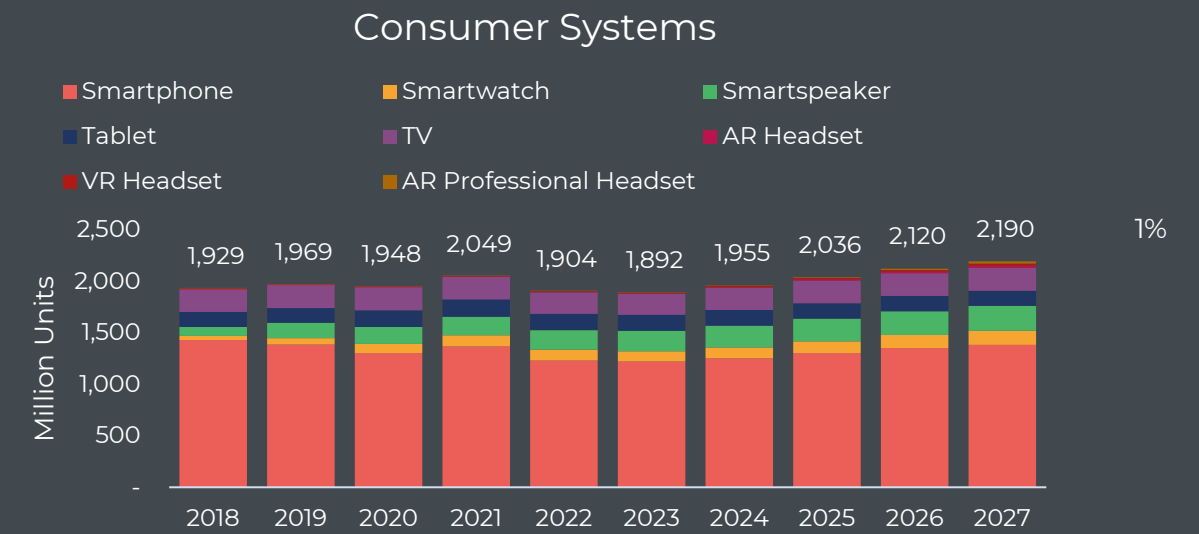
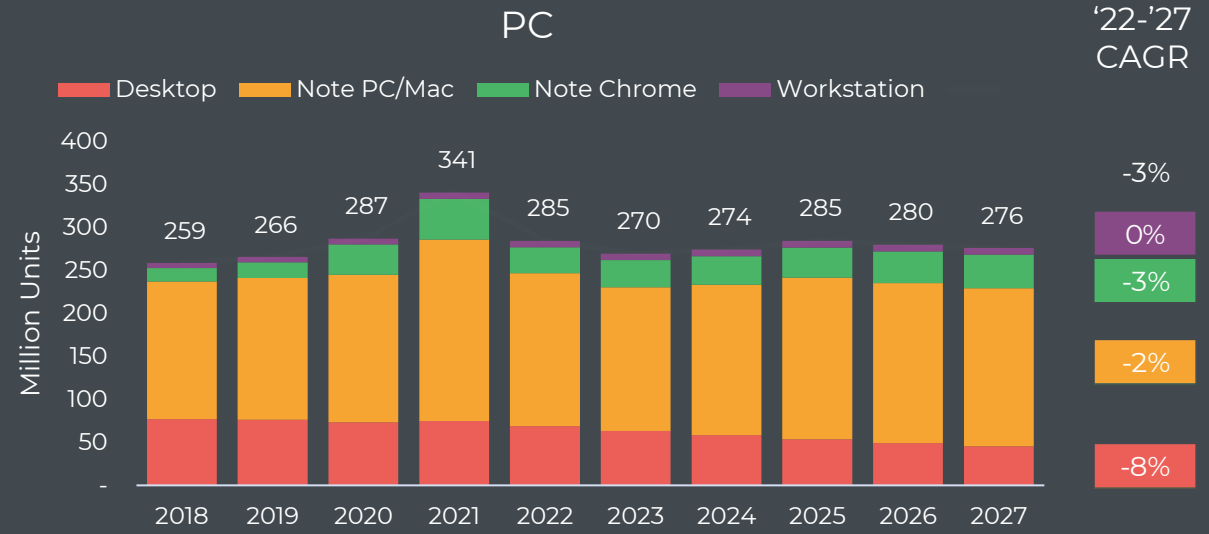
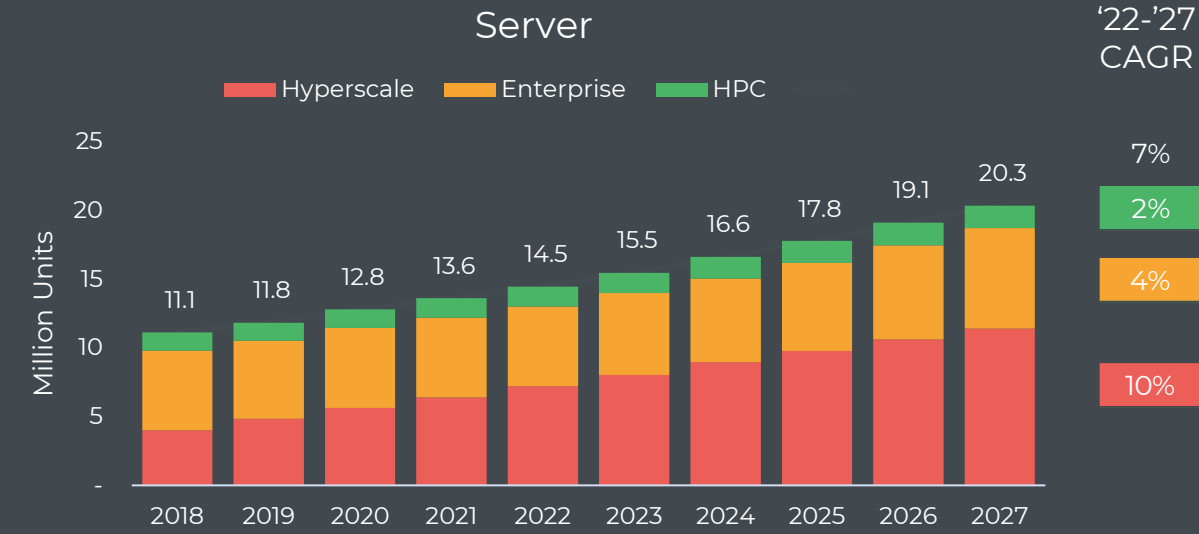
Yole Intelligence tracks electronic equipment markets, the component supply chain and semiconductor manufacturing. By sizing these markets and monitoring the history, supply and demand, barriers and driving technologies, we are well placed to approximate the value of the chiplet market. In addition to the tracked data, Yole System Plus provides teardown services to closely examine the results of the advanced packaging technique as we will share in this presentation.



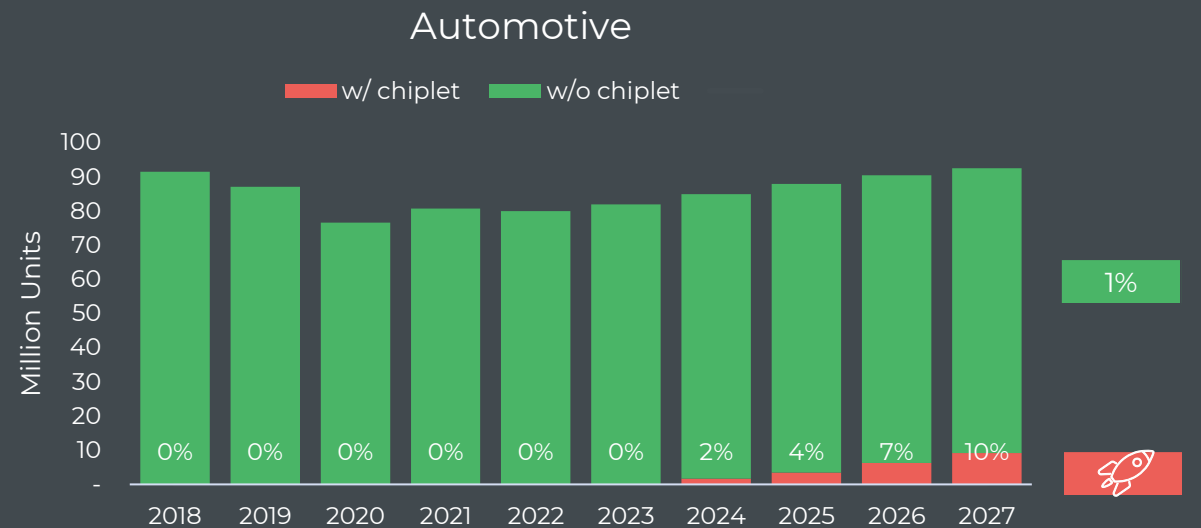
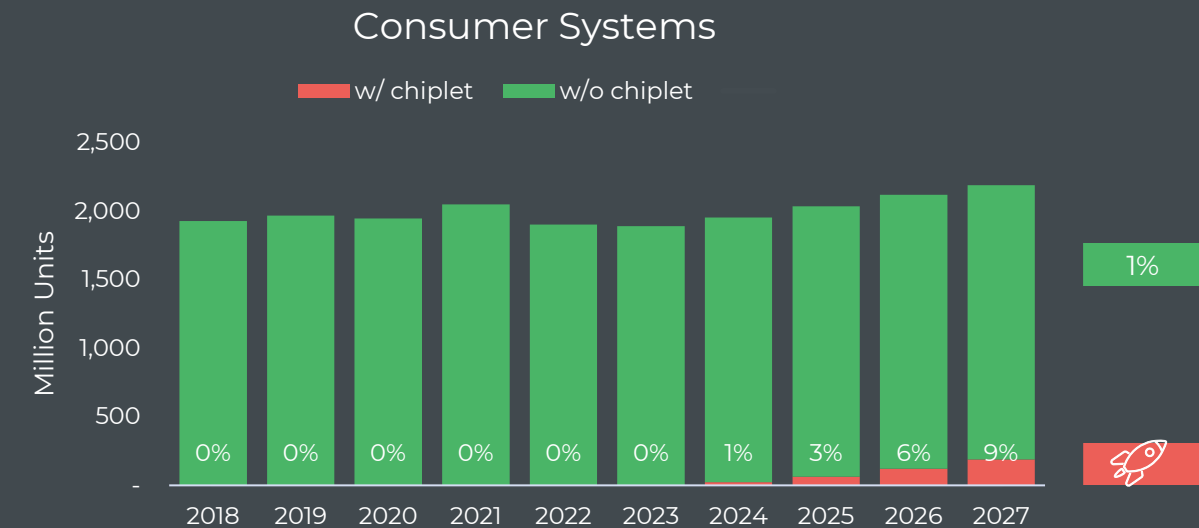
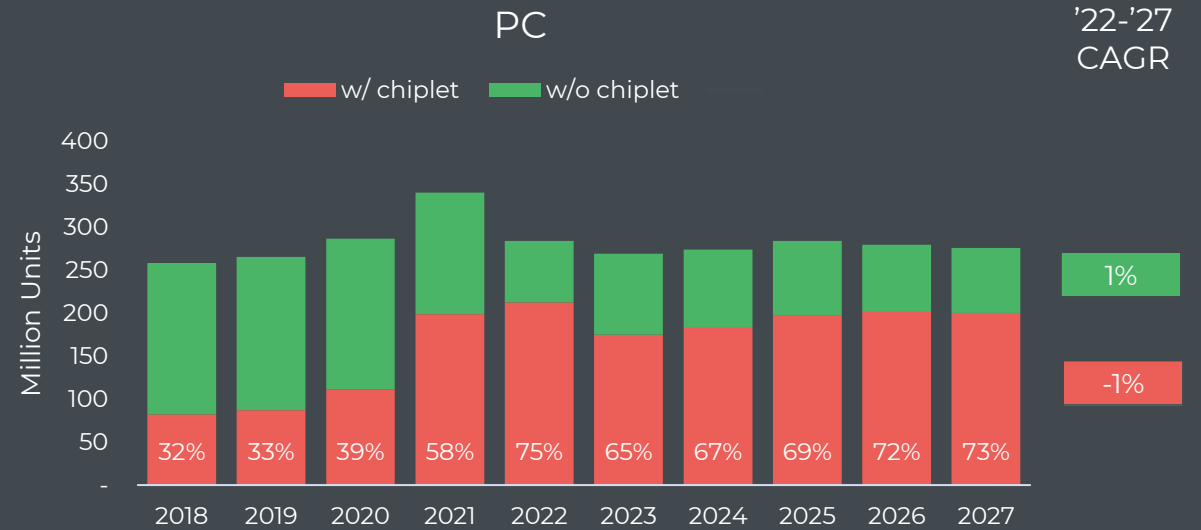
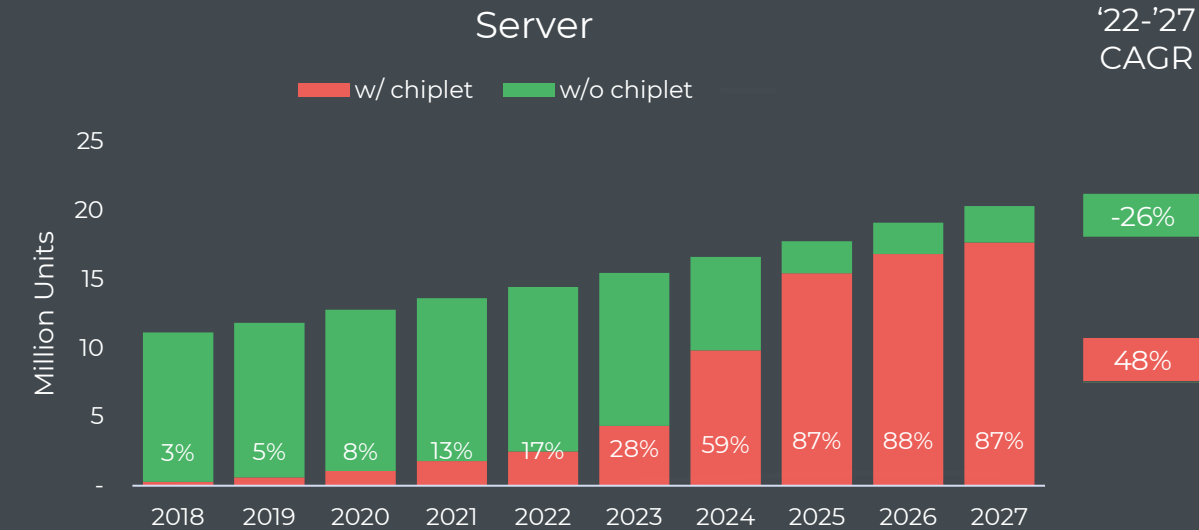
The value of the overall chiplet market is a function of the market for all ICs made in a chiplet process!

- Market value equivalent to end IC based on Chiplet-based package platform.
- Even though the main benefit is improved yield, it provides a path forward for expanded optimization, fewer tape-outs, improved product line efficiency, and industry diversity.
- Separating value of individual chiplet dies from the platform is impractical.
- The market value of the chiplet platform mainly benefits the SoC/SiP chip supplier.
- To address this challenge, Yole is tracking the value of the Chiplet market as a function of the Total Addressable Market (TAM).

# END SYSTEMS MOST RELEVANT FOR CHIPLETS



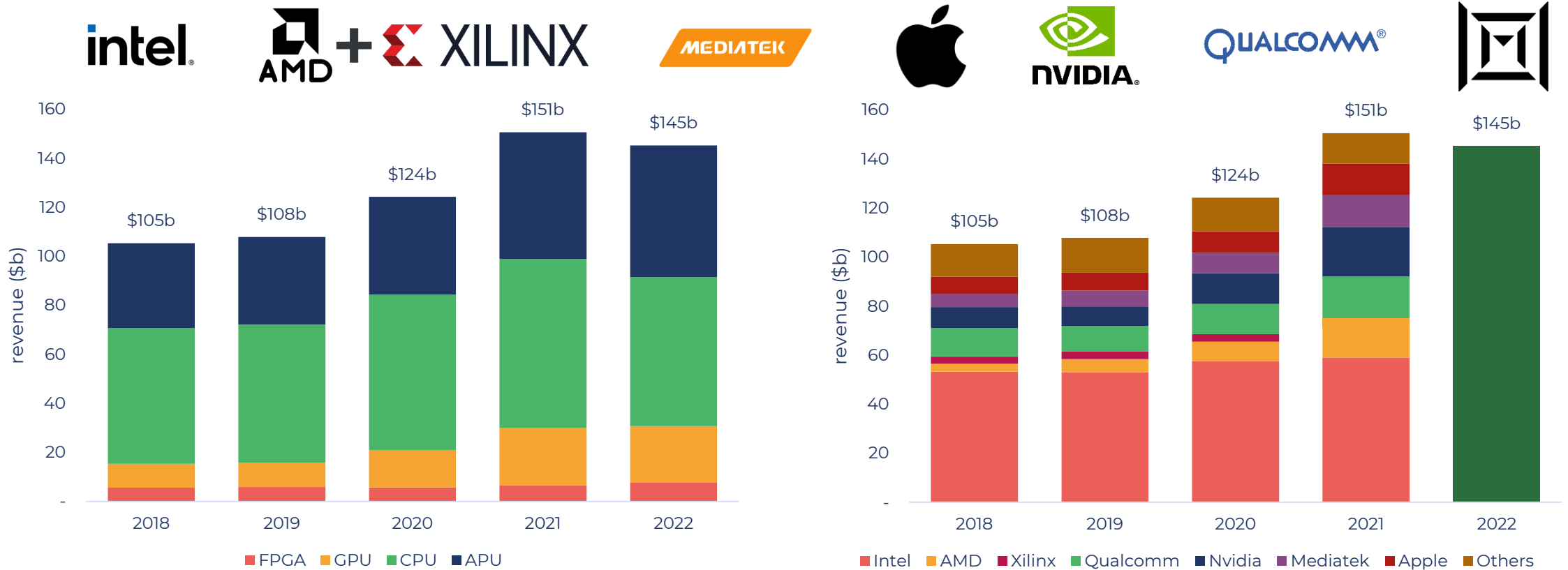
# END SYSTEMS MOST RELEVANT FOR CHIPLETS



# CRACKING INTO THE PROCESSOR MARKET



7 companies make up >90% of the overall processor revenue



- Of these companies, Intel, AMD, and Apple, Marvell, and IBM have brought implementations of chiplets to market.
- Thus far, the chiplets brought to market have been mainly the in-house, proprietary kind, where the solution contains only chips from one vendor, using in-house IP or that of a manufacturing partner

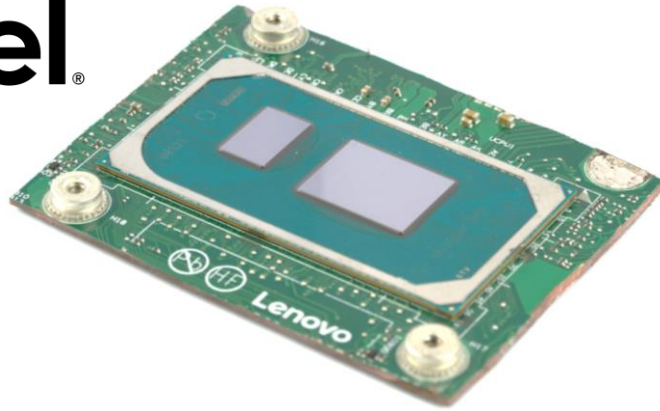
# EXAMPLES IN THE MARKET TODAY – INTEL TIGER LAKE I7



CPU and PCH die flip-chip on organic substrate to form laptop SoC

Intel has done similar since Haswell (4<sup>th</sup> generation, 2013) in mobile products

intel®



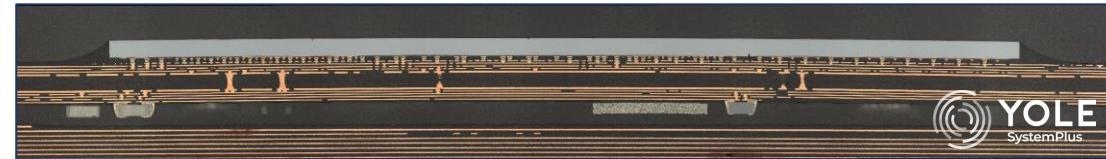
Package Overview on board

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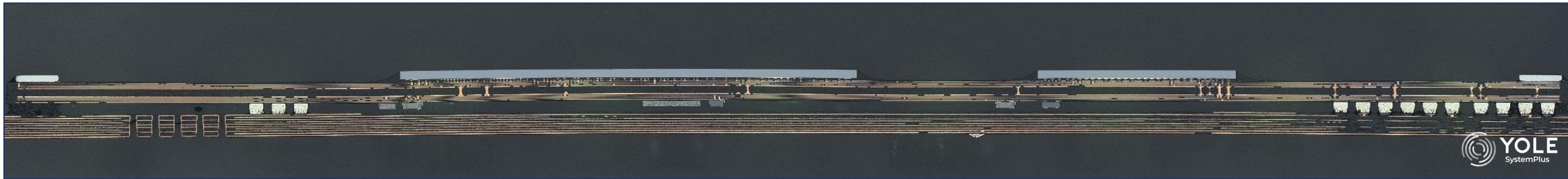
Package Overview

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Package Cross-section

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Package Cross-section

©2023 by YOLE SystemPlus



# EXAMPLES IN THE MARKET TODAY – AMD ZEN3 + 3D V-CACHE

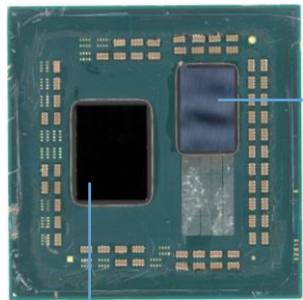


I/O die and one or more Core Complex Dies Flip-chip on org substrate. V-cache is stacked on CCD through hybrid bonding

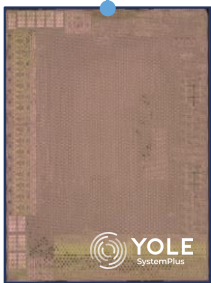
3D V-Cache Portfolio:

Client – Ryzen 7 5800X3D 2022, Ryzen 7 7800X3D, Ryzen 9 7900X3D, Ryzen 9 7950X3D

Server – Milan X, Genoa X



I/O Die AMD Ryzen 7 Package  
©2023 by YOLE SystemPlus



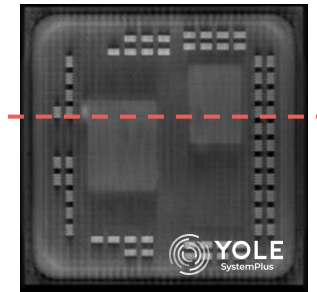
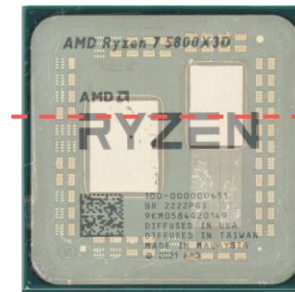
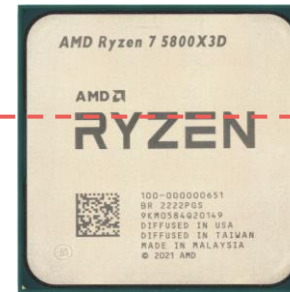
Structural silicon & Cache dies



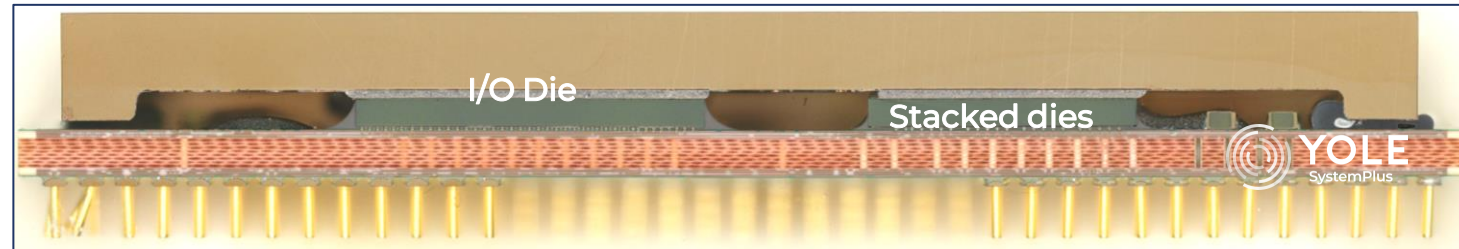
CPU Compute die



Cross sectioning



Package Cross-section plane  
©2023 by YOLE SystemPlus

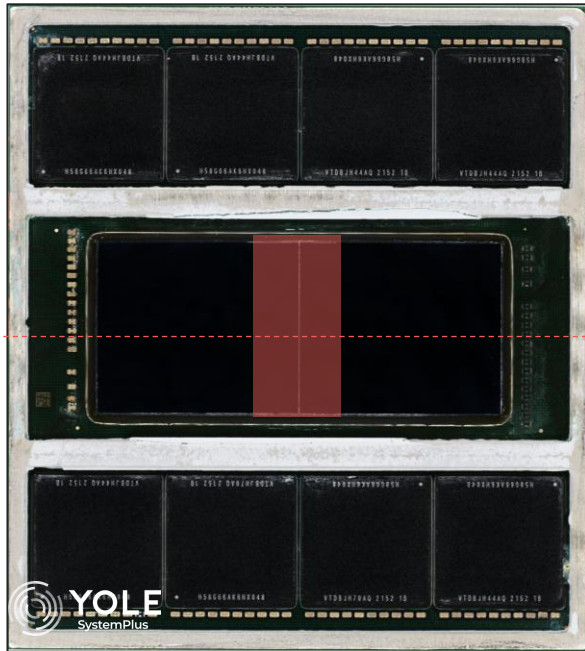


Package Cross-section  
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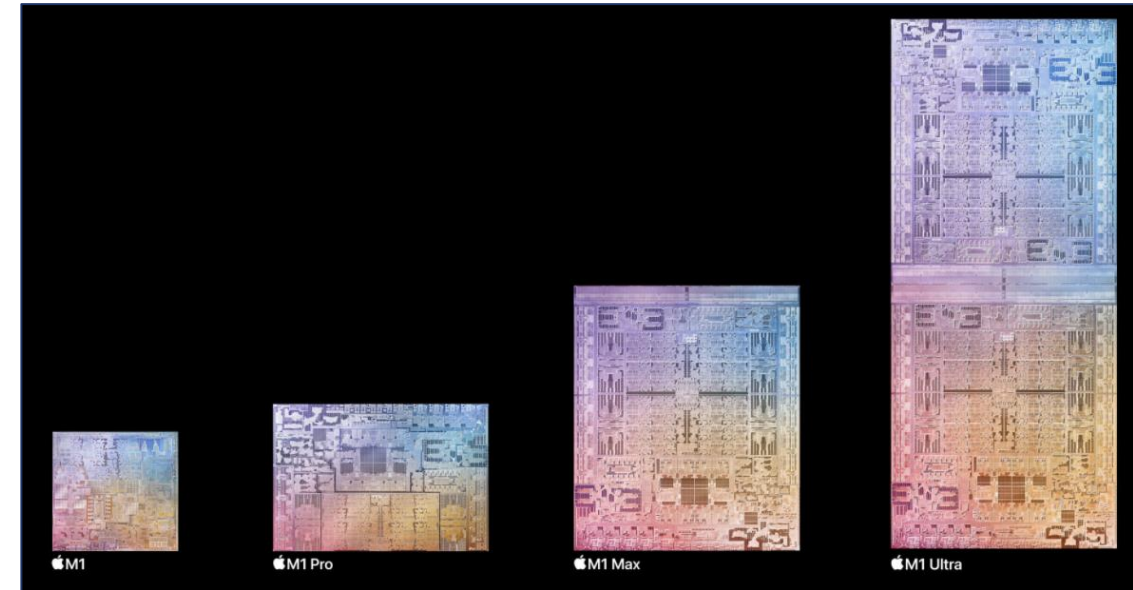
# EXAMPLES IN THE MARKET TODAY – APPLE M1 ULTRA



Two M1 Max dies connected through a silicon bridge (LSI, called UltraFusion by Apple) to make a larger SOC with 2X physical metrics (CPU cores, GPU cores, Cache size, etc)



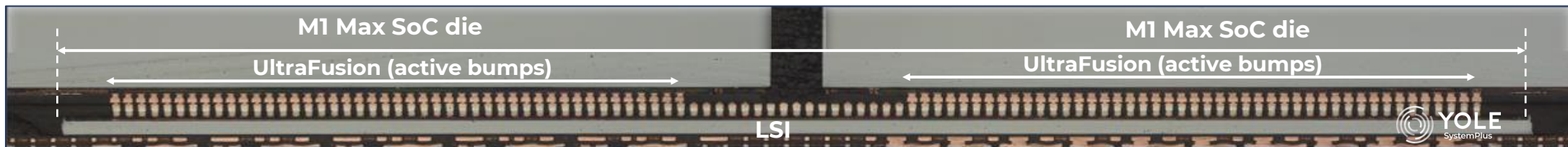
Cross-sectioning



M1 Ultra package opening

©2023 by YOLE SystemPlus

©Apple



Package Cross section

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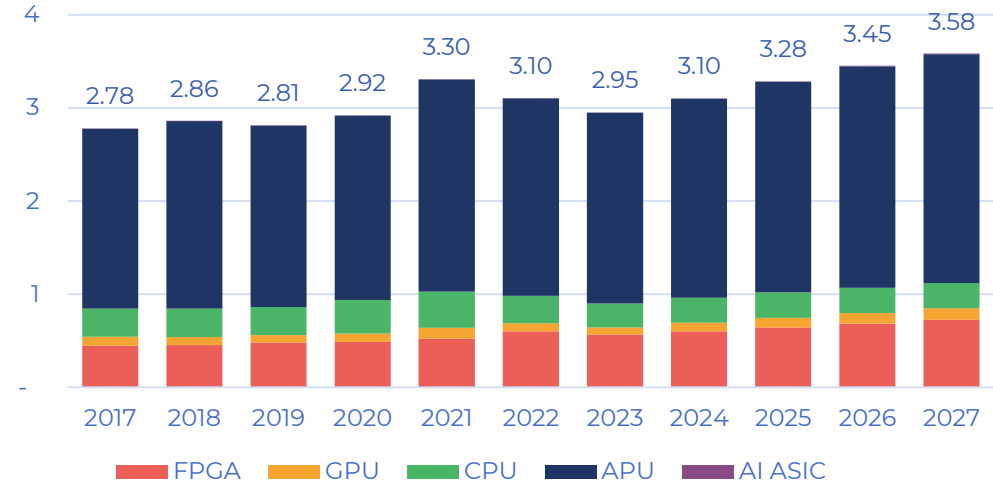


# SIZING UP THE PROCESSOR MARKET

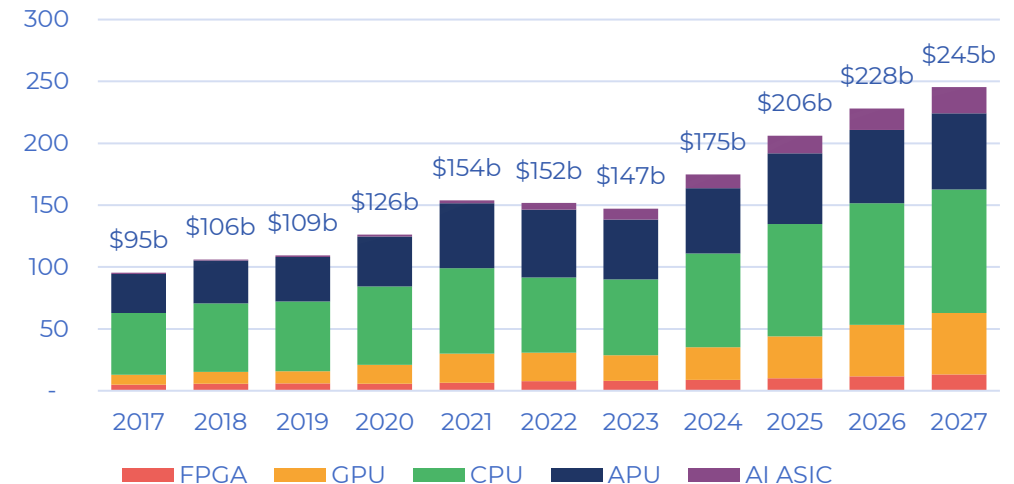


- Challenging economic environment in 2H 2022 → 2023
  - Biggest impact to consumer and personal computing
  - Data center markets looking more resilient, though CSP are adjusting near-term
- Longer term, expecting growth in units and price leading to a processor TAM of \$245b by 2027
  - CPU and GPU blended price increases as data center products become a larger piece of the total
  - Price increases in data center CPU and GPU as future generation performance gains come at incremental design and manufacturing cost

Units (billions)



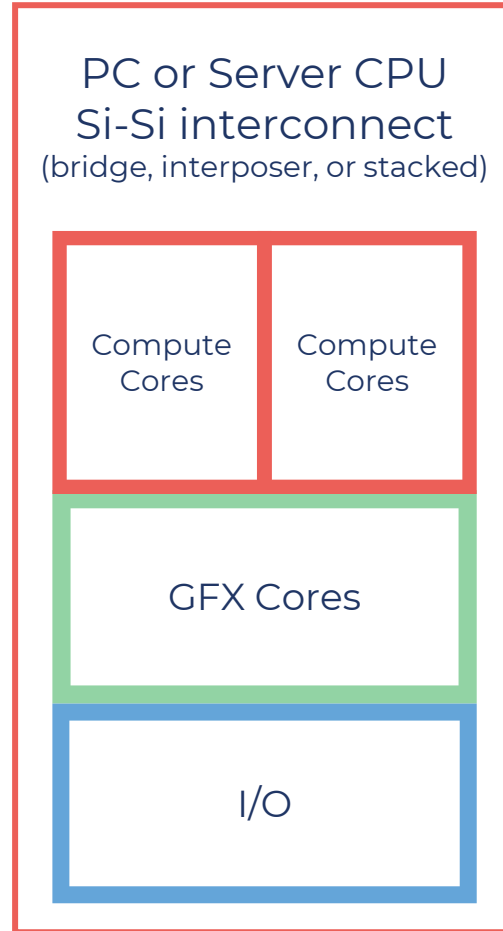
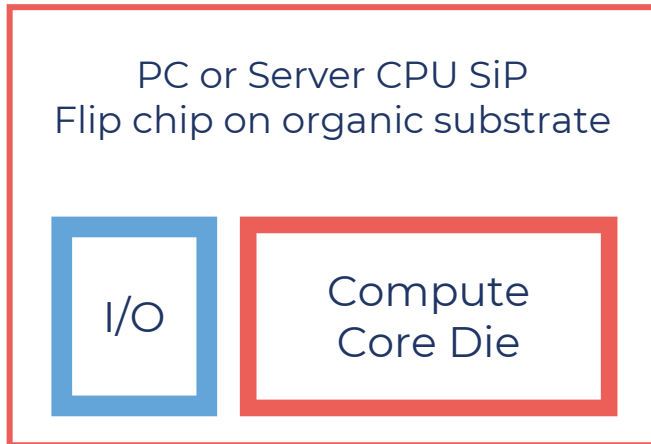
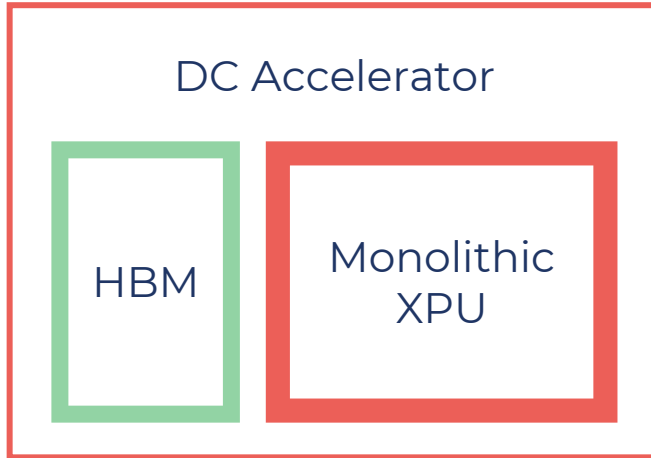
Revenue (\$b)



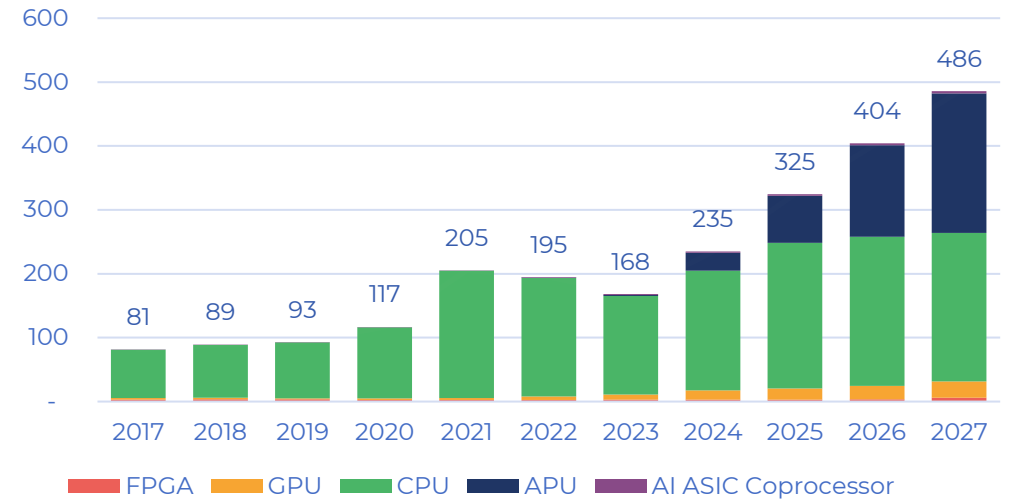
# SIZING UP THE CHIPLET-BASED PROCESSOR MARKET



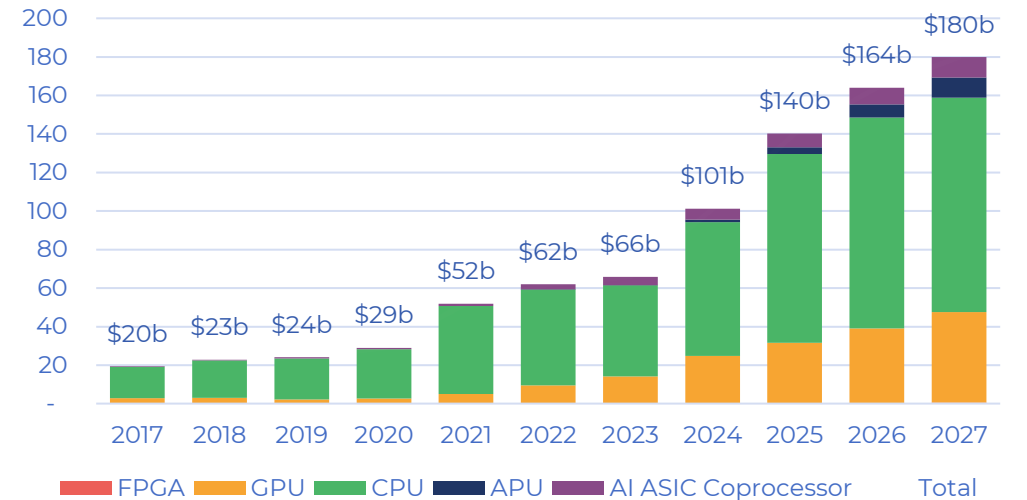
Broad definition of chiplets, including System-in-Package, implementations of HBM with monolithic XPU, and Si-Si interconnected ICs



Units (millions)



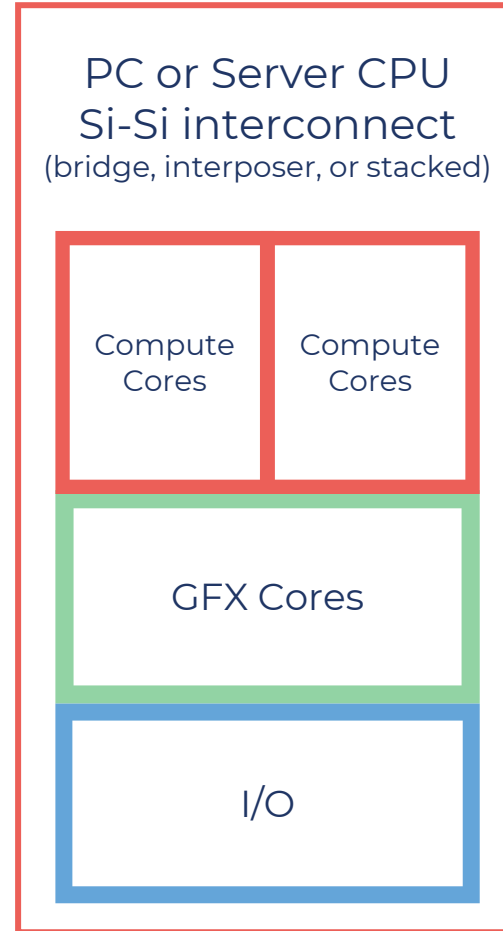
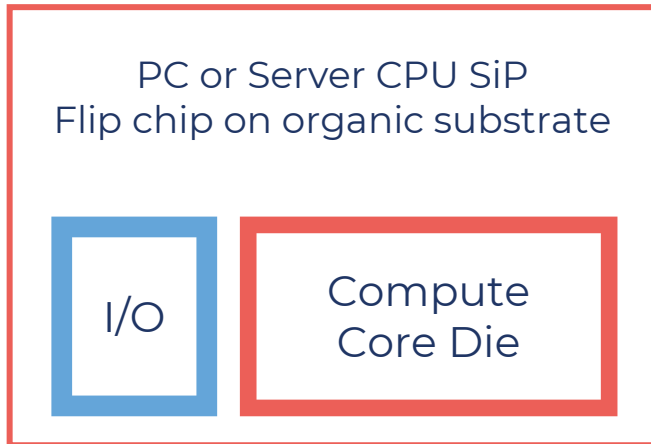
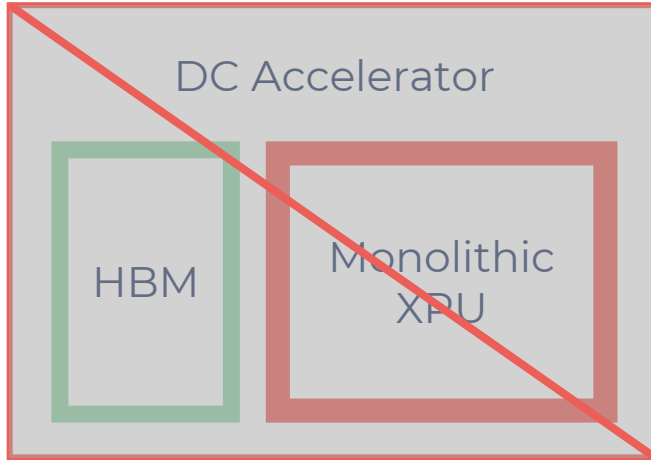
Revenue (\$b)



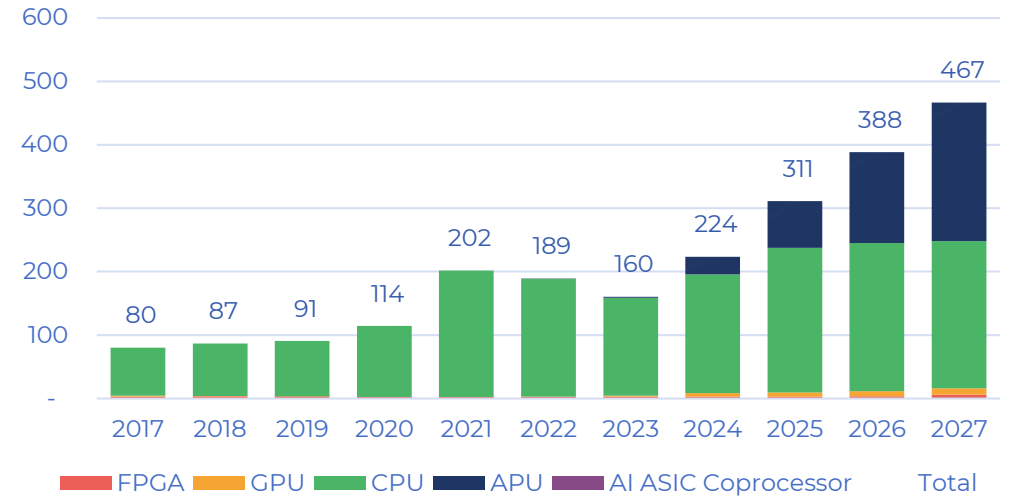
# SIZING UP THE CHIPLLET PROCESSOR MARKET



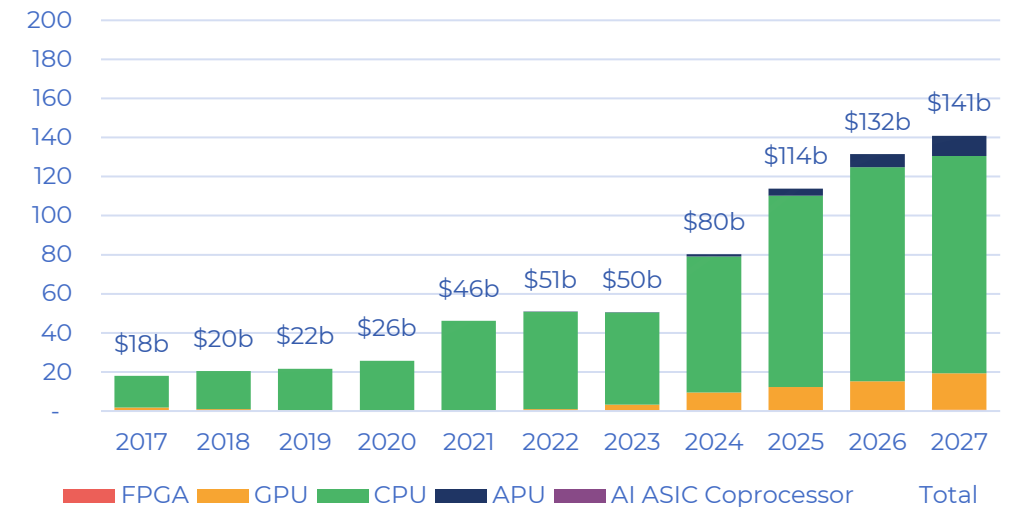
Narrower definition of chiplets, including System-in-Package, and Si-Si interconnected ICs



Units (millions)



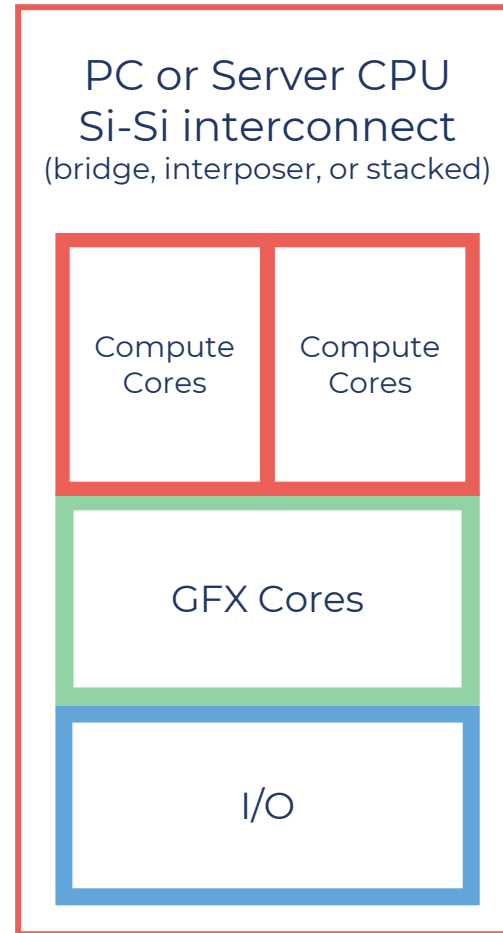
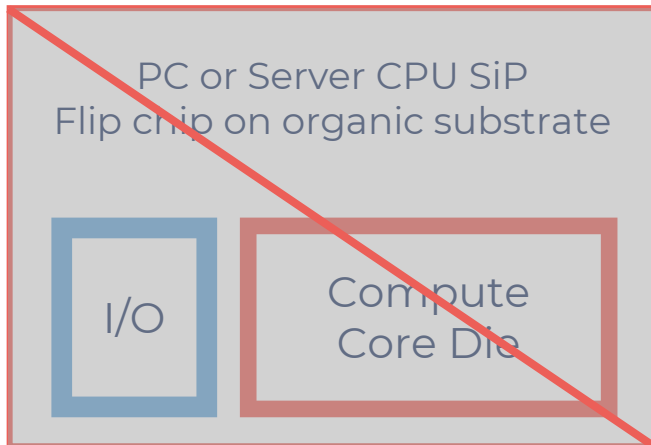
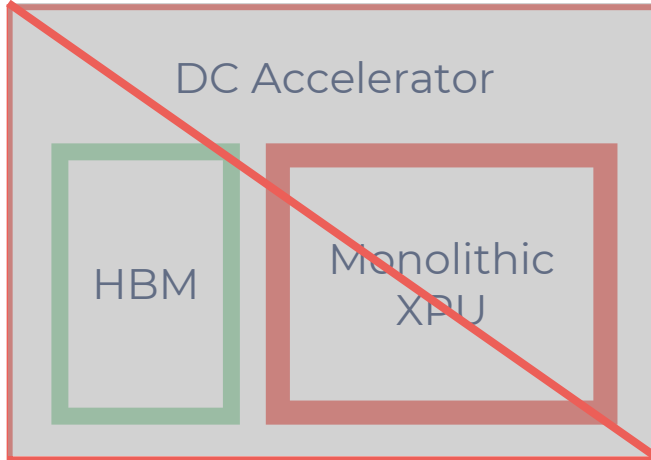
Revenue (\$b)



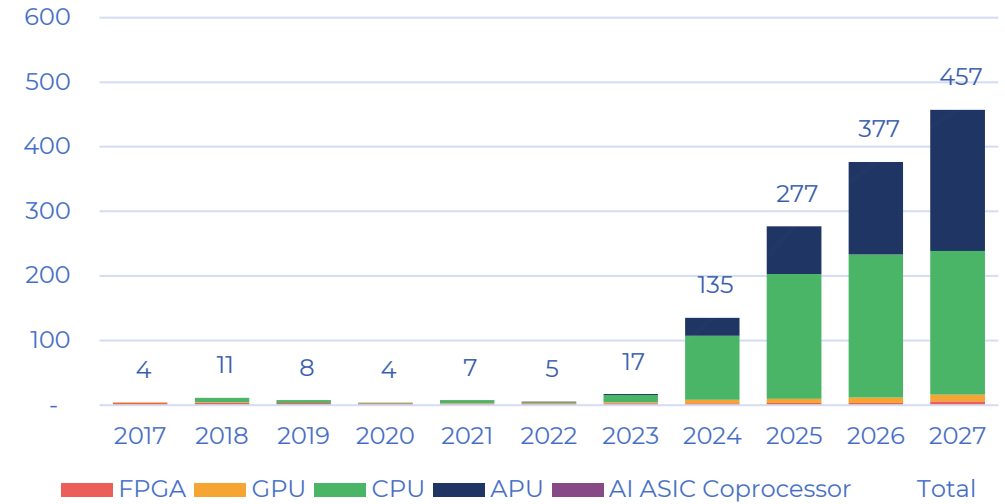
# SIZING UP THE CHIPLET PROCESSOR MARKET



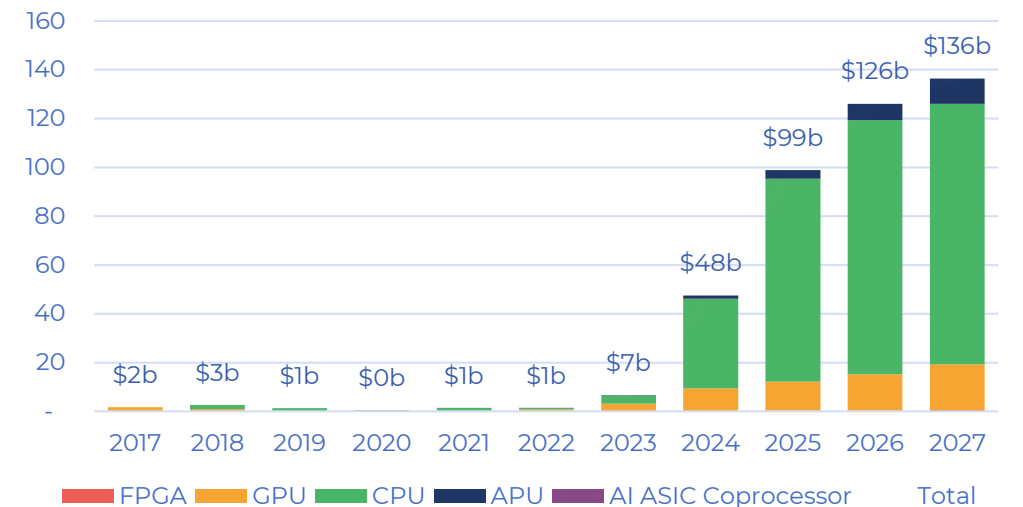
Narrowest definition of chiplets counting just Si-Si interconnected ICs



Units (millions)



Revenue (\$b)

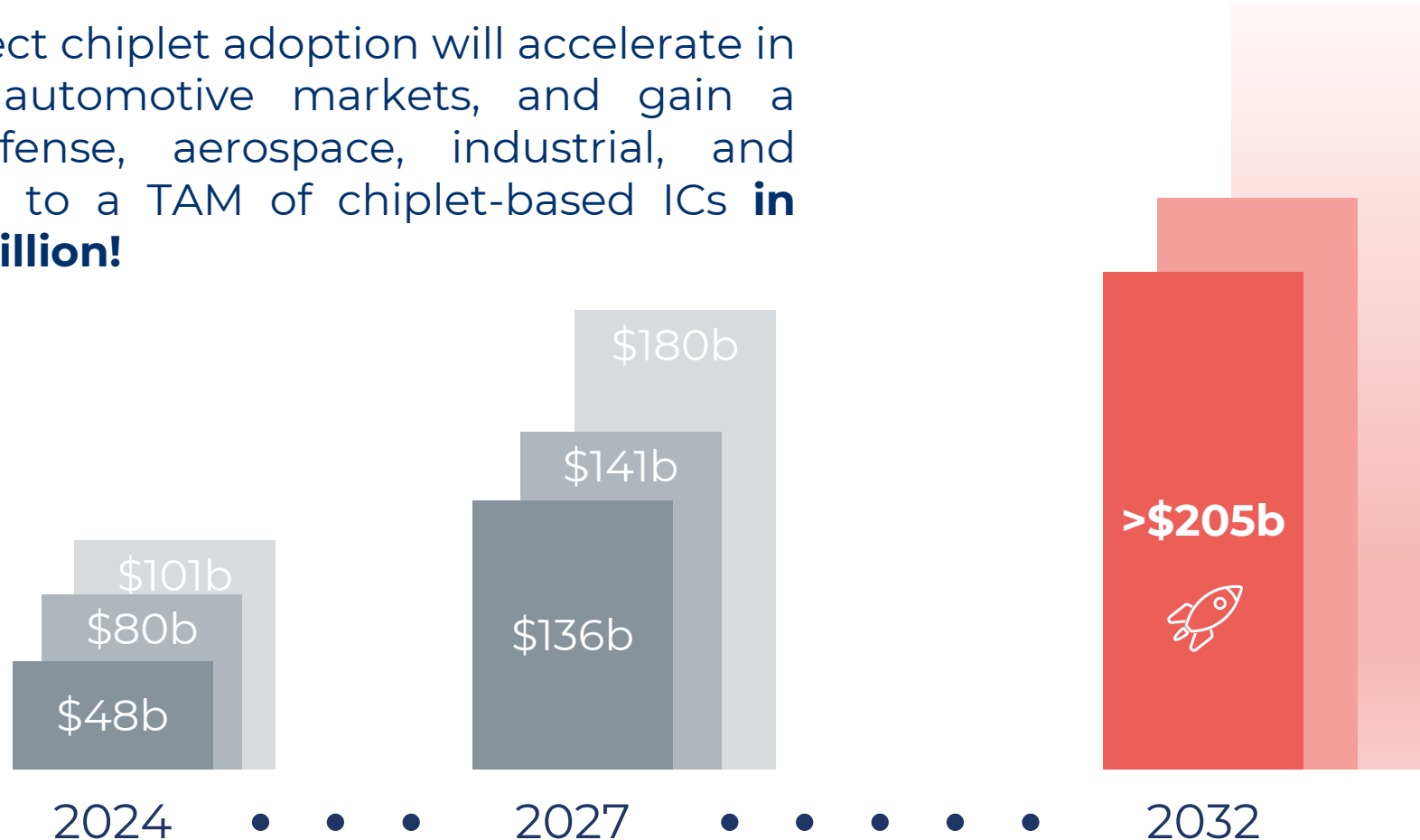


# CHIPLETS IN THE LONG TERM



With even the narrowest definition of chiplets, we still find a market for chiplet-based processors in excess of \$135 billion by 2027.

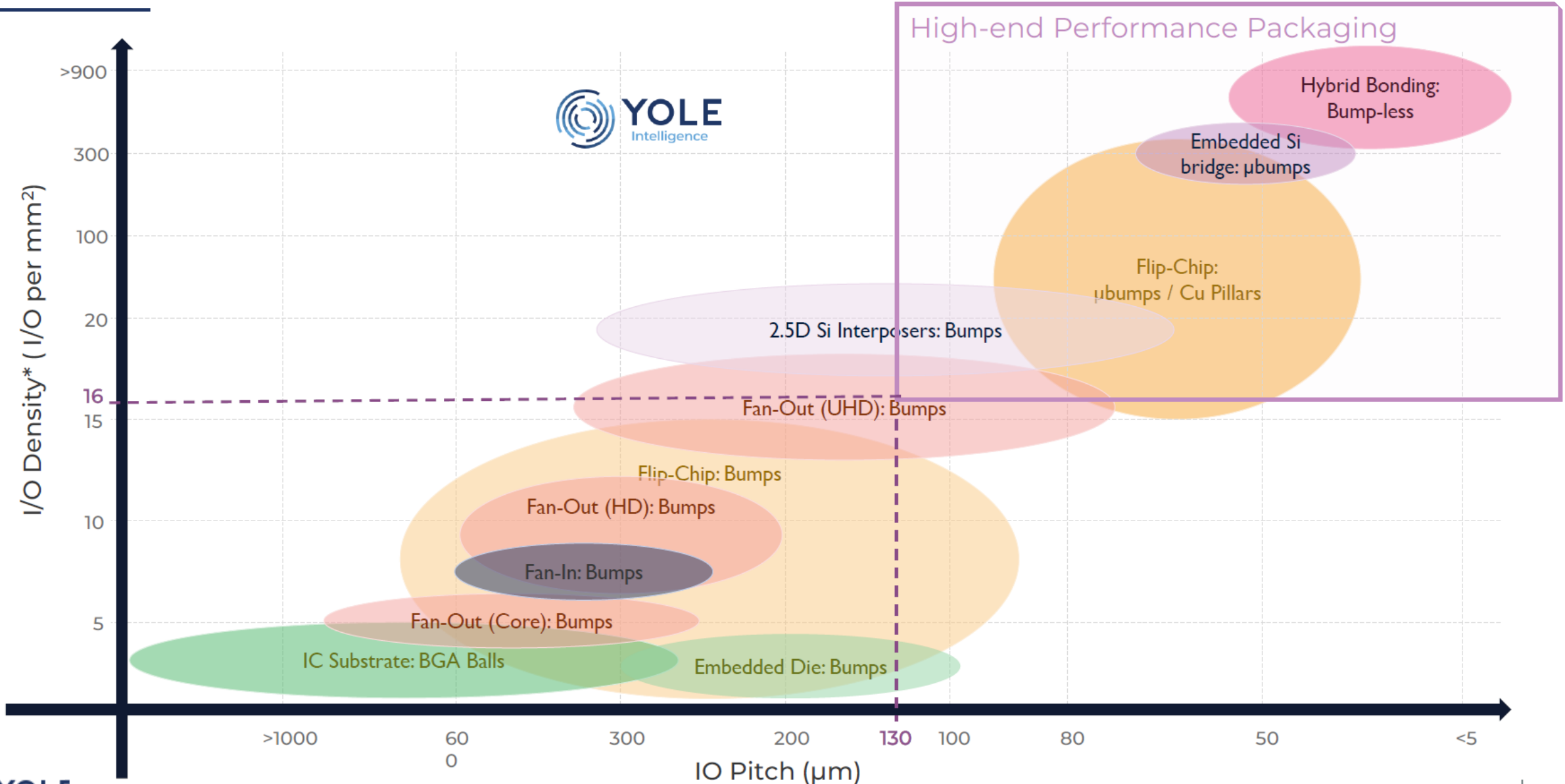
**By 2032**, we expect chiplet adoption will accelerate in consumer and automotive markets, and gain a foothold in defense, aerospace, industrial, and medical, leading to a TAM of chiplet-based ICs **in excess of \$205 billion!**



# HIGH-END PERFORMANCE PACKAGING DEFINITION



## Yole's definition of High-end Performance Packaging





# ADVANCED PACKAGING REVENUE FORECAST

Packaging revenues gain momentum → chiplets are a main factor

Advanced Packaging Revenue (\$B)



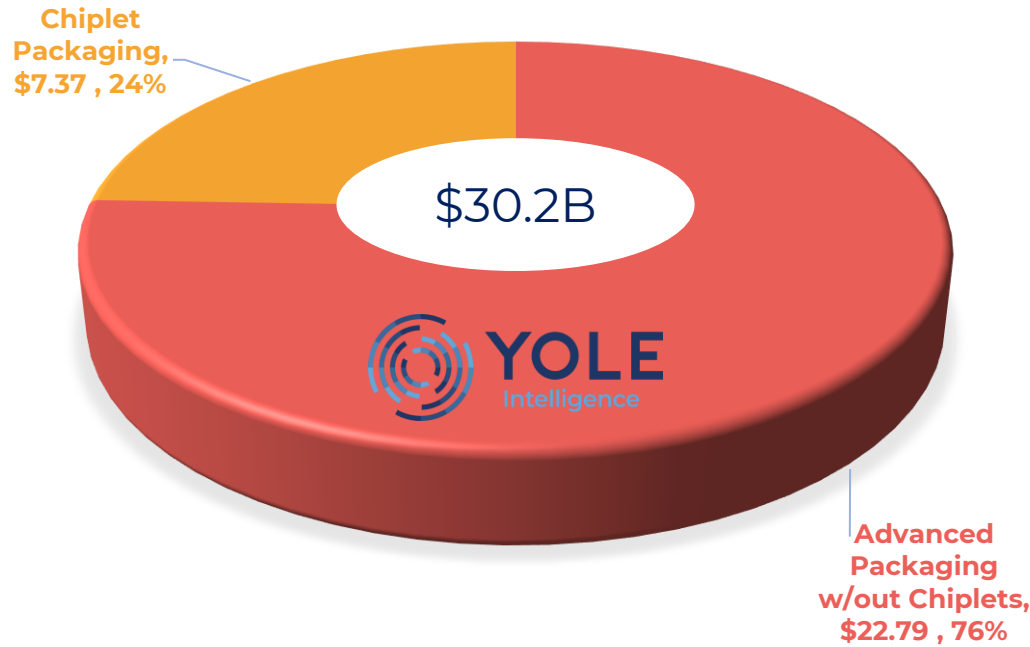
|              | 2021           | 2022           | 2023           | 2024           | 2025           | 2026           | 2027           | CAGR         |
|--------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------------|
| SiP          | \$3.50         | \$3.43         | \$3.59         | \$3.72         | \$3.90         | \$4.08         | \$4.20         | 3.1%         |
| FCCSP        | \$6.39         | \$6.89         | \$7.72         | \$8.28         | \$8.77         | \$9.87         | \$10.96        | 9.4%         |
| FCBGA        | \$9.26         | \$10.43        | \$11.13        | \$12.65        | \$14.32        | \$16.39        | \$17.70        | 11.4%        |
| 2.5D/3D      | \$7.37         | \$9.48         | \$11.29        | \$13.73        | \$15.91        | \$19.60        | \$23.91        | 21.7%        |
| WLCSP        | \$2.18         | \$2.10         | \$2.05         | \$2.12         | \$2.22         | \$2.31         | \$2.39         | 1.5%         |
| FO           | \$1.46         | \$1.51         | \$1.66         | \$1.93         | \$2.19         | \$2.34         | \$2.52         | 9.5%         |
| <b>TOTAL</b> | <b>\$30.17</b> | <b>\$33.83</b> | <b>\$37.44</b> | <b>\$42.44</b> | <b>\$47.31</b> | <b>\$54.59</b> | <b>\$61.68</b> | <b>12.7%</b> |

# CHIPLET PACKAGING VS. OTHER ADVANCED PACKAGING FORECAST

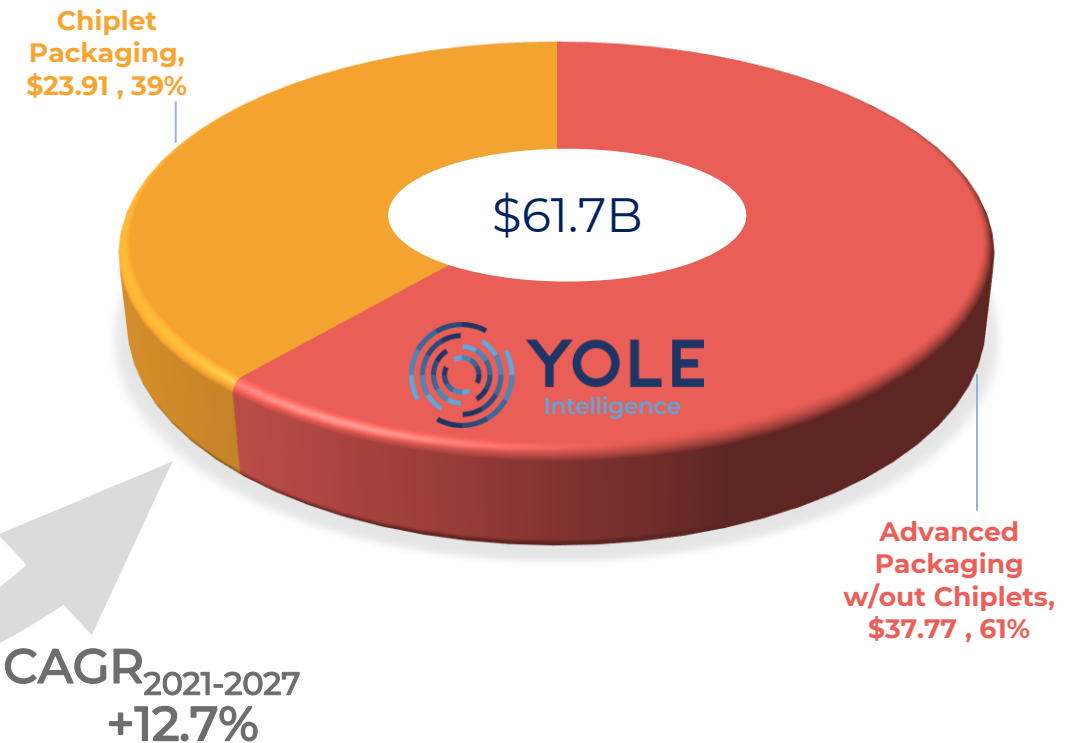


In \$B

### CHIPLET PACKAGING MARKET SHARE - 2021



### CHIPLET PACKAGING MARKET SHARE - 2027



High-End Performance Packaging, with some of its platforms incorporating chiplets, is expected to pick up more market share in the coming years reaching 39% in 2027 up from 24% in 2021.

# LARGER MARKET OPPORTUNITY AS CHIPLETS BECOME STANDARDIZED, BREAK OUT FROM PROPRIETARY MODEL



Shown here are some of the standards bodies already developing open-source models characterizing hardware or software for developing package-level IC platform interconnectivity.

In 2022, two of these organizations released specifications for open-source standardization for chiplet interconnect characteristics:

- The Open Compute Project, Open Domain-Specific Architecture (OCP ODSA) workgroup released the Bunch of Wires (BoW) specifications
- The Universal Chiplet Interconnect Express (UCIe) released the UCIe 1.0 specification standardization models starting. OCP BOW, UCIe

For details of these standards and news of their activities, we recommend visiting their tables and events.

Regardless of the characteristics of the specifications, the existence of these standards will have an impact on the future development of chiplets. We can expect:

- More opportunities for Intellectual Property (IP) developers targeting chiplets
- Electronic Design Automation (EDA) tools for chiplets
- Foundry Services targeting chiplet design and integration
- Assembly and Test services targeting chiplet design and integration
- New applications enabled by application-specific optimized chiplets





As we alluded to earlier, the value of the chiplet platform is not just in the value of the semiconductor die or the advanced packaging services. It is in its contribution to extending the economics of Moore's Law for generations to come. It also represents new opportunities for:

- Chiplets on the open market
- IP providers
- EDA tools designers
- New software extensions
- Flexible SoC architecture
- New, previously unimagined SoCs, integrating more functions.
- New applications
- Collaboration between optimized IC subsystem designers



Expanding chiplets can be a threat for:

- Monolithic chip suppliers
- Tightly controlled ecosystems with high barriers to entry
- Highly dominant vertical integrators

# WHAT IS STANDING IN THE WAY?

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Monolithic processors include decades of chip design to optimize:

- Intrachip communication with optimized timing and reduced latency
- Thermal characteristics
- Power efficiency
- Signal Integrity
- Application-specific behaviors

These optimizations can be incompatible with a chiplet-based strategy as new characteristics such as routing may have to be redesigned.

Proprietary solutions suppliers must see the value in collaborating to increase profit by increasing the market size and associated opportunities for revenue streams.

Like all new technologies that benefit from standardization, there is frequently a battle for competing standards. When competing standards become incompatible and fight for market share, advancement tends to be slower and hard earned.





Like all modern industry evolutions, there will be soaring rhetoric. Hopefully, this market briefing has put the market into perspective:

- Chiplet strategies are not going to create an overnight revolution for the semiconductor industry, but they are a much necessary next step in restoring an evolutionary path to economic progress as predicted by Moore.
- Not all semiconductor markets will benefit directly from chiplets, In fact some discrete semiconductor suppliers will find the competition difficult if they are not able to adapt to also supplying chiplets. But for advancing large heterogeneous designs, chiplets represent an evolutionary improvement over large monolithic dies that now suffer from the economical and physical limitations of continued miniaturization.
- Proprietary and open market solutions will continue to compete, but the market overall will grow much faster with industry standards adoption.
- Chiplet strategies will not eliminate the need for continued advancements in miniaturization in manufacturing processes and materials. In fact, as the bottlenecks for on-chip subsystems that do not shrink well, get off-loaded to a separate die, further miniaturization of core logic elements can progress with a more predictable cadence.

## Conclusion

*The silicon supply chain is diverse. It has to serve many vertical electronic equipment segments including Automotive, Personal Data Processing, Data Center and Enterprise Data Processing, Communications and Infrastructure, Medical, Defense, Aerospace and Industrial. Each market includes different value and application-specific requirements that need to be served. Processor suppliers have turned to highly heterogeneous chip platforms to remain competitive. This approach is becoming increasingly complex and costly to manufacture.*

*In response to these challenges, chip builders have begun to adopt the use of chiplets. However, the same diversity that created the demand for chiplets, also makes it unlikely that any one supplier has the broad expertise to serve all these markets. Thus, many different Chiplet supply chains will emerge and no one solution will serve all markets. The emerging market around Chiplets will need many players and a low barrier to entry allowing for rapid innovation. Open communities sharing the effort for building common tools, prototypes, business workflows and standardizations are critical to accelerate a Chiplet Economy,*

**We are Yole Group, come find us**



## Tom Hackenberg – Principal Analyst

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Tom Hackenberg is a Principal Analyst for Computing and Software at Yole Intelligence. Tom is engaged in developing processor market monitors and research into related technology trends. He is currently focused on edge computing, low and ultralow power processors such as microcontrollers. Tom is an industry leading expert with more than fifteen years of experience reporting on markets for semiconductor processors. Tom is also well-versed in related technology trends including IoT, heterogeneous processing, chiplets, AI and edge computing.

Tom is located in Austin, Texas and conducts market research globally throughout the United States, Europe, Mainland China and Asia Pacific markets. Tom holds a BSECE from the University of Texas at Austin.



## John Lorenz – Senior Analyst

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John Lorenz is a Senior Technology and Market Analyst, Computing & Software within the Semiconductor, Memory & Computing division at Yole Développement (Yole), part of Yole Group of Companies. John is engaged in the development of market and technology monitors for the logic segment of advanced semiconductors, with a primary focus on processors.

Prior to joining Yole, John held various engineering and strategic planning roles over 15 years at Micron Technology.

John has a Bachelor of Science degree in Mechanical Engineering from the University of Illinois Urbana-Champaign (USA), with a focus on MEMS devices.



## REPORTS

### Insight

- › Yearly reports
- › Market, technology and strategy analysis
- › Reverse costing and reverse engineering
- › Performance analysis

### Format

- › PDF files with analyses
- › Excel files with graphics and data
- › Web access

### Topics

- › Photonics, Imaging & Sensing
- › Lighting & Displays
- › Power Electronics & Battery
- › Compound Semiconductors
- › Semiconductor Manufacturing and Packaging
- › Computing & Memory

**115+ reports per year**

## MONITORS

### Insight

- › 4 times per year updated market data and technology trends in units, value at wafer level
- › Direct access to the analyst

### Format

- › Excel files with data
- › PDF files with analyses graphs and key facts
- › Web access

### Topics

- › Advanced Packaging
- › CIS
- › Compound Semiconductor
- › DRAM & NAND
- › Micro-controller
- › Processor
- › RF
- › Semiconductor Test Equipment
- › Semiconductor Subsystems
- › Wafer Start

**11 different monitors quarterly updated**

## TRACKS

### Insight

- › Teardowns of phones, smart home, wearables and automotive modules and systems
- › Bill-of-Materials
- › Block diagrams

### Format

- › Web access
- › PDF and Excel files
- › High-resolution photos

### Topics

- › Consumer: Smartphones, smart home, wearables
- › Automotive: Infotainment, ADAS, Telematics

**220+ teardowns per year  
Daily updates**

## CUSTOM SERVICES

### Insight

- › Specific and dedicated projects
- › Strategic, financial, technical, supply chain, market and other semiconductor-related fields
- › Reverse costing and reverse engineering

### Format

- › PDF files with analyses
- › Excel files with graphics and data

### Topics

- › Photonics, Imaging & Sensing
- › Lighting & Displays
- › Power Electronics & Battery
- › Compound Semiconductors
- › Semiconductor Manufacturing and Packaging
- › Computing & Memory

**190 custom projects per year**