SYNOPSYS®

UCIe: An Open Standard Interface for Chiplet-Based Multi-Die Systems

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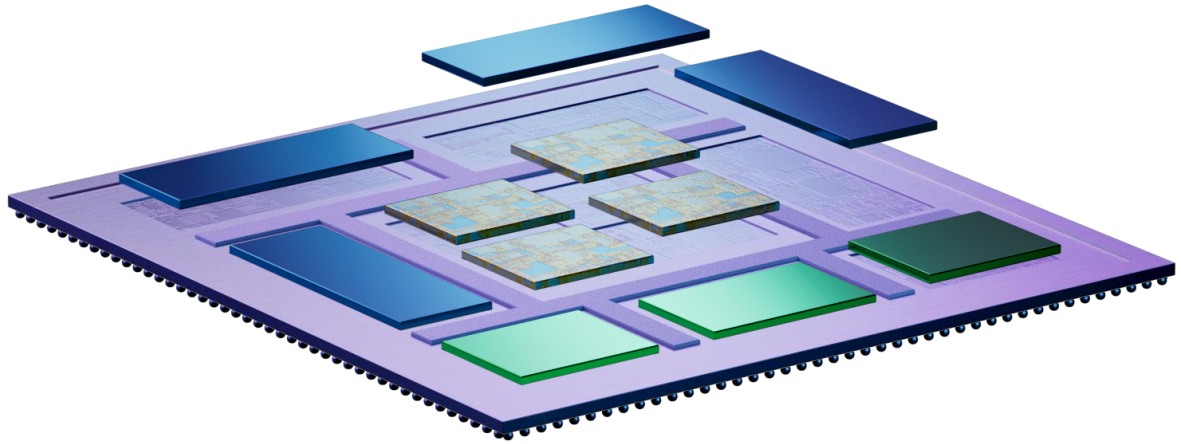
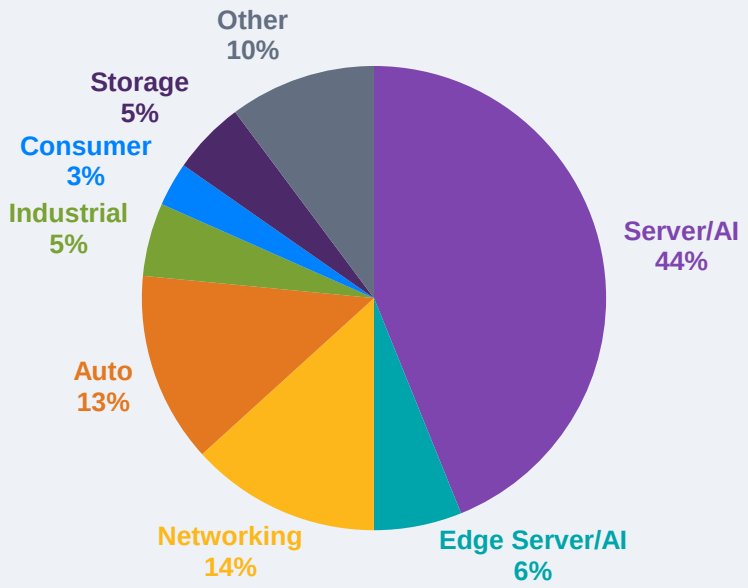
The SysMoore Era of Multi-Die Systems



The Era of Multi-Die Systems is Here

Synopsys Tracking ~100 Multi-Die System Designs

Designs by Application



- Servers / AI dominate
- NICs, Switches common use case
- Smartphone / Graphics /PC primarily proprietary
- Co-packaged Optics, Automotive ramping

Multi-Die System Drivers

- Accelerated scaling of system functionality at a cost-effective price (>2X reticle limits)
- Reduced risk & time-to-market by re-using proven designs/die
- Lower system power while increasing throughput (up to 30%)
- Rapid creation of new product variants for flexible portfolio management

Multi-Die Systems Require D2D Interface Standardization

Technical Merits, Maturity & Strength of Ecosystem are Key for Success

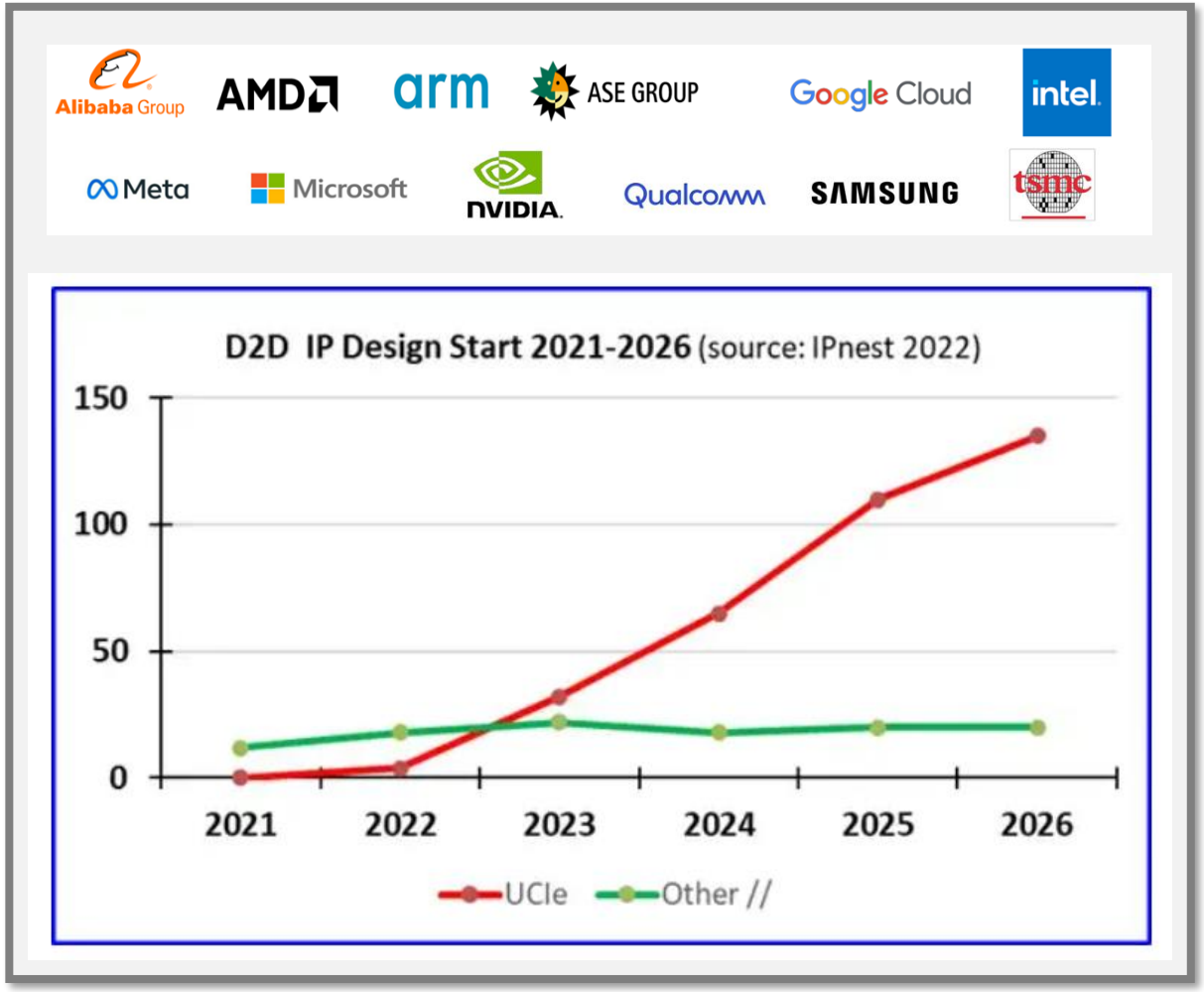
Alliance	OIF	OPEN Compute Project®		CHIPS ALLIANCE	UCIe Universal Chiplet Interconnect Express
Standard	**XSR**	**BOW**	**OHBI**	**AIB**	**UCIe**
Data Rate	112G / 224G	8G / 16G	8G / 16G	6G	16G / 32G
Protocol	Not Defined	Not Defined	Not Defined	Not Defined	Streaming, PCIe, CXL
Package Focus	2D	2D (2.5D also supported)	2.5D (2D also supported)	2.5D	2D, 2.5D
Target Applications	Optical Networking (CPO/NPO)	Cost sensitive aggregation	High density scale for data center	Mil-aero ecosystem	Scale & Split w/ streaming Aggregation w/ PCIe/CXL

UCIe is the Preferred D2D Interface

Technical Merits, Comprehensive Spec & Broad Eco-System

UCIe Universal Chiplet Interconnect Express

- Technical Merits
  - Most compelling PPAs
- Comprehensive & Futureproof
  - Full stack & Interoperability
- Broad Industry Support
  - Open Eco-system
  - More than 100 UCIe members

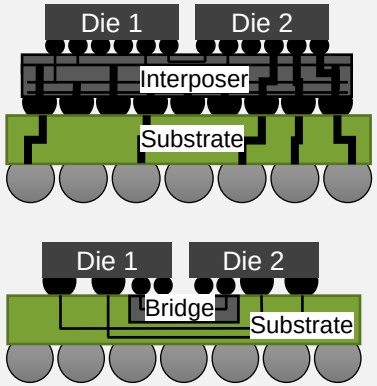


UCIe PHY Support for Advanced/Standard Packages

Two Options Optimized for Each Use Case

UCIe-A PHY for Advanced Packages

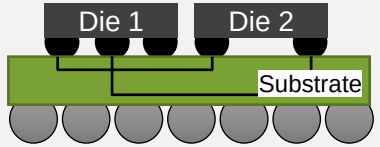
- 1Tbps per module @ 16Gbps/pin
- 0.3pJ/bit energy efficiency
- 64 TX + 64 RX pins per Module
- 5.2Tbps/mm aggregate BW efficiency
- 45~55um bump pitch
- 2mm unterminated link
- Low power modes
- 2ns latency (TX + RX)
- BER << 1e-15



UCIe-S PHY for Standard Packages

- 0.25Tbps per module @ 16Gbps/pin
- 0.5pJ/bit Energy Efficiency
- 16 TX + 16 RX pins per Module
- 0.9Tbps/mm aggregate BW efficiency*
- 110~130um bump pitch
- 25mm, terminated link
- Low power modes
- 2ns latency (TX + RX)
- BER << 1e-15

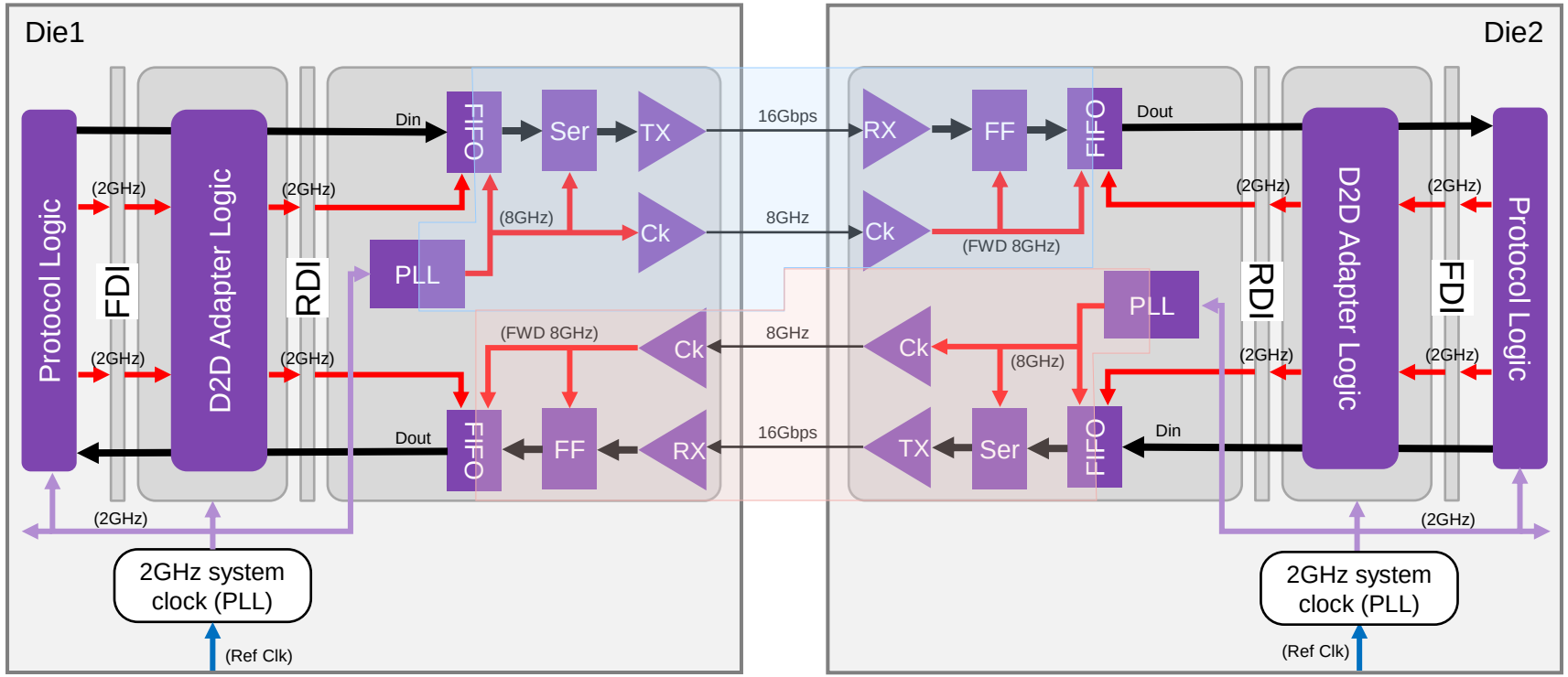
* 32 pin stacked mdule



Common Architecture, Protocol and Logic Interfaces for all Package Types

UCIe is a Latency Optimized Architecture

Simplified Clock Domains w/ Clock Forwarding and Matched Lanes

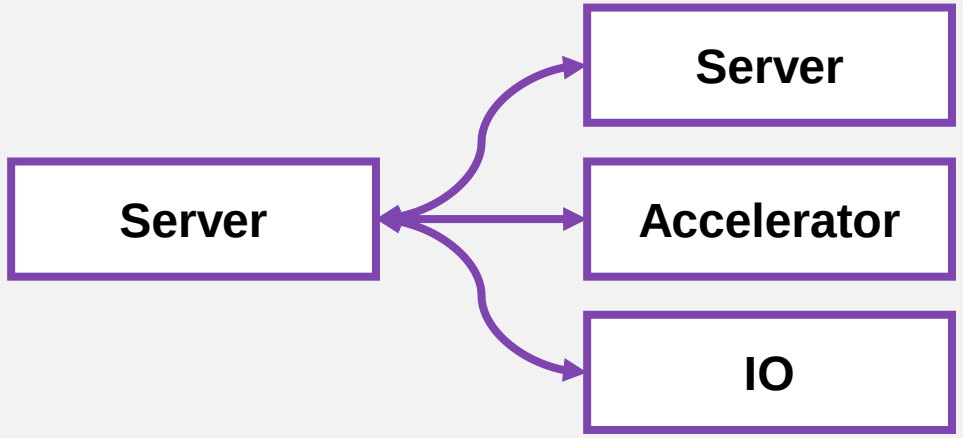


- Optimized architecture for D2D links
  - No CDR
  - Simple equalization
  - Optional RX termination
- RDI/FDI interface operate with local 2GHz system clock
  - Optionally 1GHz
- PHY includes FIFOs to accommodate phase mismatch between 8GHz FWD clk and local clk

Use Models Projected to Evolve from Captive → Marketplace

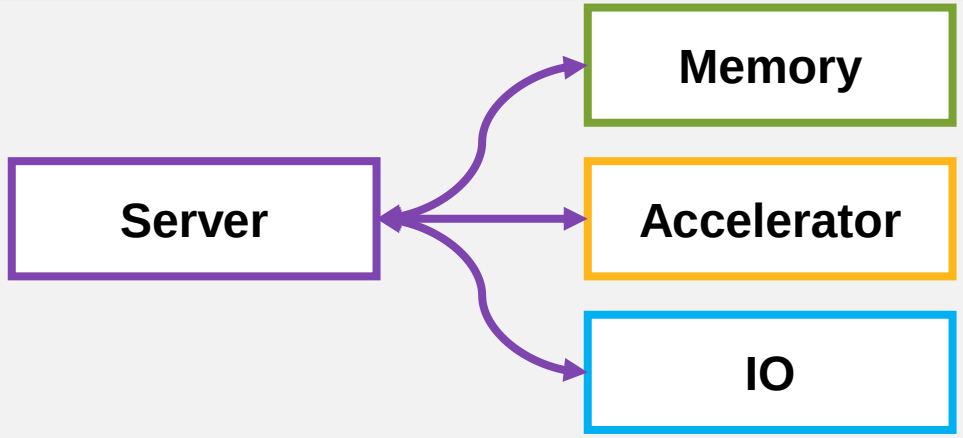
UCIe Supports Multiple Protocols: Lightweight (Captive) & Standards Based (Chiplets)

Captive/Fixed Systems (Now & Future)



- Function splitting by the same vendor
- No interop, no standard protocol
- Lightweight, low latency, streaming mode
- Bridges to NoC for virtual NoC-NoC interface
- Example – Server, Smart NIC, AI, Switches

Open Marketplace (Future)

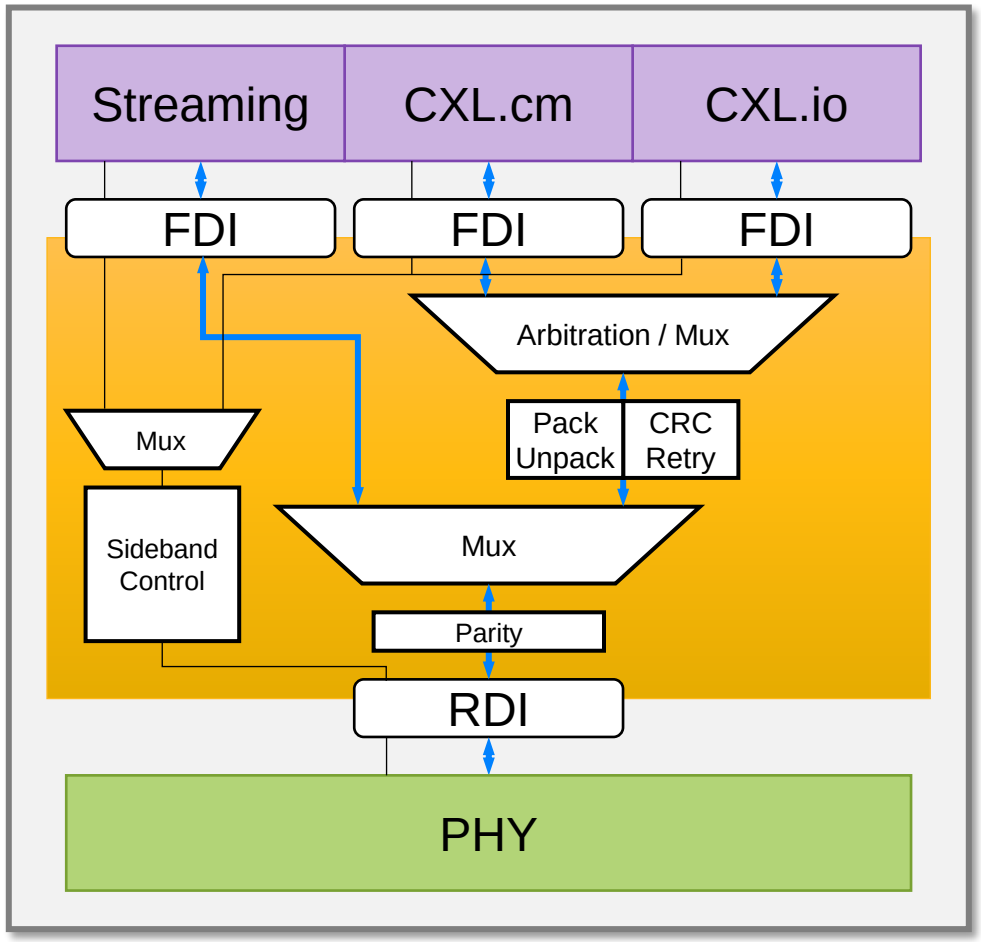


- Isolated functions from different vendors
- Standardization, eco-system & Interop
- Protocols: CXL & PCIe
- Example – Chiplets, Memory extension, 5G

Muti-Protocol Selection Enabled by UCIe

For General Purpose “Market Place” Chiplets

- Negotiation of protocol at link startup
- Reliable data transfer
  - CRC computation and Retry functionality
- Protocol Arbitration and Muxing
- Link State Management
- SideBand channel for
  - Protocol and Parameter negotiation with the remote Link partner
- Supporting various flit modes
  - Eg: CXL & PCIe 256B Flit and CXL 68B Flits

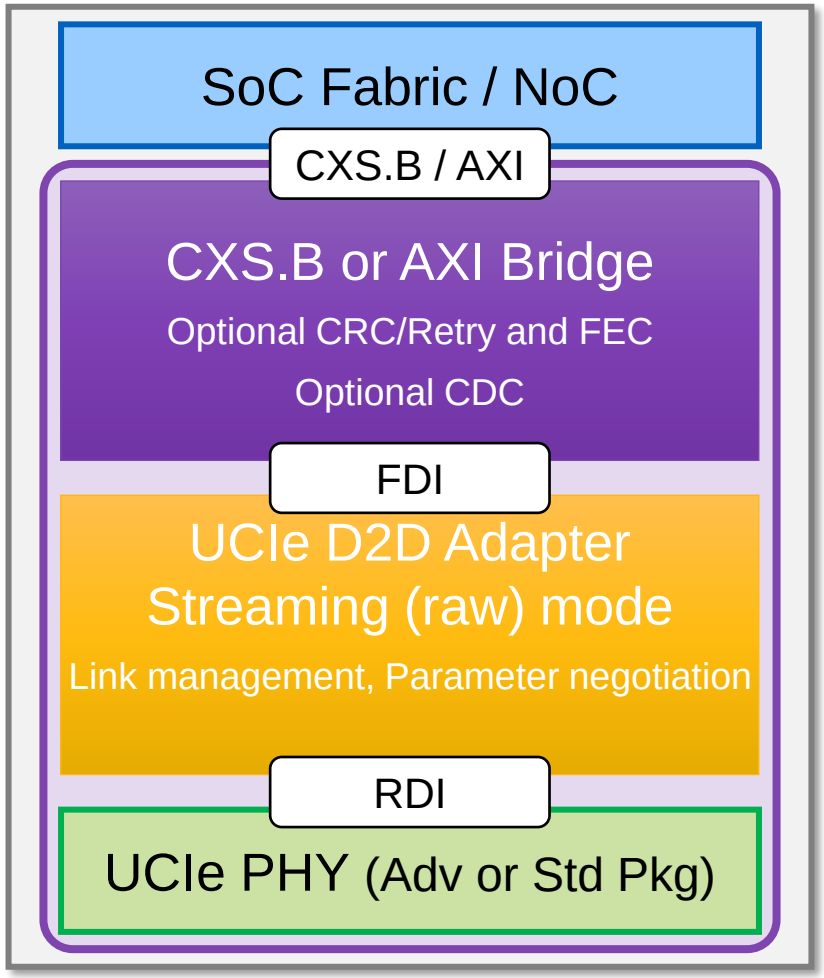


Lightweight Multi-Die NoC-NoC Bridge with UCIe

Protocol Bridge to FDI Leveraging Streaming Mode

- Low complexity D2D interconnect for compute-compute links
- Ultra Low Latency down to ~5.5ns Fabric-to-Fabric
- Supports coherent and non-coherent data traffic
- High link Reliability with CRC / Retry functionality
- Optional FEC coding minimizes BER and Retry rate, enables predictable latency links

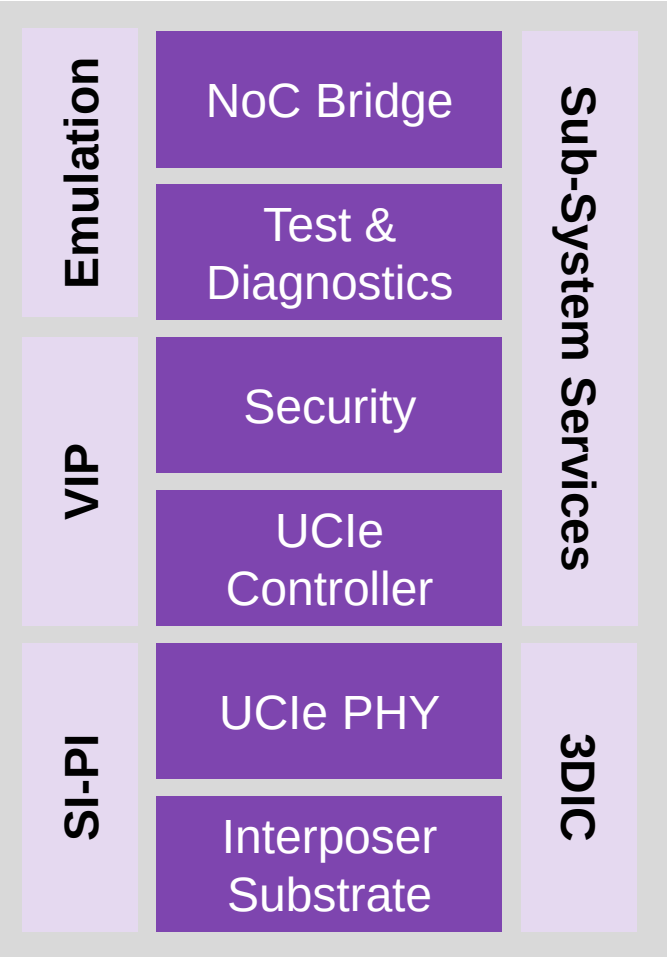
- Optimized for Compute-Compute links in Scaling & Die Splitting use cases



Synopsys UCIe Interface Solution

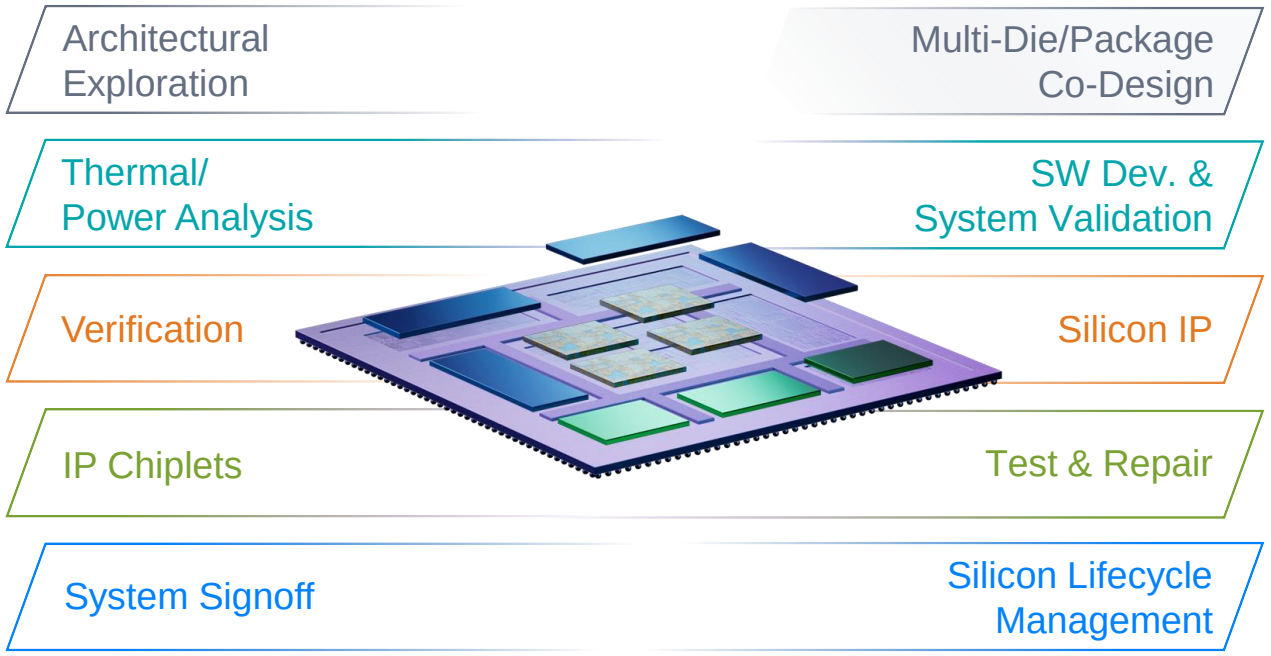
Lightweight Die-to-Die Interface for Multi-Die Systems

- Latency and Power Optimized PHY and Controller
- Support for all package technologies
- Extensive test & debug features for KGD
- Protocol stack options optimized for all use cases
- Interface to common fabric interfaces
  - CXL protocol → CXL fabric (.mem/cache) or AXI fabric (.io)
  - PCIe6 protocol → AXI fabric
  - Streaming: CXS.B or AXI bridge → CXL or AXI fabric
- Design Enablement with VIP, Emulation, Services, Design Tools



Synopsys Multi-Die System Solutions

A Comprehensive Solution for Heterogeneous Integration



Architectural Exploration	Optimize thermal, power, and performance with early exploration and partitioning
Software Dev. & Validation	Rapid software development and validation with high-capacity emulation & prototyping
Design Implementation	Efficient die/package co-design with unified exploration-to-signoff platform and robust IP
Manufacturing & Reliability	Improve health, security and reliability with holistic test and lifecycle management solutions

Thank You