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Warpage simulation methodology for assessing chip-package interaction in chiplet-based 3D stacks

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Contents

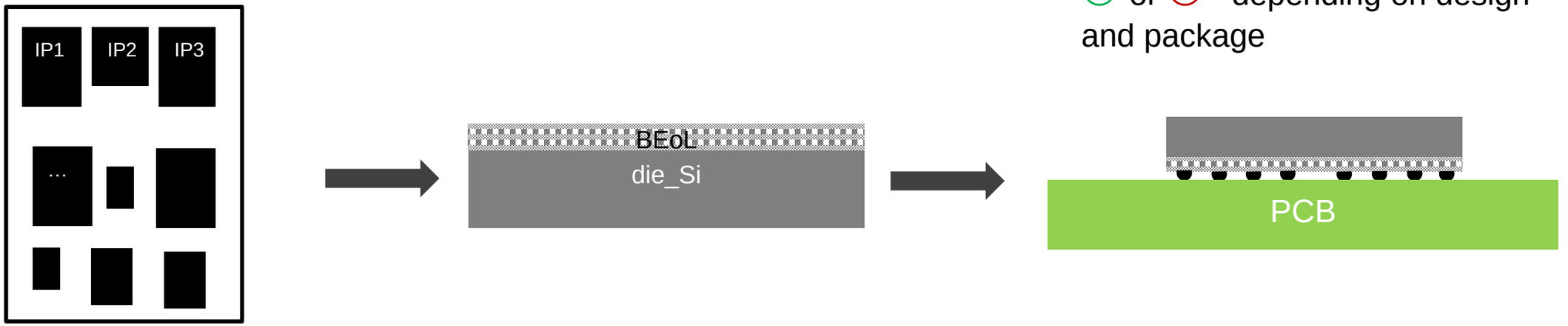
- Chip-Package Interaction (CPI)
- EDA analysis flow for CPI induced problems
- eCPI analysis
- mCPI analysis – warpage
- Conclusions

Chip-Package Interaction (CPI): the problem

Design – LVS clean ☺

Performance after chip production ☺

Performance after chip packaging/soldering ☺ or ☹ - depending on design and package



Impact of CPI on chip performance and reliability:

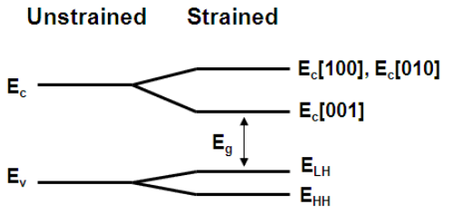
- **mechanical deformations/stresses**
- temperature increase during the operation
- electrical issues

Simulation capabilities are required to prevent IC failure after the packaging

CPI stress induced challenges

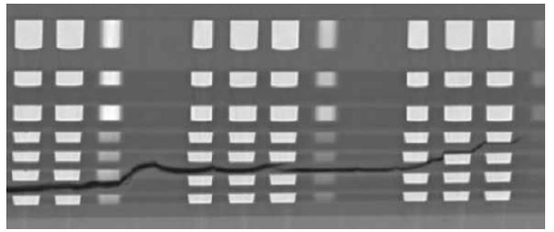
Electrical impact - eCPI

Stress impact on band structure of Si → variations in mobility and Vt in devices → changes in circuits performance



Mechanical impact - mCPI

Interconnect fracture –
cracking of ULK/ ELK dielectrics, delamination;
bump fatigue and cracking

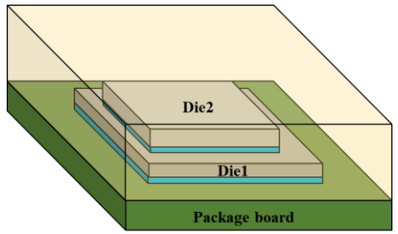


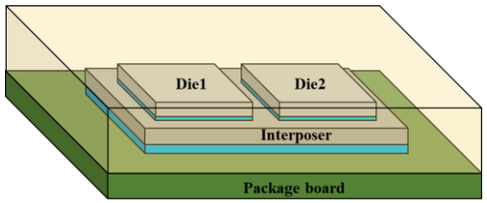
Crack propagation in a multilevel interconnect.

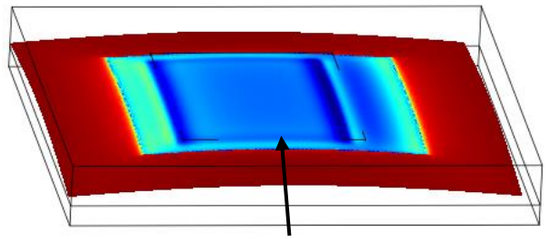
X. F. Zhang, et al., Advanced Metallization Conf., 2008.

2.5/3D IC and Chip-Package Interaction

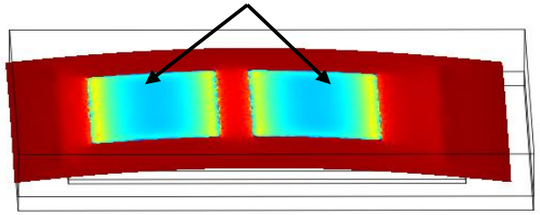
- 2.5D and 3D packages – efficient integration; but CPI stress is unavoidable.
  - mismatch of materials' thermo-mechanical properties generates stresses and causes die warpage.
  - local stress sources: solder balls and Cu pillars, TSVs, edges of neighbor dies, …

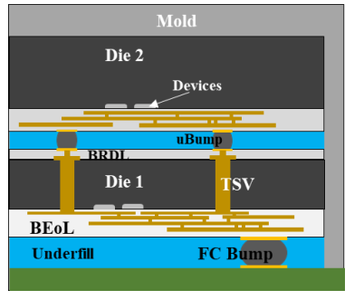


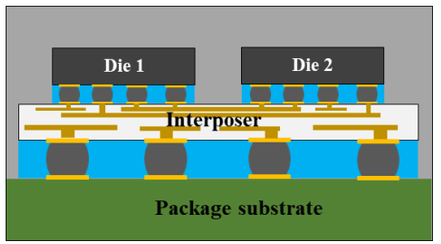




Stressed and bent dies







EDA analysis flow
for CPI induced problems

CPI stress: from package analysis to EDA flow

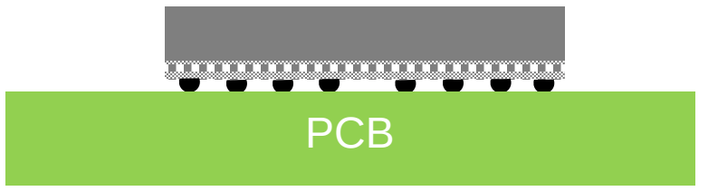
Package simulations – FEA

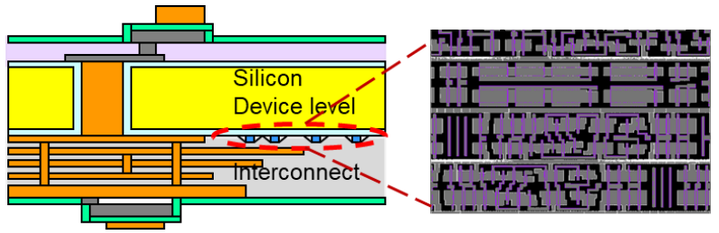
Required input:
geometry description;
material properties;
assembly process conditions

Layout analysis

Details of non-uniform composite blocks (metal layers, diff layer, C4, micro-bumps,…)

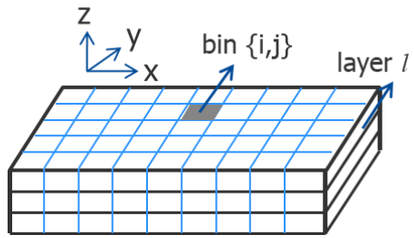
Locations/orientations of devices



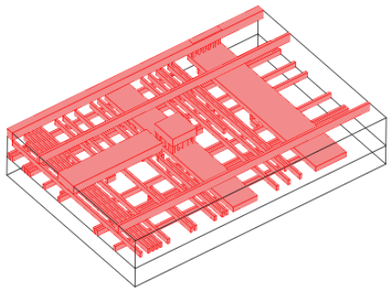


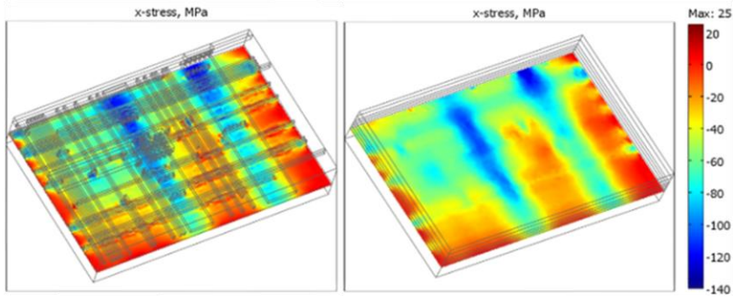
Anisotropic Effective Material Properties (EMP) for Resolving Effects of Layout Nonuniformities

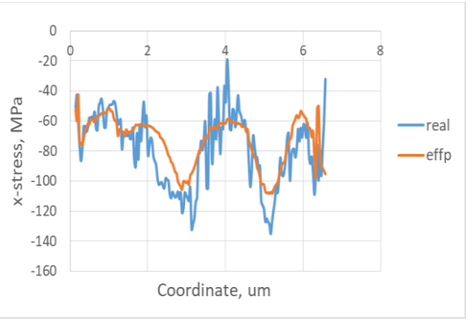
- **Effect of the layout-feature-scale variations in mechanical properties (responsible for essential variation in stress components) is accounted by introducing the Effective Anisotropic Properties of composite materials.**
- Composite layers are partitioned into rectangular bins. Different granularities are used for package-scale and IP-scale analysis.
- Metal density and routing direction in each bin are extracted by **layout extraction tools** and used for calculation of components of average Young's modulus, Poisson's ratio, and CTE in directions parallel and normal to the routing direction.



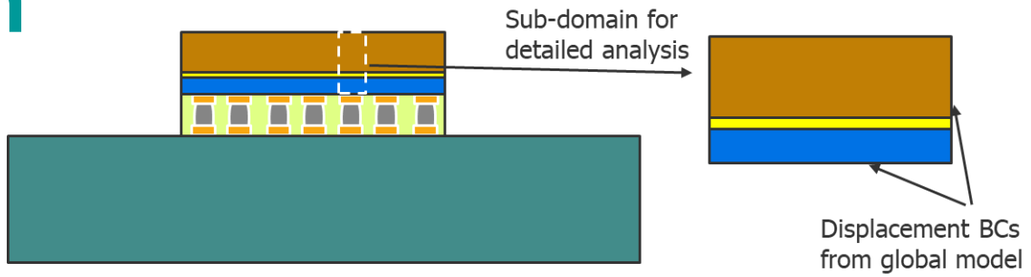
$$E_{\parallel} = E_M\rho_M + E_D(1-\rho_M),$$
$$E_{\perp} = E_M E_D/\left(E_D\rho_M + E_M(1-\rho_M)\right)$$
$$\alpha_{\parallel} = \frac{\alpha_M E_M\rho_M + \alpha_D E_D(1-\rho_M)}{E_M\rho_M + E_D(1-\rho_M)}$$
$$\alpha_{\perp} = \alpha_M\rho_M + \alpha_D(1-\rho_M)$$
$$\nu = \nu_M\rho_M + \nu_D(1-\rho_M)$$



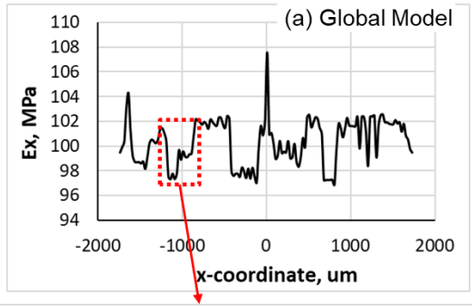


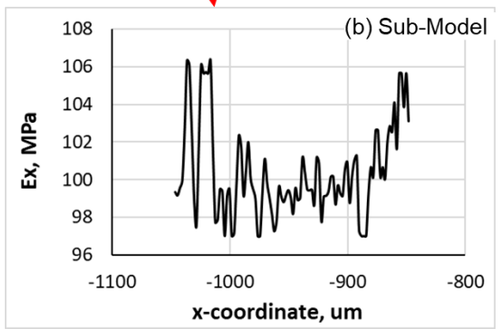


Multi-Scale Simulation



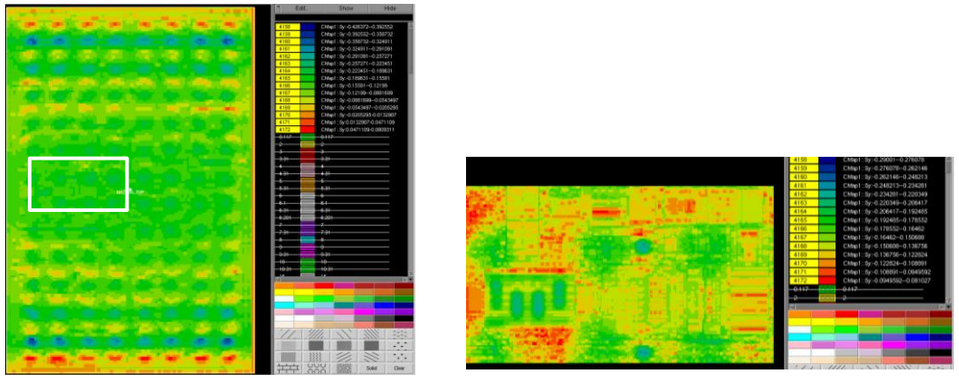
- Multi-scale in dimension: thickness varies from “mm” (PCB) to “sub-micron” (device layer).
- Very fine FEA mesh/EMP grid is required for device and BEoL
- Solution: multi-step simulation with displacement boundary conditions that transfers the obtained global-scale stress distribution on surfaces to successive sub-modeling.



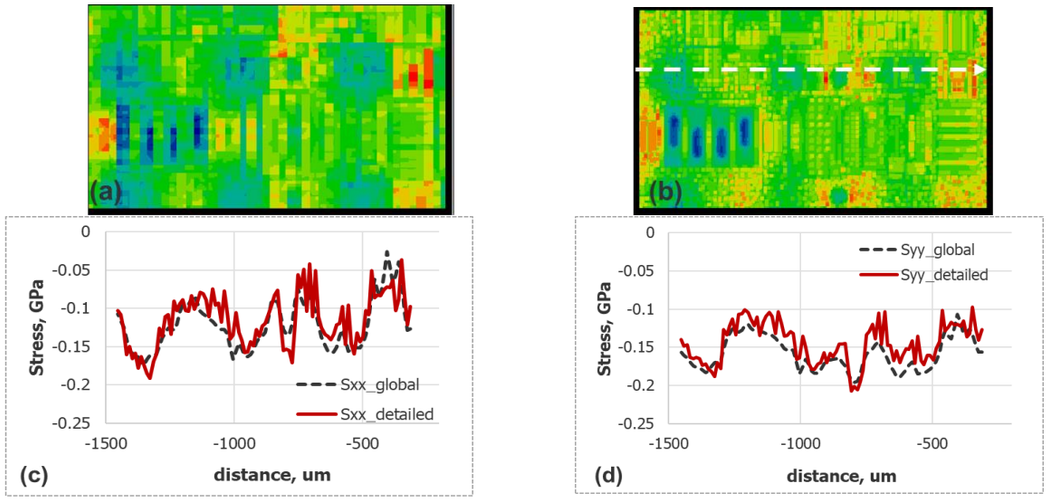


Multi-Scale Simulation - results

- Die-scale stress colormap imposed on the layout for visual detecting suspicious regions/IPs
- IP-scale stress colormap for detecting suspicious layout features



Bending stress simulation



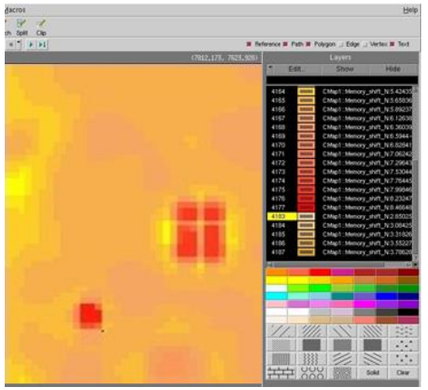
Thermomechanical stress simulation

A. Kteyan et. al, Proc. International Symposium on Physical Design (ISPD), (2022)

eCPI: electrical

eCPI: Stress Impact on Circuits Performance

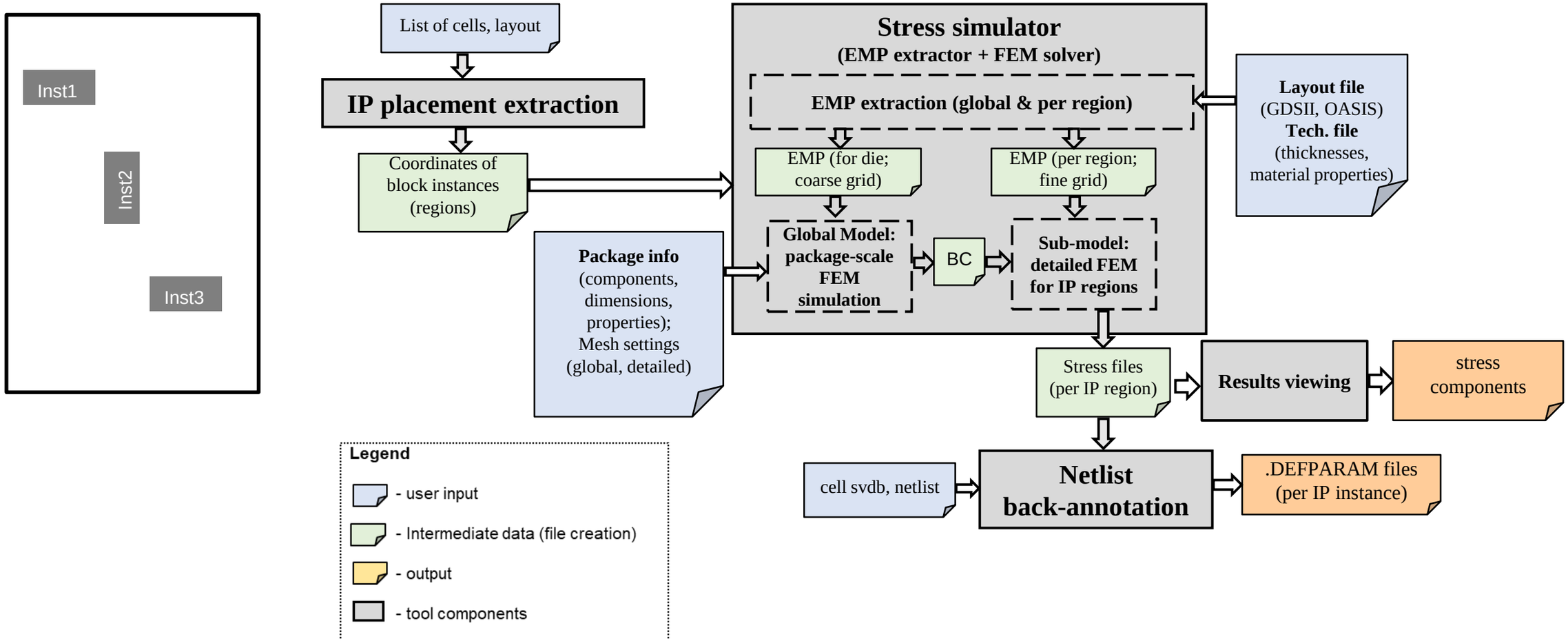
- Mobility shift $\Delta U/U0 = -(\pi_l\sigma_l + \pi_t\sigma_t + \pi_z\sigma_z)$: silicon crystal orientation and channel direction
- Change of current ΔI
  device size, electric field (SPICE device models)



Complex analysis of CPI stress impact:
- **stress simulations**
- **circuitry/device locations**
- **device models**

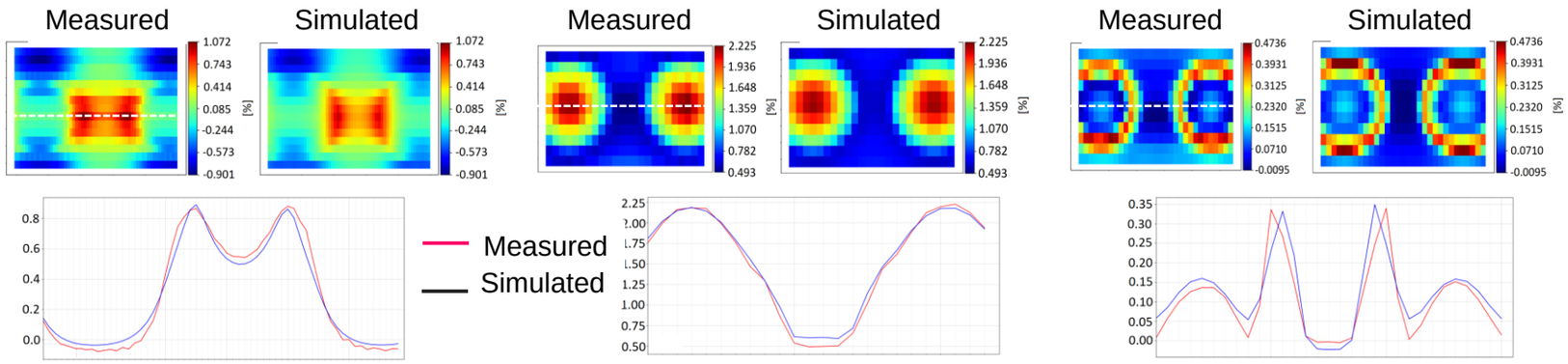
- **Avoid circuits performance risks by modifying layout at floor-planning stage**
- **Final sign-off with account of stress impact**

eCPI: assessment flow



eCPI: experimental validation

- WLCSP die contains matrices of MOS, resistors and BJT devices. Multiple placements of each matrix across die.
- Measurements of electrical characteristics of all device instances enable to separate out stress impact on electrical performance of devices.
- Simulated stresses were transformed to current variations: $\Delta I = \pi_{\parallel}\sigma_{\parallel} + \pi_{\perp}\sigma_{\perp} + \pi_{out}\sigma_{out}$ (“∥”, “⊥” along and across electric current flow, and “out” for out-of-device plane)
- Good agreement of measured and simulated device characteristics.

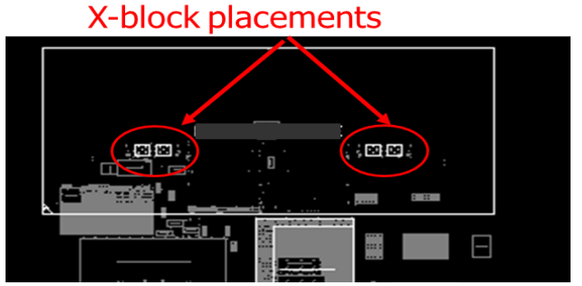


(a) ΔId of MOSFETs (b) ΔIc of BJTs (c) ΔR of resistors

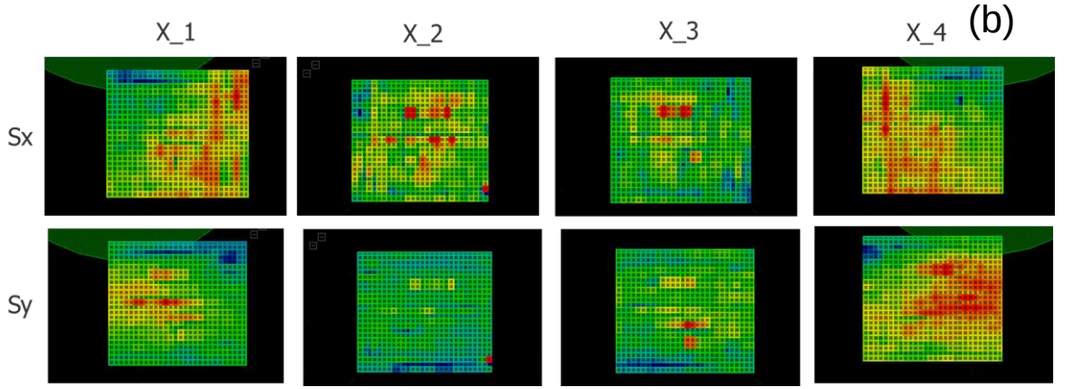
A. Kteyan et. al, Proc. International Symposium on Physical Design (ISPD), (2022)

eCPI: What-if Analysis for Circuit Block Placement

- Performed during the design floor planning step, for optimization of the IP-block placement in terms of stress effects.
- A user-supplied average metal density can be used for extracting BEoL EMP when routing is not available: stress variation due to C4 bumps, die edges.
- Designers define several different locations for the studied block, and obtain SPICE netlist annotated with stress components for each placement instance.
- Four instances of the same X-block in different layout environment exhibit different distributions of the X- and Y-stress components.



(a)

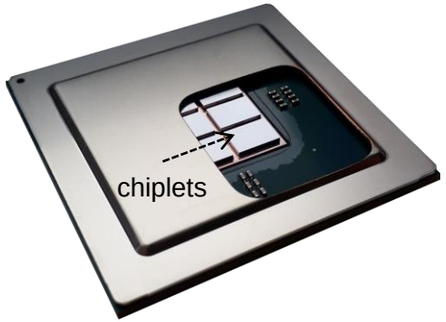


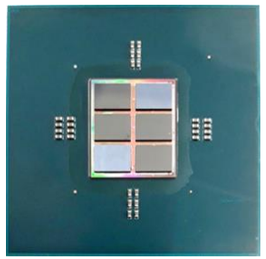
(b)

mCPI: mechanical

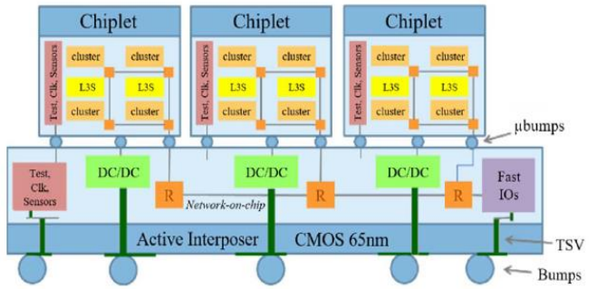
mCPI: calibration on warpage measurements

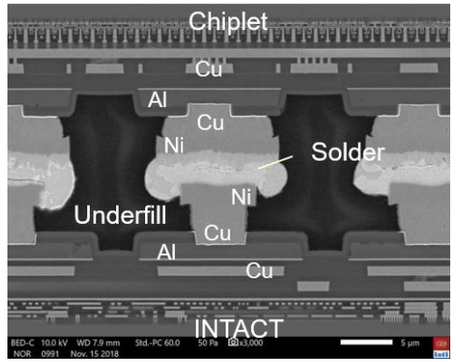
- Calibration on electrical measurements may not be available in pre-design stage during process development.
- Warpage measurements on package components can be employed for model calibration.
- Altitude measurements during heating, and subsequent cooling, on INTACT package components – chiplet, active interposer, PCB.
- Measurement tool: Altisurf 520 (Altimet)





INTACT demonstrator

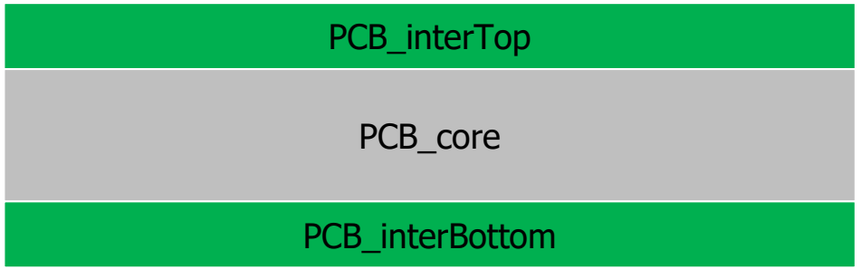




P. Coudrain, et al., Proc. IEEE Electronic Components and Technology Conference, (2019).

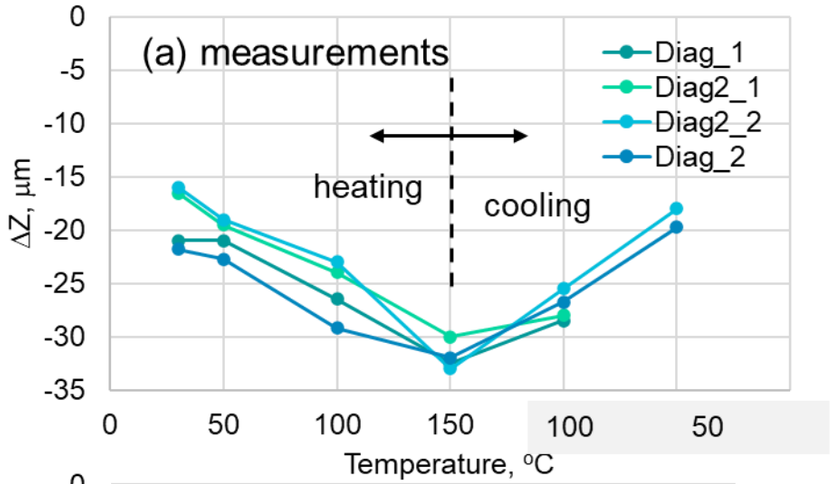
PCB model

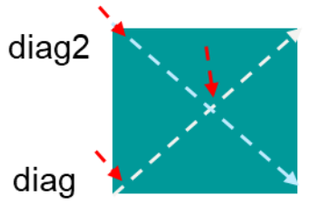
- Employ three blocks.
- For each block, extract uniform smeared EMPs - (E: Young's modulus, CTE: thermal expansion coeff., P: Poisson ratio) by employing known properties of {conductor, insulator}, thickness, and routing directions for consisting layers.
- These properties are further calibrated by fitting temperature dependent warpage measurements.

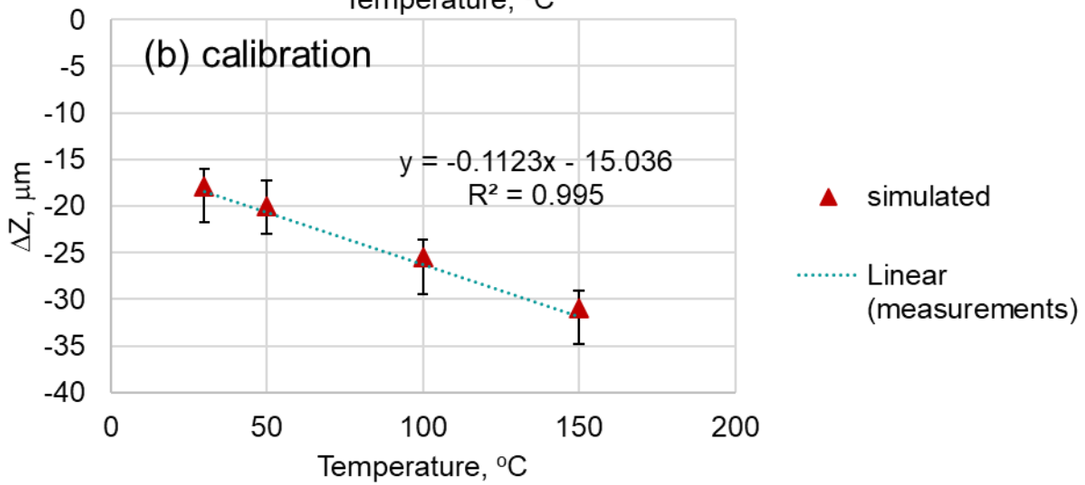


mCPI: calibration on PCB warpage measurements

- Model calibration: altitude measurements on a top surface of a stand alone PCB, across two diagonal directions during heating and cooling.
- After parameters adjustment, good agreement is found between measured average altitude (ΔZ), and simulated warpage values.
- Calibration continues for other stand-alone components: interposer, chiplet.

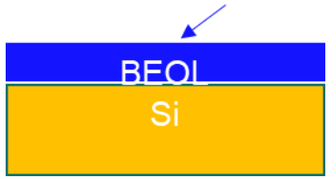


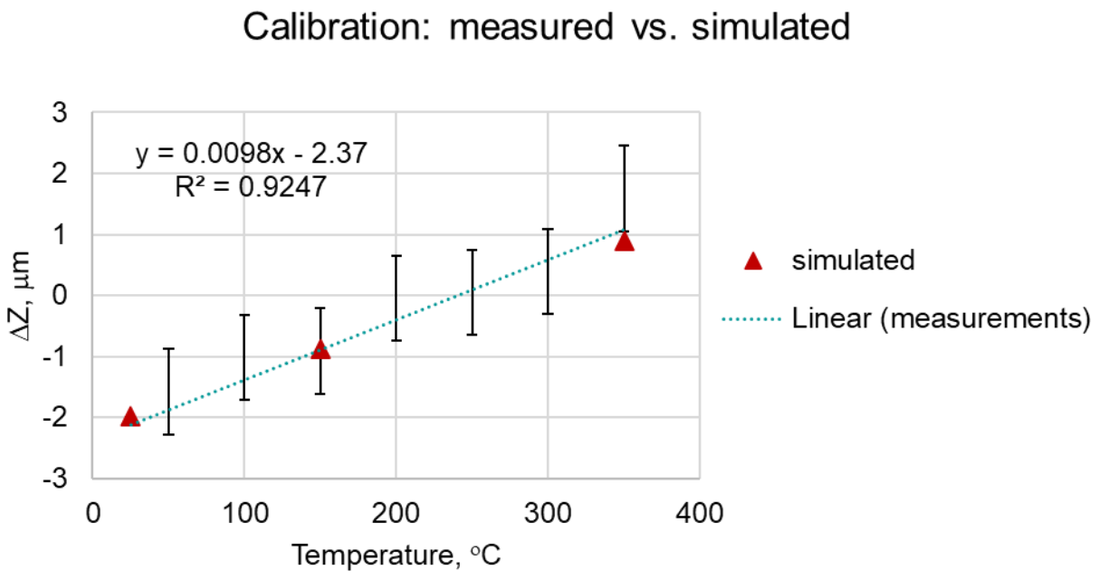




mCPI: calibration on chiplet warpage measurements

- Warpage on BEOL top surface.
- Uniform smeared BEOL properties are calculated after extracting properties of individual layer: (E, CTE, P), by employing known properties of {conductor, insulator}, thickness, and routing directions of consisting layers.
- These properties are further calibrated by fitting temperature dependent warpage measurements.

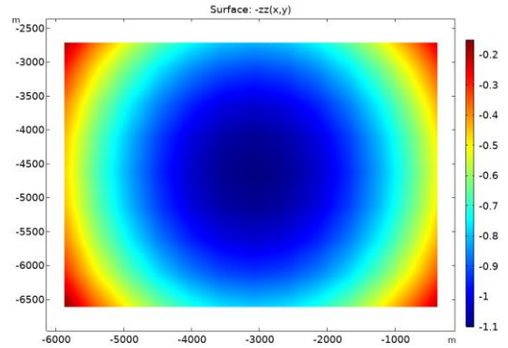


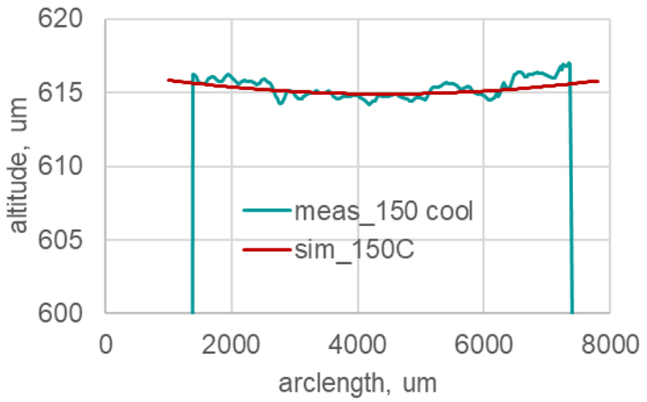


Chiplet warpage simulation (1)

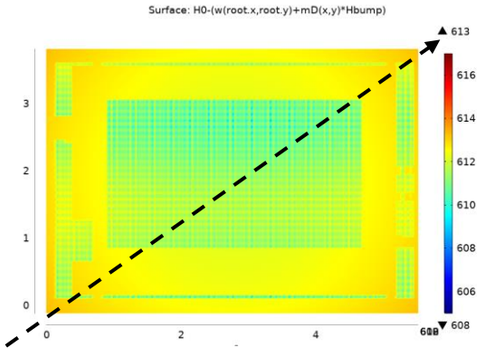
T=150 °C

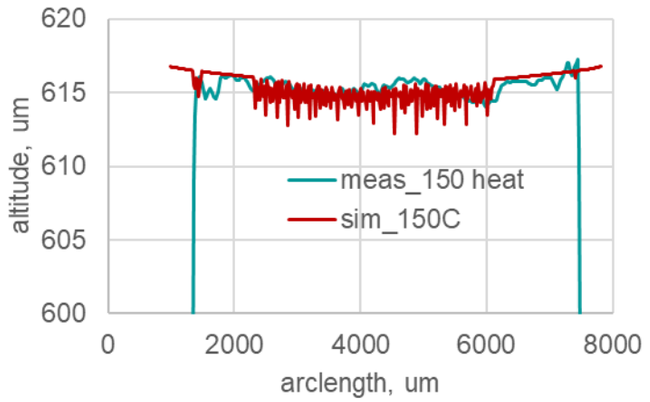
Simulated:
Uniform BEoL properties



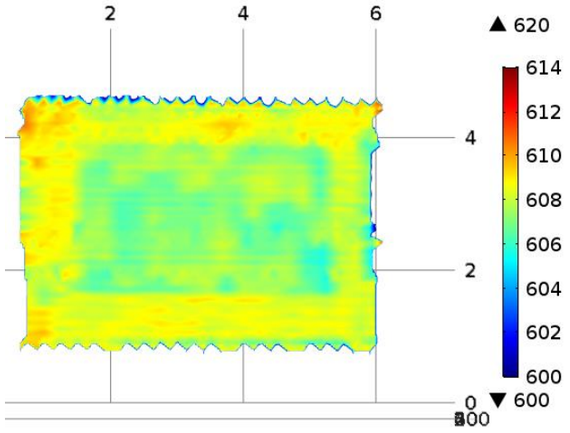


Simulated:
EMP(x,y) for μBump





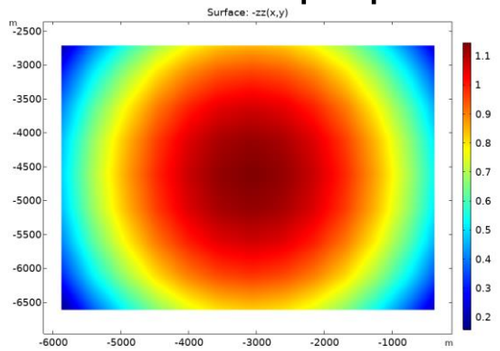
Measured

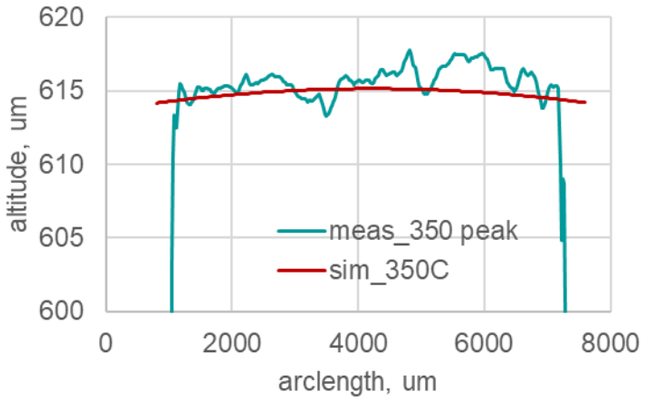


Chiplet warpage simulation (2)

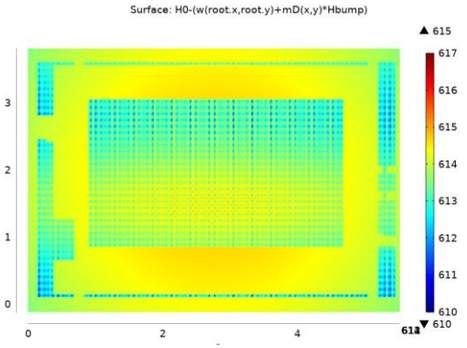
T=350 ºC

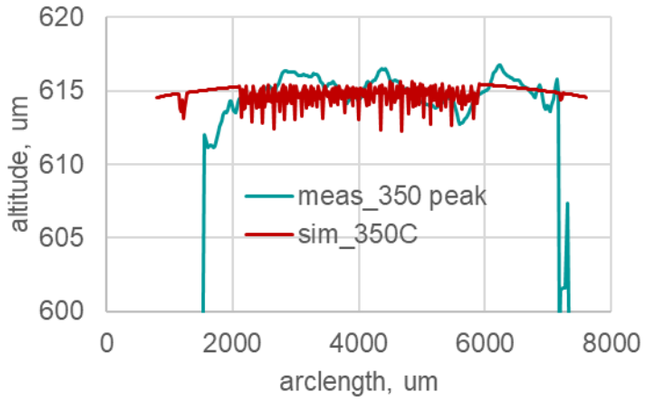
Simulated:
Uniform BEoL properties



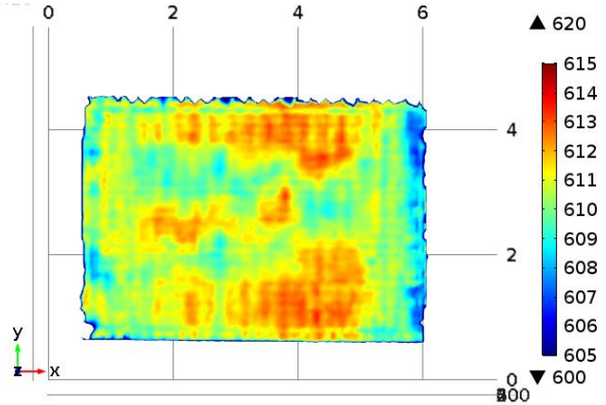


Simulated:
EMP(x,y) for μBump



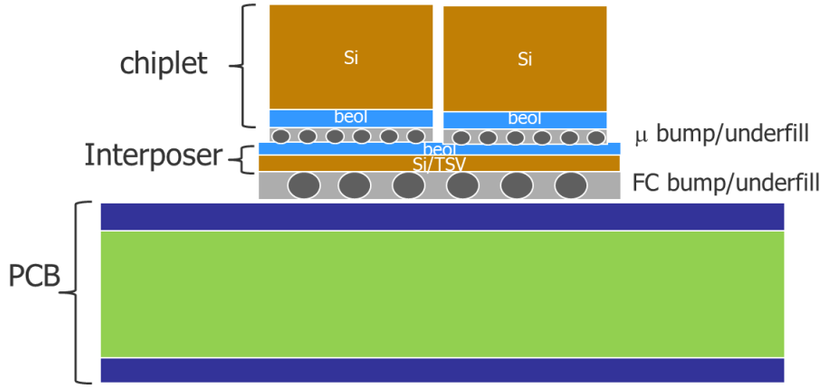


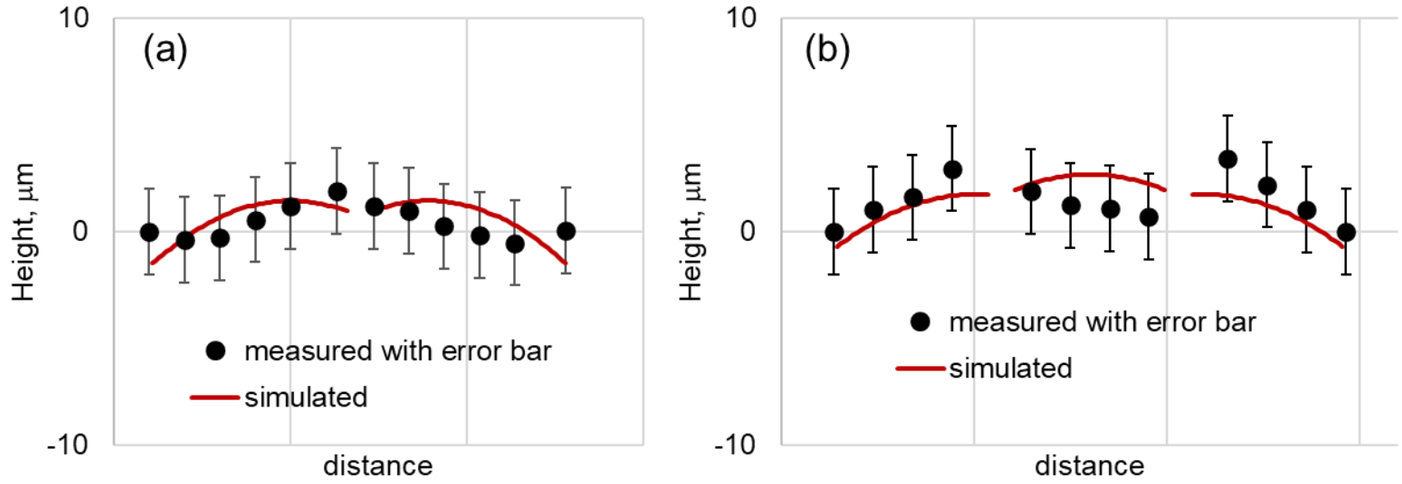
Measured

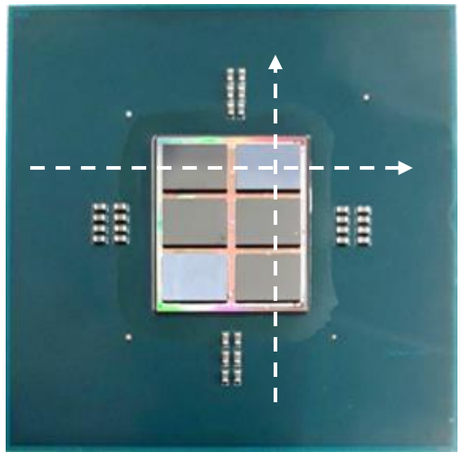


mCPI: warpage prediction on full stack package

- Simulated 1D profile on a full stack package at room temperature, after model calibration.

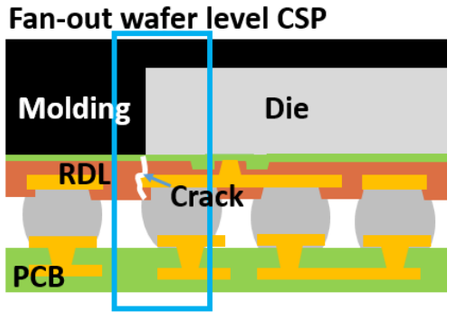






Interconnect Reliability Analysis (mCPI)

- Highly stressed regions are prone to interconnect fracture - cracking of ULK/ ELK dielectrics, interconnect delamination.
- Probabilistic nature of cracking: depends on distribution of micro-defects in ILD (pores, flaws)
- Analysis of stress distribution in each layer is required for detecting possible cracking/delamination.



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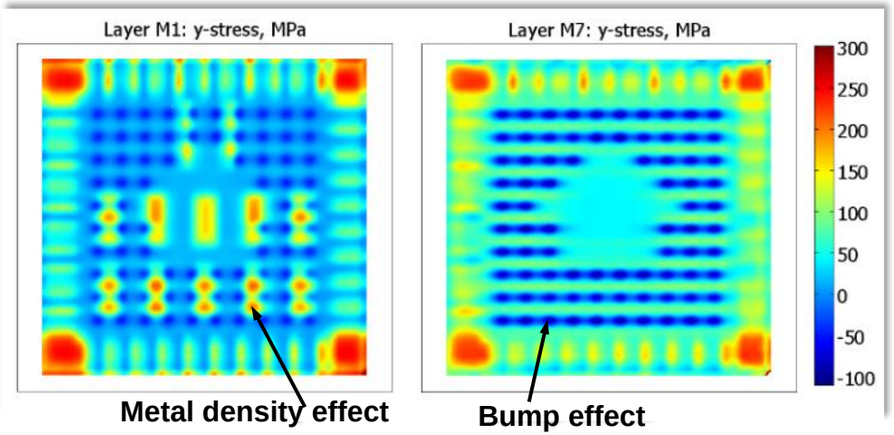
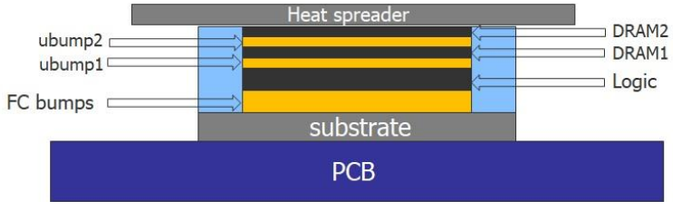
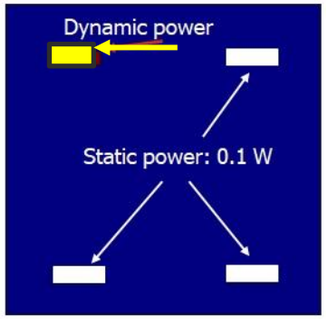
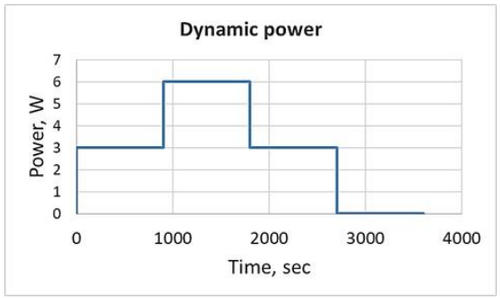


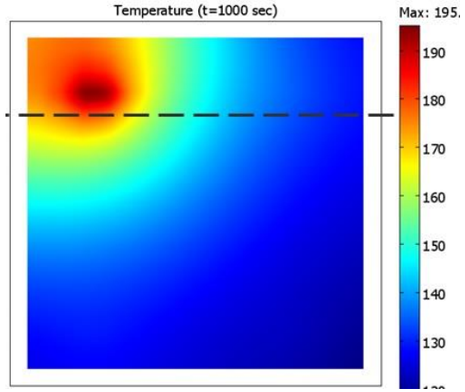
Assessment of Temperature and Stress during Chip Operation

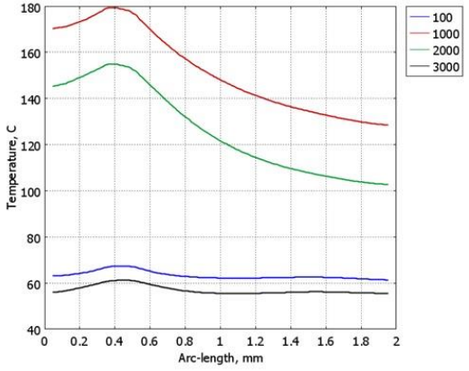
- **Thermal-mechanical FEA** allows assessing the stress in the stack during chip operation

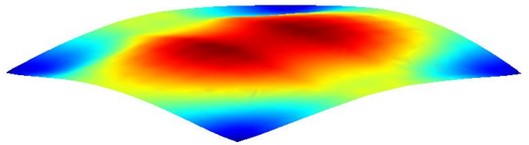




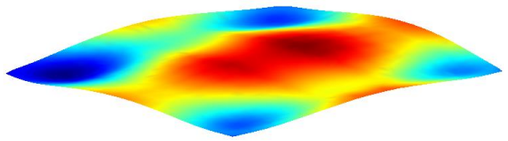








Packaging induced warpage (t=0)



Warpage evolution due to heating (t=1000)

Conclusions

- Combining FEA simulations with layout analysis capabilities allows obtaining CPI stresses with any desired resolution, by applying multi-scale simulation technique.
- EDA methodology for assessment of CPI stress impact on circuits performance has been developed by linking stress analysis with SPICE simulations
- For the purpose of mechanical failure analysis in the early stage of a package design, the warpage measurements can be used for the tool's calibration.
- Analysis of the CPI stress distribution in chip metallization is performed for estimation of interconnect fracture probability; linked thermal-mechanical simulations - for operational stresses.

Acknowledgement

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