Chiplet-Based
Heterogeneous Advanced Packaging
Keith Felton – Siemens EDA
Agenda

Introduction
Architecture definition
System planning and design
Multi-physics analysis
Device-level test planning
Manufacturing & reliability
Chiplet based heterogeneous packaging
Disaggregation disrupting traditional tools and methods

Transition to system-based optimization from design-based optimization
• Die-die and die-package connectivity definition, planning, and optimization
• Die, package, board cross-domain influences and interactions

Expanding supply chain and tool ecosystem
• Sharing/updating content in a multi-vendor/tool environment, independent verification
• Process specific design enablement (PDK/ADK/CDK)

Balancing design resources across competing multi-domain requirements
• Recognizing the impact of early, critical decisions on resource utilization, cost, & performance
• Greater visibility into the impact of downstream effects earlier in the design process
Chiplet based Heterogeneous Integration Functions

Architecture
Identify and map chiplets/D2D PHYs to Vendor Libraries
High level power, thermal, throughput analysis
Select appropriate package technology
Capture viable design scenarios
Preliminary floorplan/routing
Assess PPA, cost using STCO flow

Verification
Substrate DRC using PDK
Function verification using LEC
Assembly LVS using ADK

Place & Route
3D enabled physical layout of SIP, Chiplet, silicon interposer, and package substrates
Physical IP reuse and concurrent team-based design

Electrical Analysis
Parasitic extraction, system level power and timing analysis of die, interposer, and package
Static/dynamic IR drop and electro-migration analysis
Automated interface compliance analysis

Mechanical Integration
Managed co-design of mechanical parts such as stiffeners and heat spreaders with a fully documented ECO flow between ECAD and MCAD.
Access to mechanical analysis

Thermal & Stress
Thermal analysis from transistor to system-level – chiplet, interposer, package, system
Detailed die-level thermal analysis with accurate package and boundary conditions
Co-simulation and optimization of thermal-mechanical stress effects

DFT & Test
Hierarchical DFT, SSN (Streaming Scan Network), enhanced TAPs (test access ports) and IEEE 1687 IJTAG.
Scalable, flexibility, and ease-to-use, help designers optimize test technology resources.
Pivoting from Design-level to System-level Optimization

Architectural
- SIP/SOC partitioning
- Scenario exploration

Manufacturing
- Testability
- Thermal/stress/reliability

Verification
- Functional
- 2.5D/3D assembly

Physical
- SIP/SOC floor planning
- Stacking configuration

Performance
- Signal integrity
- Bandwidth and picojoule/bit

Power
- Power integrity
- PDN planning

System Technology Co-Optimization (STCO)
5 Workflows that deliver the 7 functions of Heterogeneous Integration
Architecture Definition

Architectural Planning & Analysis workflow

- SiP Level decomposition
- Define SiP level IO & chiplet components
- Define CTC/D2D interfaces/protocols
- Create D2D interconnect
- CTC/D2D IP Mapping/Analysis
- Early SiP Floor planning
- Early Power Network Planning
- Trade-off and scenario exploration
- Select optimal micro-architecture design

Viable Chiplet Scenarios
- Custom/Std Chiplets

Viable Design Scenarios
- SIP Netlist 1
- SIP Netlist 2
- SIP Netlist N

Optimal Design Scenario
- SIP Netlist (V)
- SiP Power Intent (UPF)

Functional Simulation

Predictive modeling with high-level design abstractions

System Level product/design metrics

Thermal/Mechanical
- Power
- Cost

Signal Integrity
- Area/Form factor

Power Delivery

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System planning and design

Co-Design Planning & Prototyping

- Data aggregation & design setup
- Device placement & stacking definition
- Net list definition & connectivity optimization
- Data path planning & route feasibility
- Mechanical part feasibility
- Trade-off and scenario exploration
- Predictive modeling to qualify scenarios
- Export of qualified implementation data

Qualified design ready for implementation

Design Intent (Architecture)
- Verilog

System PCB Design
- Critical comps
- Interface info
- Optimized pkg

Chiplet Designs
- IO & bump info
- Interface info
- Floorplan/keep-outs

Signal Integrity
Power Integrity
Thermal Analysis
Route Feasibility
Mechanical Design

Predictive modeling with high-level design abstractions

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Physical design workflow

Physical Substrate Implementation

- Detailed constraint import & setup
- Detailed placement – stacking, embedding, etc.
- Collaborative mechanical part optimization
- Design routing including high-speed tuning
- Power plane/striping and degassing generation
- Physical IP block reuse and team-based design
- SI/PI and DFM validation
- Generate manufacturing outputs & docs

Qualified design ready for implementation

PDK/ADK/CDKs Tech templates

In-process identification/resolution of overt SI/PI, DFM & thermal errors to minimize sign-off iterations

Signal Integrity

Power Integrity

Mechanical Design

Thermal Analysis

In-process DFM

Manufacturing Outputs

GDS
OASIS
Gerber
ODB++
IPC-2581
Others…
Multi-physics Analysis

Design Analysis workflow
- Silicon (PEX)
- Organic (PEX)
- Signal Integrity Analysis
- Power Integrity Analysis
- SiP IR Drop/EM Analysis
- SiP STA
- Timing Simulation
Test Planning & Validation workflow

Test Planning & Validation workflows:
- Chiplet Test IO Planning
- Test Bus Planning
- Test Bus Routing
- Test Timing (STA)
- Test Functional/Timing Simulation Support
- Wafer Level Die Test IO Planning/Validation

Test Timing Analysis
- Timing Simulation
- Static Timing Analysis
- Package PEX
- Interposer PEX
- Chiplet CDX (UB)
- Materials PDK
Reliability Analysis workflow

- Chiplet/Stacked Die Thermal Analysis
- Package/System Thermal Analysis
- Thermo-mechanical Stress Analysis
- Thermal/Stress Co-design/Optimization
- Reliability ERC checks
- DFM signoff checks

Design Data

- Chiplet Design(s)
- Package Design
- Mechanical Package Design

IP Data

- ASIC/Interposer PDK
- Package IP & ADK/DRM
- Materials PDK
- Chiplet CDK

Package Design Chiplet/Material Models

Thermal Analysis

- Chiplet/Stacked Die Layout(s)
- Materials PDK
- Chiplet CDX (GDS2, JEP30)
- Chiplet CDX (ECXML)

Stress Analysis

- Thermal Analysis
- Package Design
- Device Level
- Co-Design/Optimization
- SIP Level

Design Signoff

- Substrate DFM
- Die/Interposer DFM
- SIP D2D Latch-up
- SIP D2D ESD/EOS
- Die Level Latch-up
- Die Level ESD/EOS
- DFM & Reliability Verification
HI of chiplets using an advanced package brings multiple benefits

- Lower wafer costs
- Simpler die/chiplet designs
- Lower power
- IP reuse
- Faster time-to-market
- Better overall system performance

Disrupts traditional packaging methods and design tools

Can deliver more than Moore
Thank You!

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Keith Felton
Product Marketing – Semiconductor Packaging
EBS Division
Siemens EDA

Phone +1-508-303-5806

E-mail keith.felton@siemens.com