January 24 - 26, 2023
DoubleTree by Hilton San Jose
ChipletSummit.com

Creating a Vibrant Open Chiplet Economy

Morning Keynote - Thursday, January 26th 11:30 am

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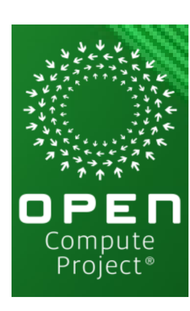


The Rise of Diverse Domain-Specific Architectures

Machine Learning
Neural Networks
Deep Learning
Pattern Recognition
RT Translation
Robotic PAs
Autonomous Vehicles
NLP
Cognitive Security
Block Chain

Modern Computation

Standard Computation

Graphics

HPC

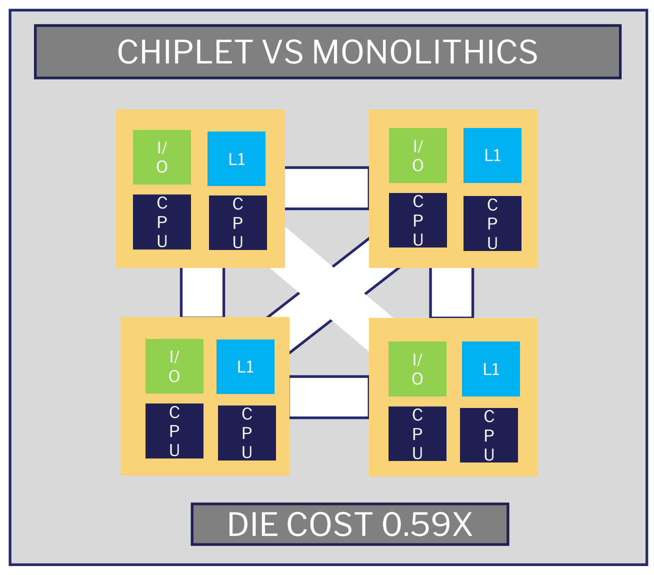
Early Compute Era

General Purpose CPU

AI and Machine-learning and data-heavy workloads have exploded in past 5 years and will diversify as new applications are discovered constantly…

Chiplet Motivations

Proven Chiplet Business Models



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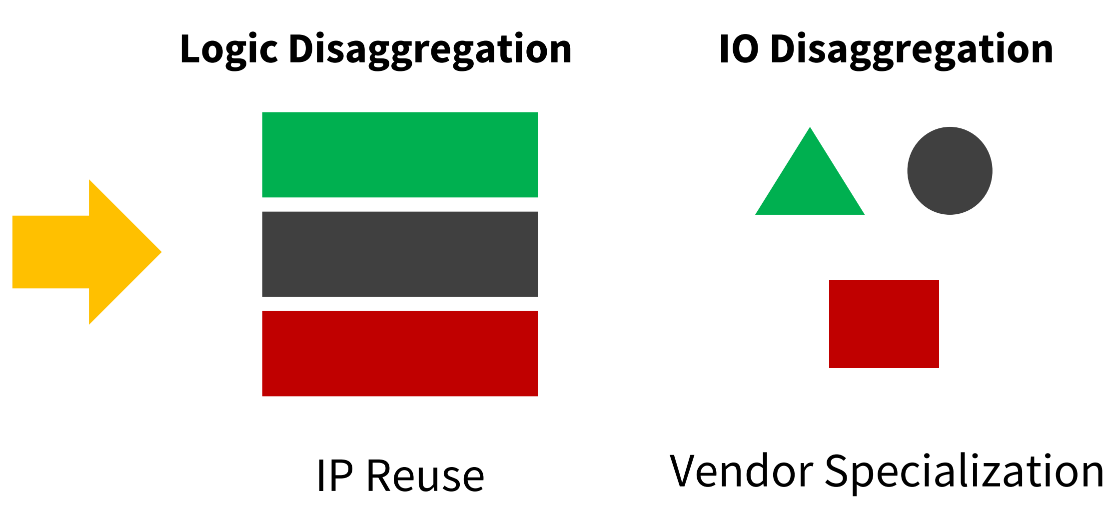


Chiplets Will be Everywhere Chips Are…

Semiconductor worldwide revenue by end vertical, sales (source: Gartner)

End vertical	Example	% of total 2020	% of total 2025E	2025 revenue projection	2021E-2025E% CAGR
Automotive	ADAS, Infotainment Chassis	8.3%	12.0%	$80.2B	12.4%
Communication	Smartphones	32.9%	31.5%	$210.3B	3.0%
Consumer	TVs, Digital Set-Top Box	10.4%	10.5%	$70.3B	2.6%
Data processing	PCs, Servers, Storage Media	37.7%	33.8%	$225.6B	1.6%
Industrial	Automation, Healthcare, Security	10.7%	12.1%	$80.7B	8.5%

Accenture: Harnessing the Power of the Semiconductor Value Chain

…Need new integration across the Value Chain

Customer specification

Design and verification

Semiconductor Foundry

Assembly, packaging, and test

Contract manufacturing

OEM and products

Semiconductor supply chain

OPEN Compute Project

Can One Size Fit All?

Semiconductor worldwide revenue by end vertical, sales (source: Gartner)

End vertical	Example	% of total 2020	Power	I/O	Other
Automotive	ADAS, Infotainment Chassis	8.3%	10s of W	10s of Gbps	Long life
Communication	Smartphones	32.9%	< 10 W	Gbps	Rapid churn
Consumer	TVs, Digital Set-Top Box	10.4%	< 10 W	Gbps	Cost sensitive
Data processing	PCs, Servers, Storage Media	37.7%	100s of W	100s of Gbps	Rapid churn
Industrial	Automation, Healthcare, Security	10.7%	10s of W	10s of Gbps	Harsh environment

Accenture: Harnessing the Power of the Semiconductor Value Chain

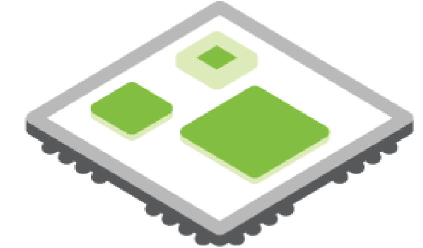
Linux: Model for Innovation

- Anyone can modify
- Many domain specific distributions
- Unrestricted use, unstoppable growth

For a Chiplet Economy

To meet huge diversity in requirements we need

- A core set of standards
- A low barrier to entry for innovation
- Freely usable, customized for applications



Build and let the market use as it sees fit

Establishing a New Open Chiplet Economy

Chiplet Vendors

Open Marketplaces

ASIC (SiP) Builders

End Users

IP Providers

EDA

Manufacture

Tools

Support Ecosystem

Open Platform
Standards, Tools, Business Workflows

Platform Elements for Rapid Growth

	Business Workflow	SiP Integration	SiP Design	Chiplet Interconnect
Standards		Digital Chiplet Physical Descriptions Modularity	Digital Chiplet Functional Descriptions	PHY layer Link layer Trans. layer
Tools and Reference	SiP cost models Known-Good Die contracts	Package Analysis & Tools Device Test	Architecture Exploration Test Package	Selection Guides Channel models Open Designs
Production Support	Business Logistics	In-field management	Chiplet Catalog	

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Enabling Business Workflows

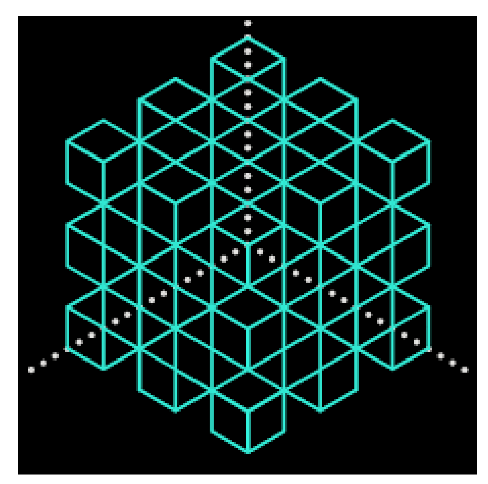
- SiP Cost Models
  - Comparing SiP costs with single die implementation design and manufacturing costs
- Known-Good Die
  - SiP scrapped if even just a single die is faulty
  - New supplier-vendor models
  - Better test coverage
- Business Logistics
  - Revised inventory models
  - New EOL practices

Simplifying SiP Integration

- Digital Chiplet Physical Descriptions
  - Machine readable chiplet physical descriptions
- Modularity
  - Standardized physical form factors for components to enable automated SiP assembly
- Package Analysis & Tools
  - Thermal and power delivery
  - Mechanical design
  - Assembly and manufacturing
- Device Test
  - Chiplet test, full package test
- In-field management
  - Operation, management, telemetry

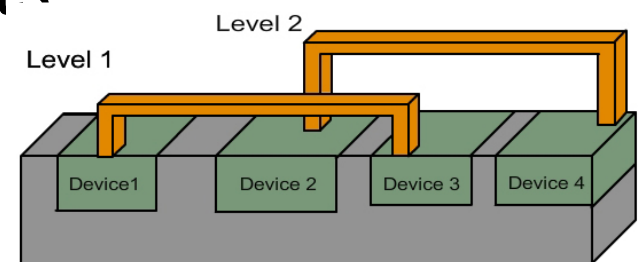
Automating SiP Design

- Digital Chiplet Functional Descriptions
  - Digital descriptions to represent functional data
- Architecture Exploration
  - Tools to explore power, performance and cost tradeoffs
- Test Package
  - Reference packages using various technologies
- Chiplet Catalog
  - A catalog of Chiplets including data on chiplet status, use in designs



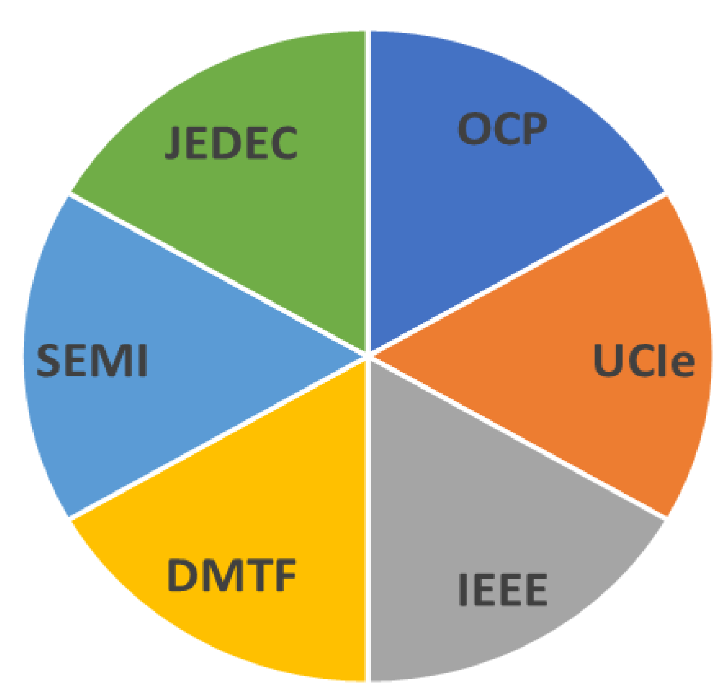
Chiplet Interconnect

- Interface Specifications
  - PHY, Link and Transaction layers
- Selection Guides
  - Criteria for choosing the best interconnect that meets requirements
- Channel Models
  - Open models to aid with interface design and implementation
- Open Design
  - Open source design to spur innovation



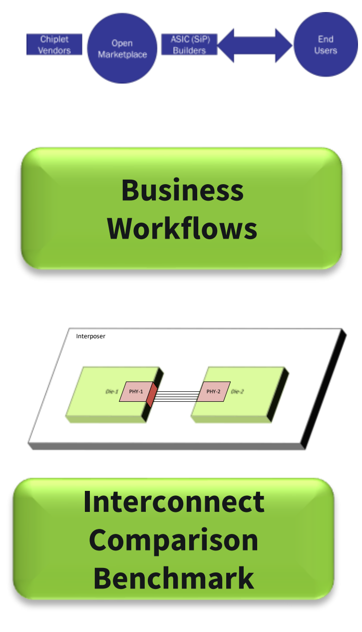
Will take a Village

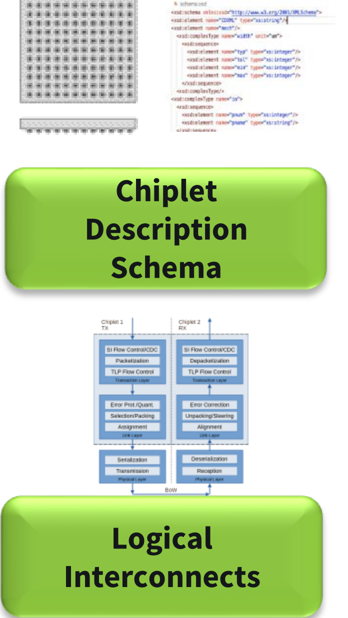
- JEDEC: Microelectronic Industry Standards
- OCP: Modularity and DC Requirements
- UCIe: Chiplet Interconnect & Market Development
- IEEE HIR: Packaging & Assembly Roadmaps
- DMTF: Device Management
- SEMI: Business Models

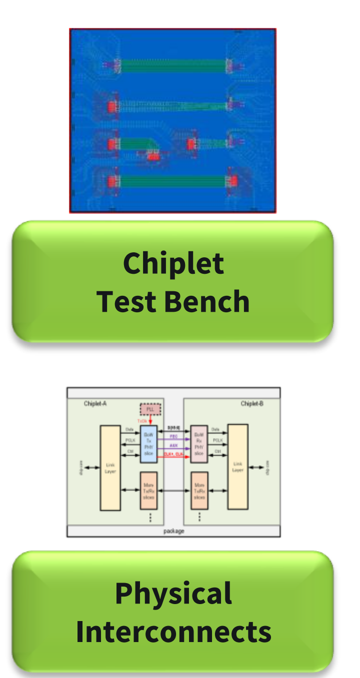


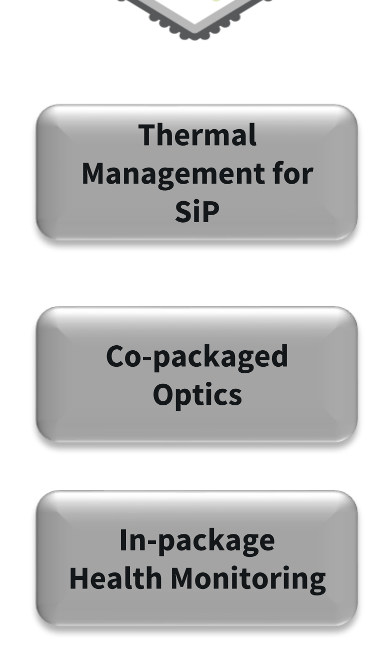
OCP Investing to establish an open Chiplet Economy
(Accelerating advanced computing)

Open Domain Specific Architecture Project

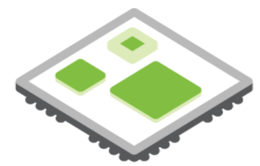




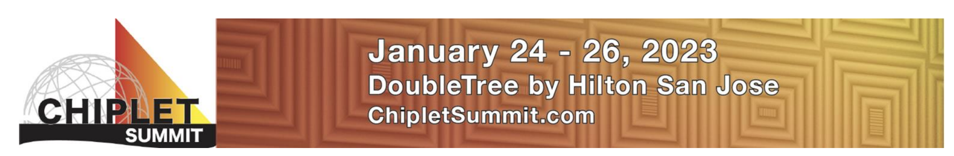




ODSA Accomplishments

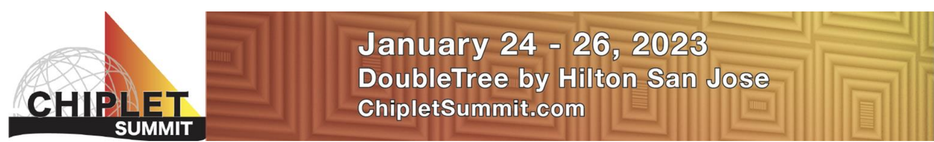


- Business Workflows
  - Design and manufacturing cost trade-off model and tool
  - DoE whitepaper developing the Chiplet Economy concept
- Chiplet Description Schema
  - Automating System in Package (SiP) design and build
- Chiplet Test Bench
  - Multi-vendor Chiplet interop PoC w design guide
- Interconnect Comparison Benchmark
  - Standardized & widely used benchmark metrics for interconnects
- Logical Interconnects
  - Link layer specification (Draft)
- Physical Interconnects
  - Open HBI specifications
  - Bunch of Wires (BoW) specifications
    - Applied to AI, CPU, FGA Chiplets & many prototypes



2023 Plans

- Business Workflows
  - Refine chiplet economy proposal
  - Die disaggregation cost model
- Technical Workflows
  - CDXML 2.0
  - Modular packaging
- Chiplet Test Bench
  - Complete Multi-vendor Chiplet interop PoC w design guide
- Interconnect Comparison Benchmark
  - 2023 Release
- Logical Interconnects
  - Link layer specification (Draft)
  - Link control protocol specification
- Physical Interconnects
  - Bunch of Wires next



Top Takeaways

- Market is diverse, the will be many domain specific solutions
- For rapid innovation, we need low barriers to entry to include more participants
- Open communities are critical to accelerate the Open Chiplet Economy

How YOU can get Involved

- Participate in OCP ODSA Project Workstreams
- Invest to build the Chiplet Economy
  - Chiplets, Tools, and Services

Join
- Project Mailing Lists
- Project Calls

Drive
- Project Focus
- Thought Leadership

Run
- Project Leaders
- Technical Steering Committee

Contribute
- Specifications
- Products & Facilities