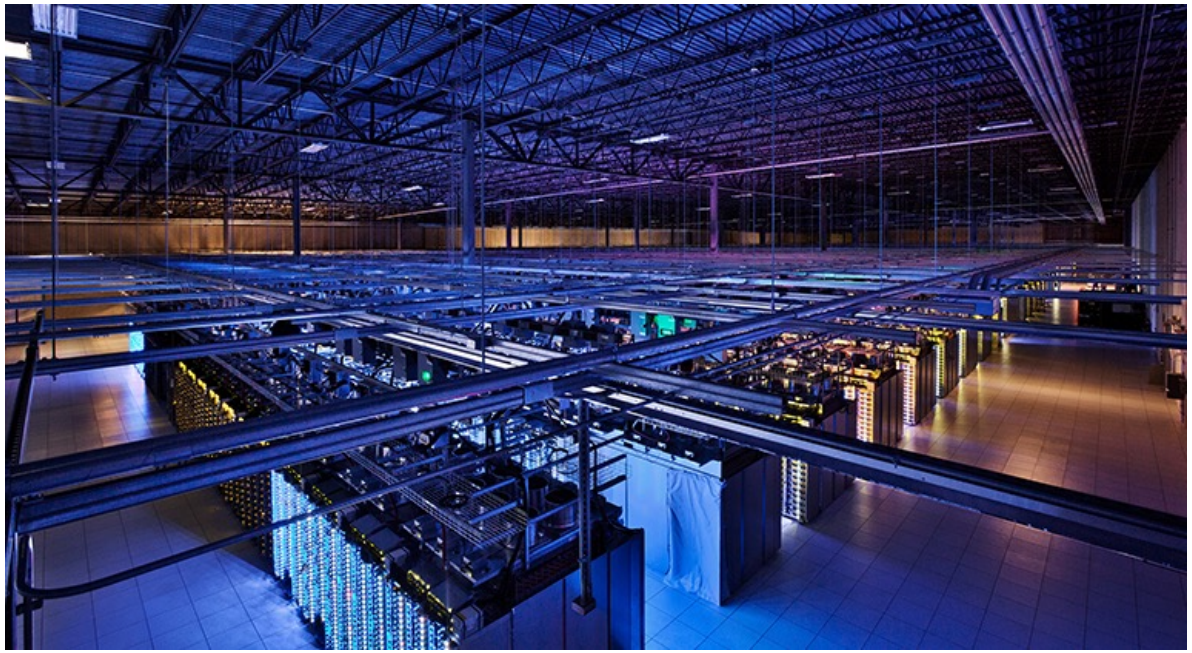
Using Silicon Photonics in a Co-Packaged Optical Interconnect

Manish Mehta
VP of Marketing and Operations – Optical Systems Division

February 6th, 2024

Datacenters: Systems At Scale



$100B Annual Capex Spend by Cloud with 15% CAGR[1]

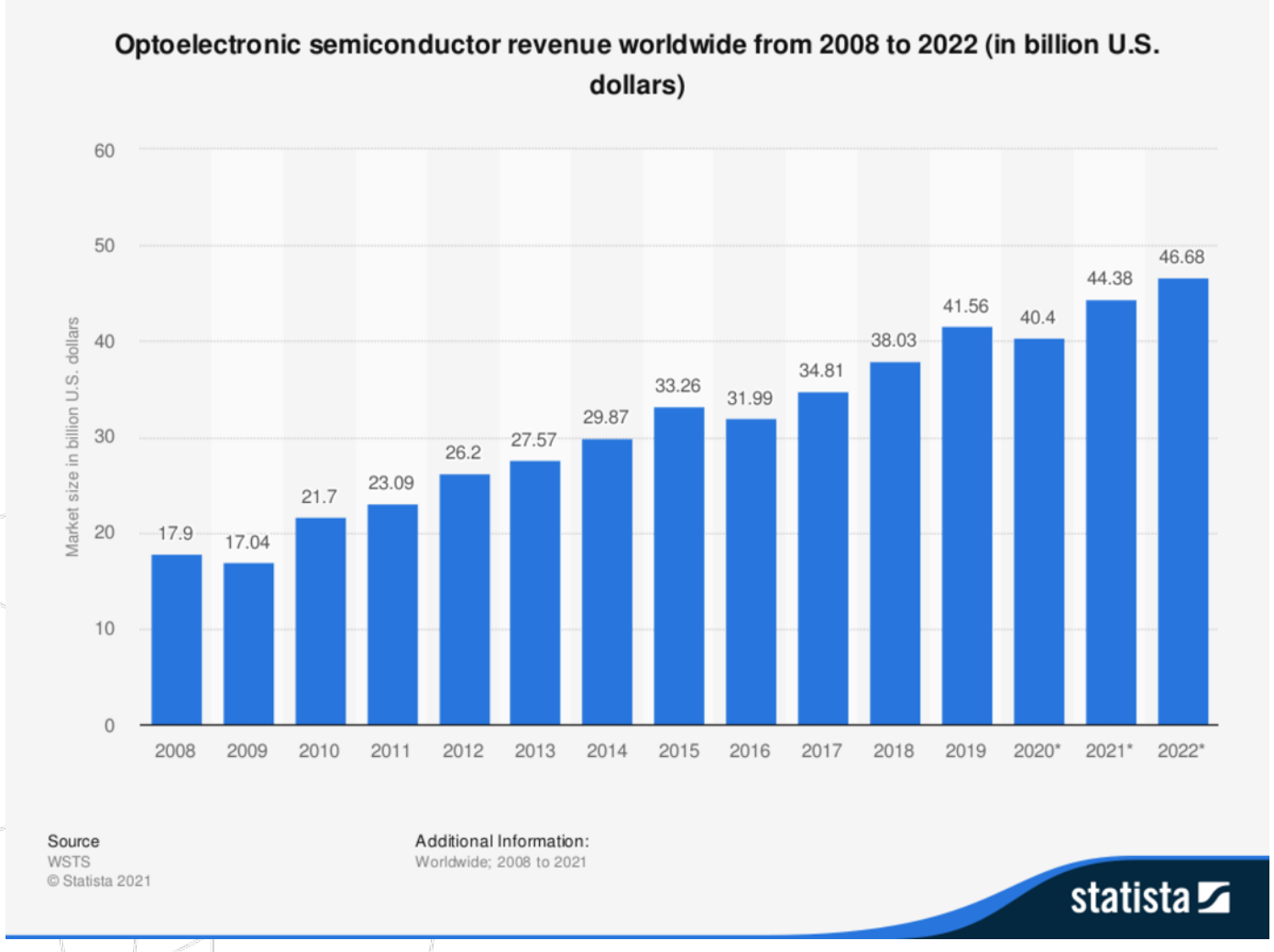
19.5 Zettabytes of Cloud Data Movement[2]

Per hyperscale datacenter
> 100k Servers
> 10k Switches
> 1M Optical Interconnects

Source:
1. 650 Group, Cloud Total Market and Forecast Report
2. Cisco Global Cloud Index, https://blogs.cisco.com/news/acceleration-of-multicloud-era
3. Left: Digital Realty's Loudoun Three campus in Ashburn, Virginia. Photo courtesy of Digital Realty
4. Right: Google's Council Bluffs, Iowa Data Center. Photo courtesy of Google

BROADCOM

The Increasing Role of Photonics Within Semiconductors



Source: Statista 2021

$45B

Optical Semiconductor Market

$1B → $3B → $4.6B

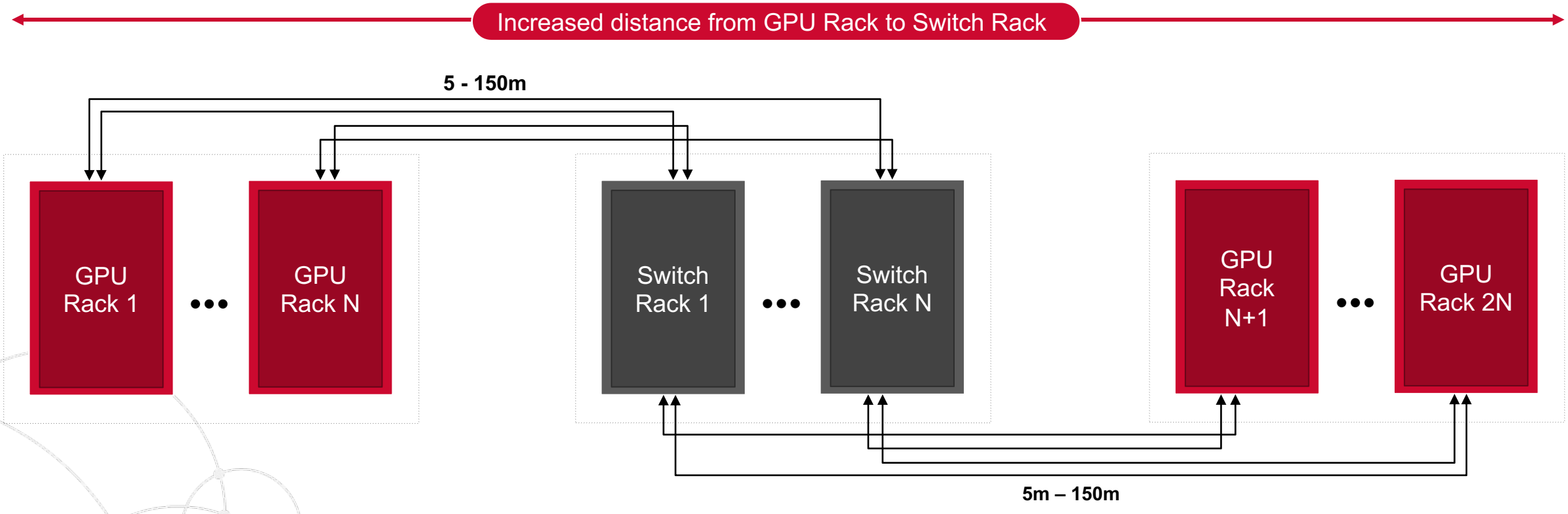
2020 2025 2027

Global Silicon Photonics Market[1,2]

1. Markets and Markets, Silicon Photonics Market with COVID-19 Impact Analysis by Product
2. Emgen Research

BROADCOM

AI Cluster Trend: Interconnect Distances



Clusters > 32k GPUs in deployment

Difficult for copper interconnect to support GPU clusters larger than 64

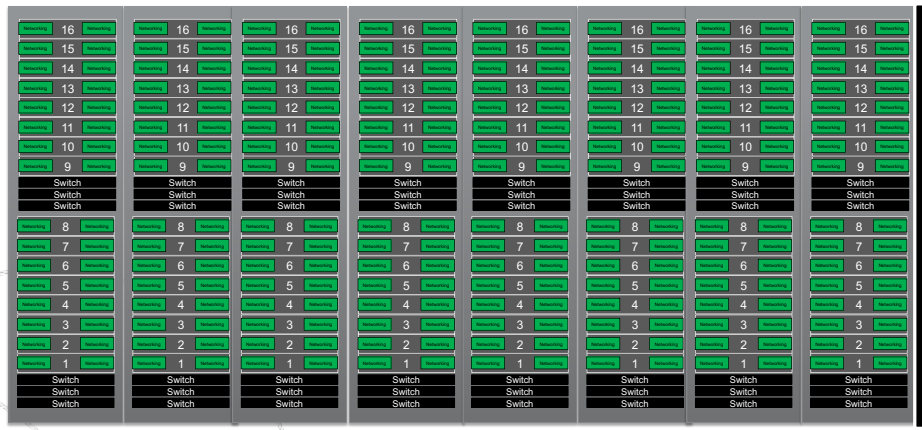
Single-mode optics needed for speeds > 106Gbps and distances > 100m

Multi-mode optics could be used to support 106Gbps at < 100m

BROADCOM

AI ML Cluster Example: 256 GPUs with 51.2T Switches

102.4TB/s



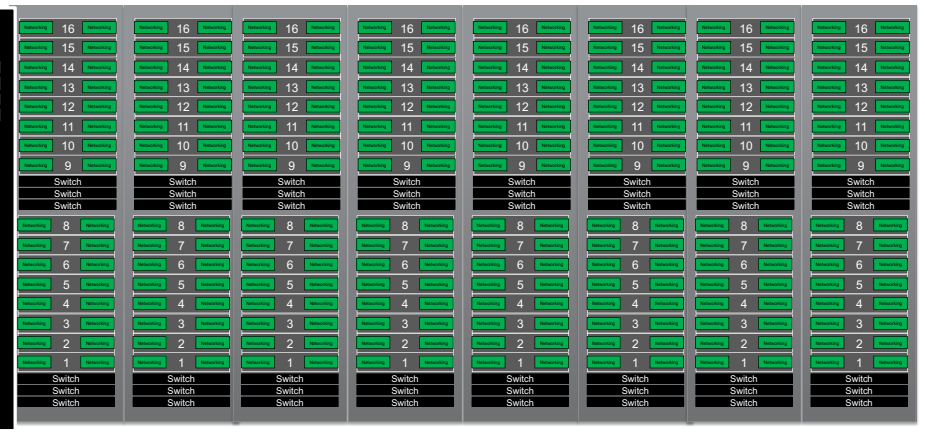
8 RACKS

16 GPU/Rack | 6.4Tbps/GPU

32x

51.2T TH5 Switches

102.4TB/s



8 RACKS

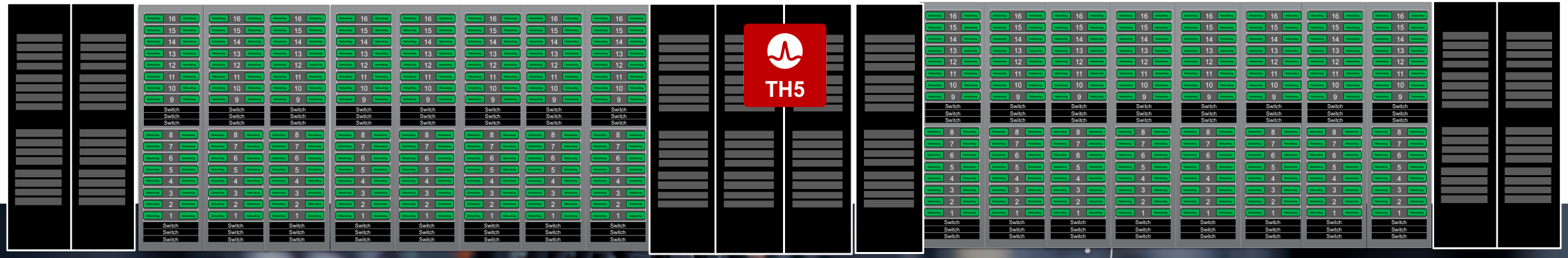
16 GPU/Rack | 6.4Tbps/GPU

BROADCOM

AI ML Cluster Example: Scale-out

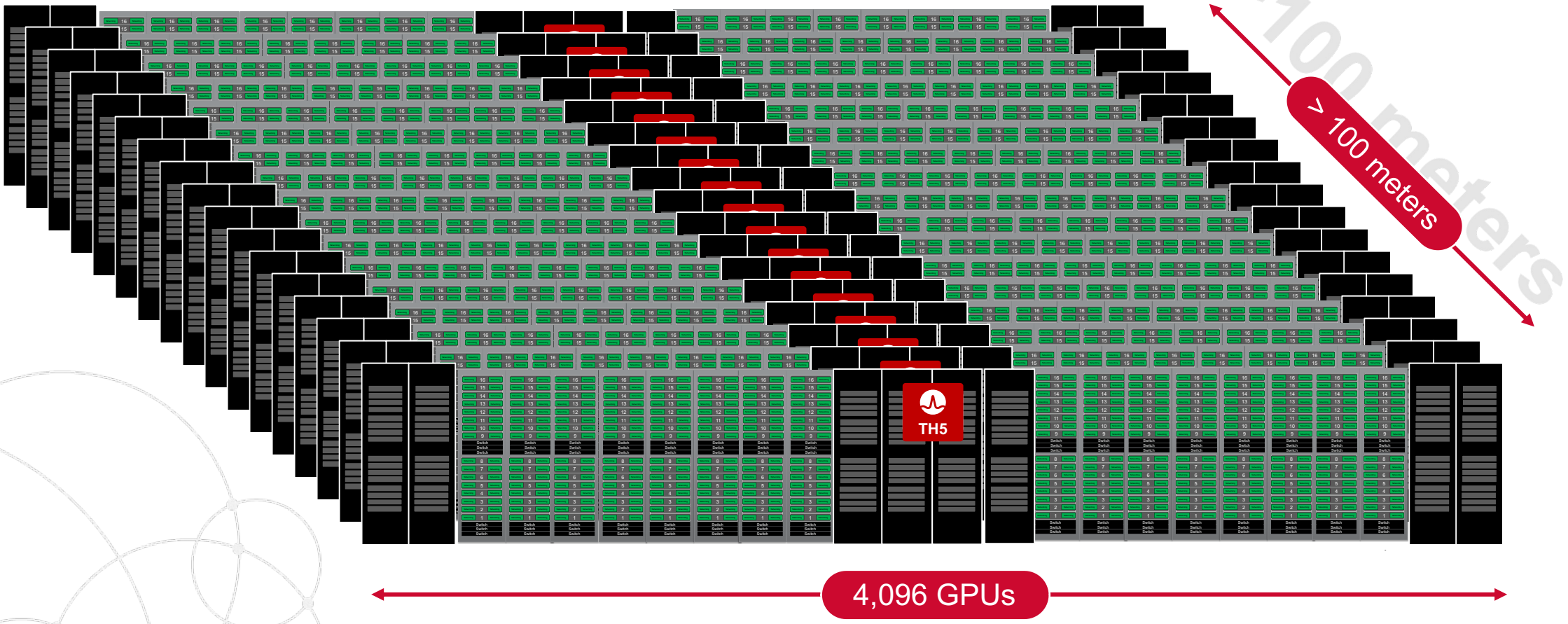
30 meters

256 GPUs



BROADCOM

AI ML Cluster Example: Scale-out

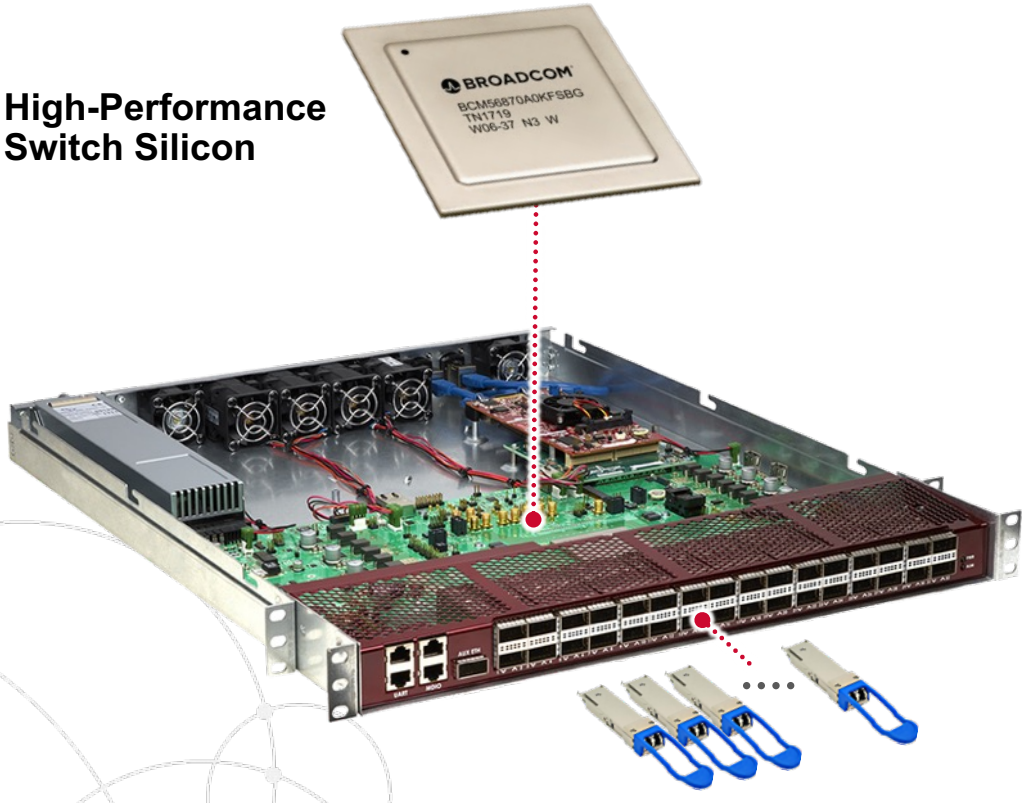


Optical Interconnect required between GPU pods

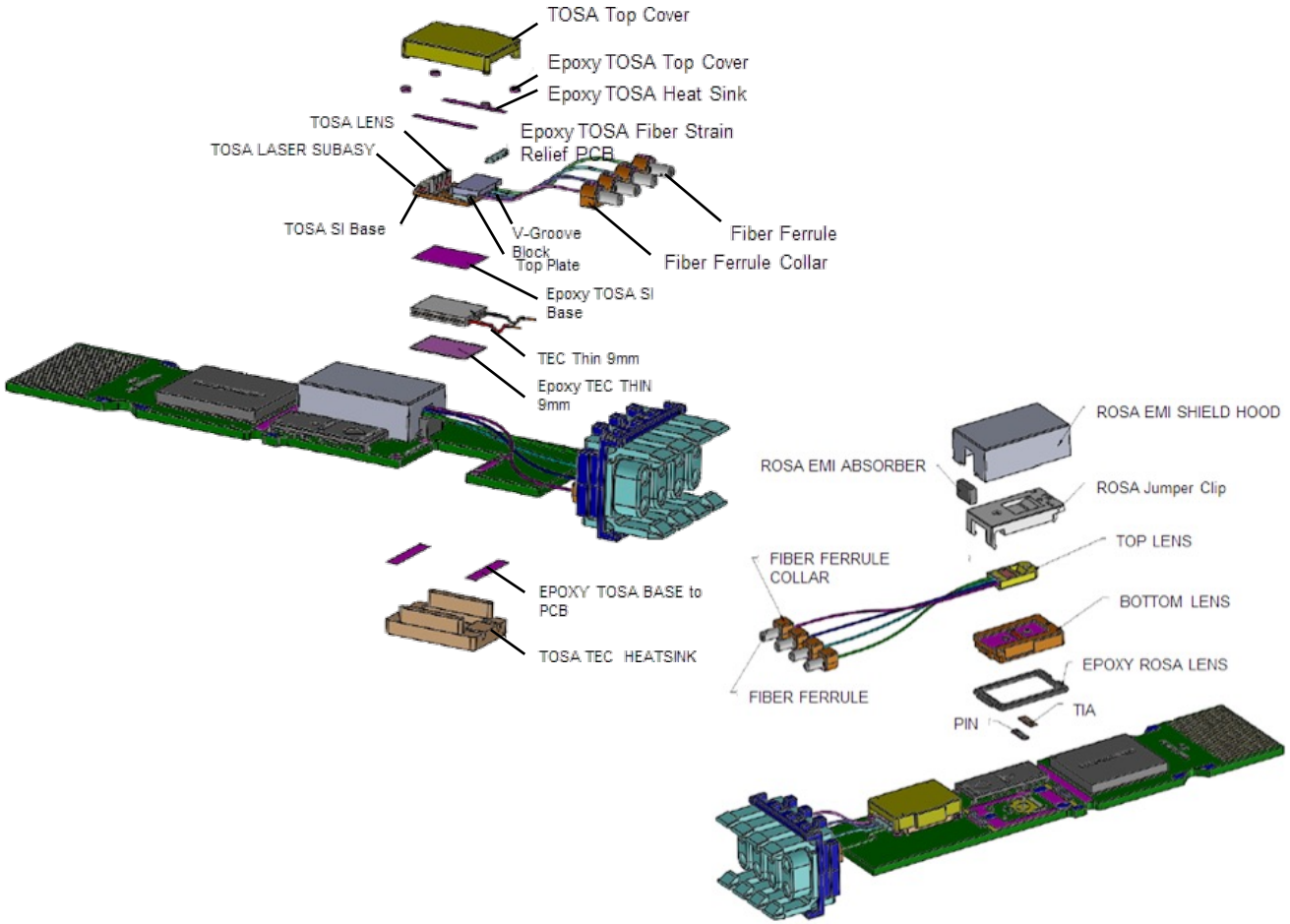
BROADCOM

Complexity of Each Box in the Datacenter

High-Performance Switch Silicon



Optical Transceivers



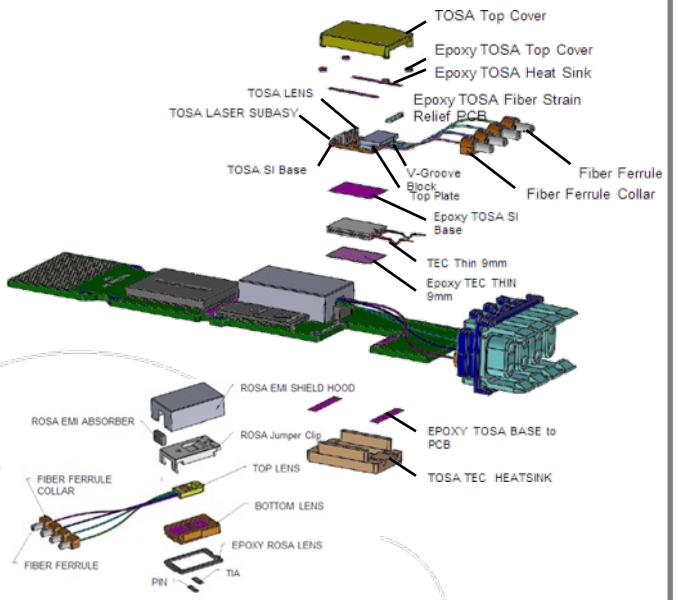
Standard Rack Appliance

Standard Optical Transceiver

BROADCOM

Evolution of Optics: Discrete III-V to Co-Packaged SiPh

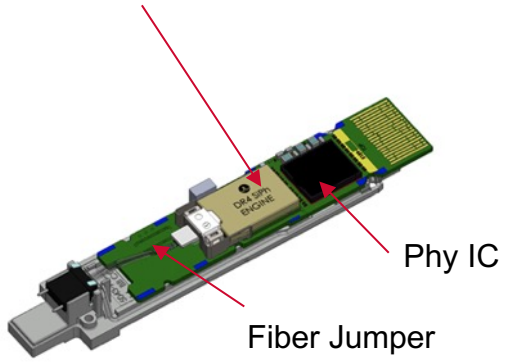
Conventional Module Design



Engineering and manufacturing limits to scale

Integrated Module Design Based w/ Silicon Photonics

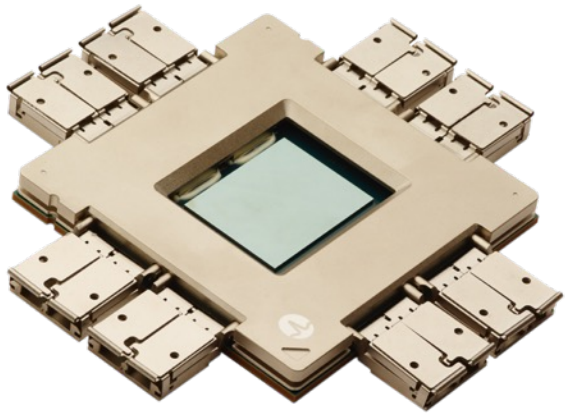
SiPh Chiplets in Package (SCIP)



30% fewer Piece Parts!

Module Integration = First step to improved scale

Co-Packaged Optics



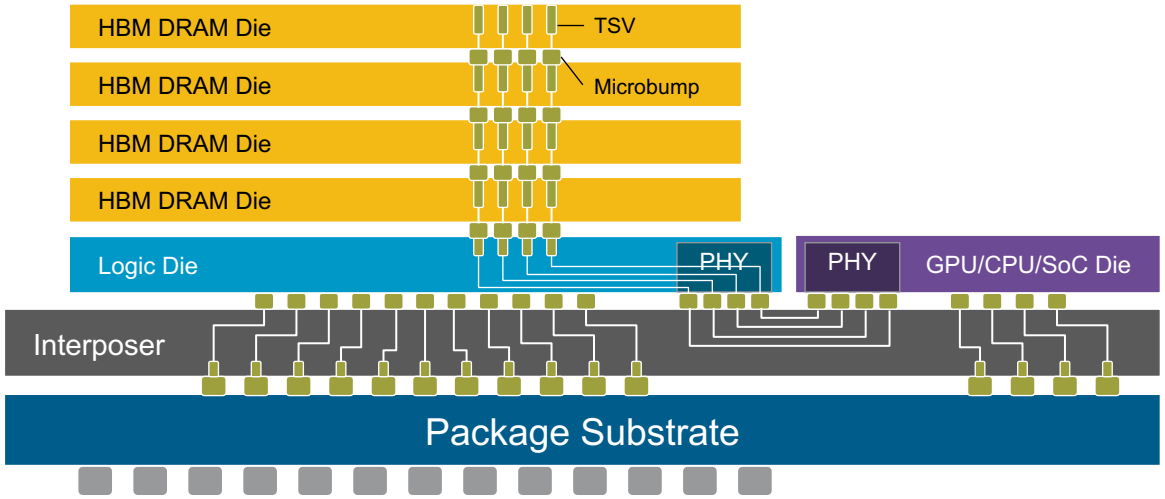
Highly Integrated Optical Engines (3.2T to 6.4T)

BROADCOM

True Co-Packaged Optics Using Heterogenous Integration

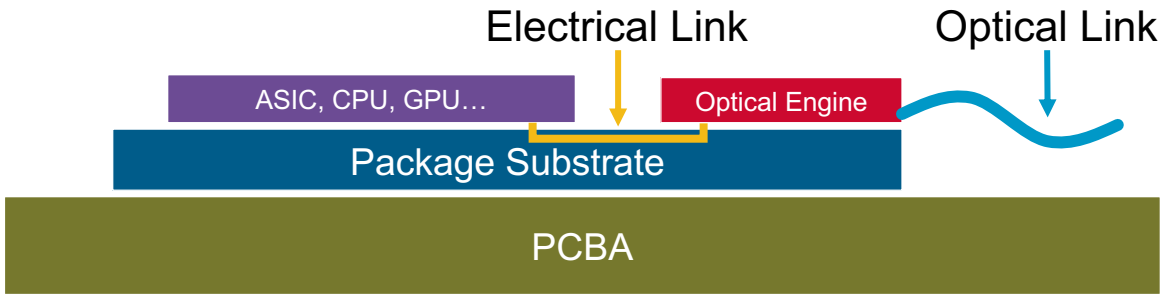
Co-Packaging

- Integration of **multiple dies** on a common package substrate
- High volume use cases today like HBM



Co-Packaged Optics

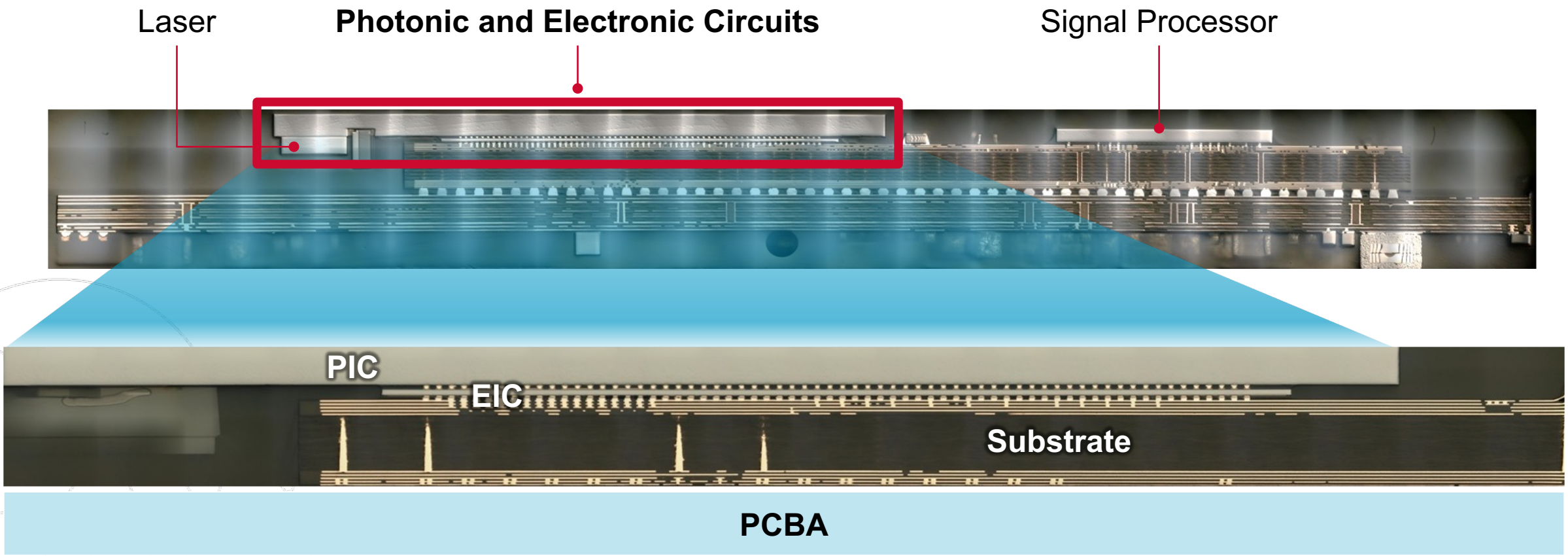
- Integration of **optical engines** on a common package substrate
- Objective: alleviate the "interconnect density bottleneck"



* Source: Image, AMD, https://www.amd.com/en/technologies/hbm
☆ Source: Yole Developpement, http://www.yole.fr/3D_25D_Stacking_Technologies_IntelEMIB.aspx#.YJyx7pNKh25

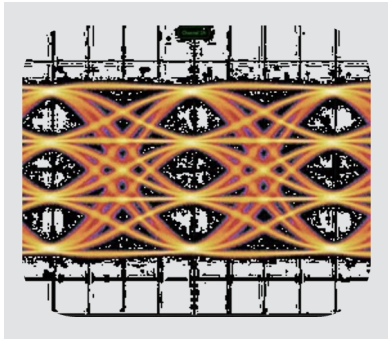
BROADCOM

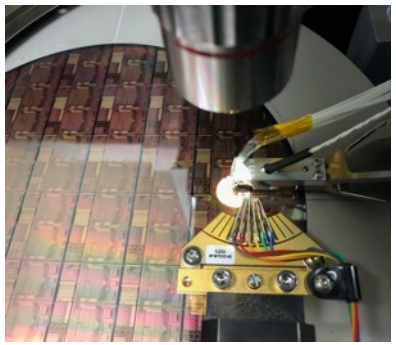
The Anatomy of a Fully Integrated Silicon Photonics Engine

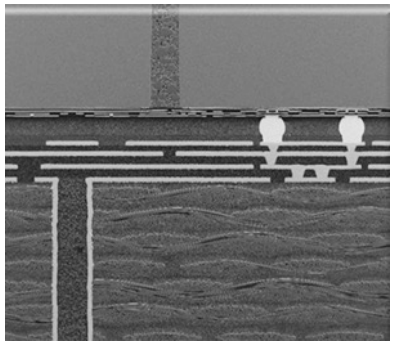


BROADCOM

Overcoming Copper Bottlenecks at Scale



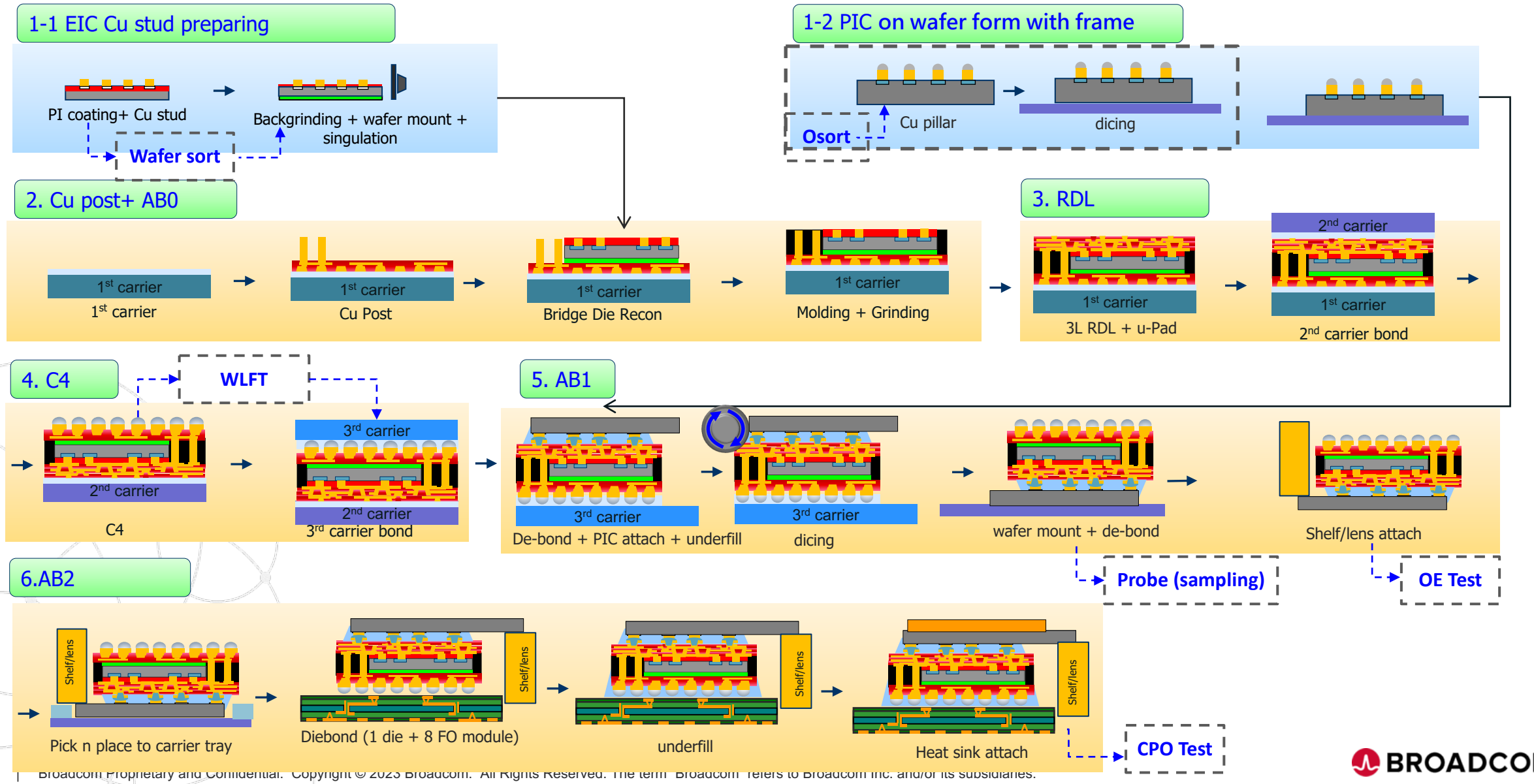




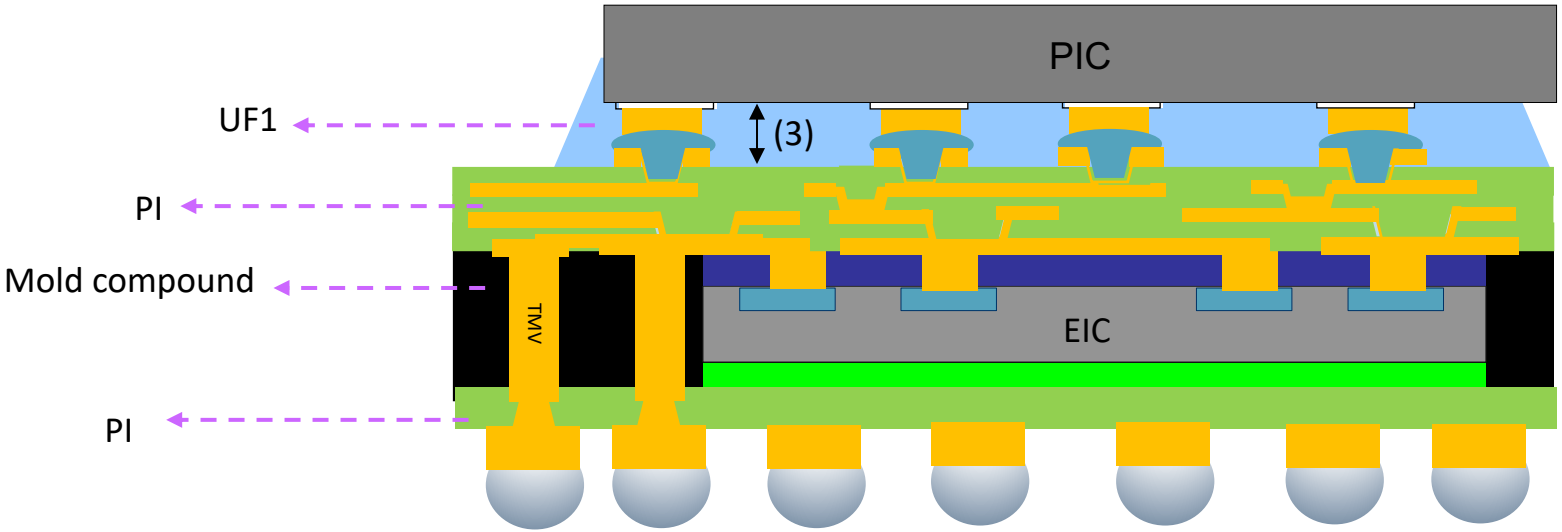
ASIC	Mixed Signal IC	Optical Devices & Fabs	Advanced Packaging & Test	Silicon Photonics
• Core switch, SerDes and DSP in leading node • Sustained generational differentiation	• Power and performance optimized in both SiGe and CMOS	• 50M lasers/year from internal fabs • High-volume optical manufacturing • High-power, multi-wavelength sources	• Wafer-level test • TSV • FoWLP	• High-density PIC design • Modulators and PDs in silicon • Low-loss SOI waveguides

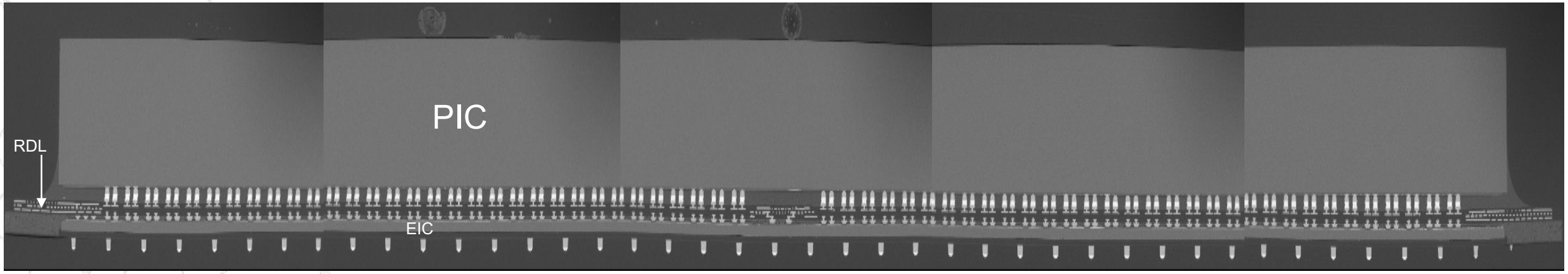
BROADCOM

Co-Packaged Optics Fan-Out Process Flow



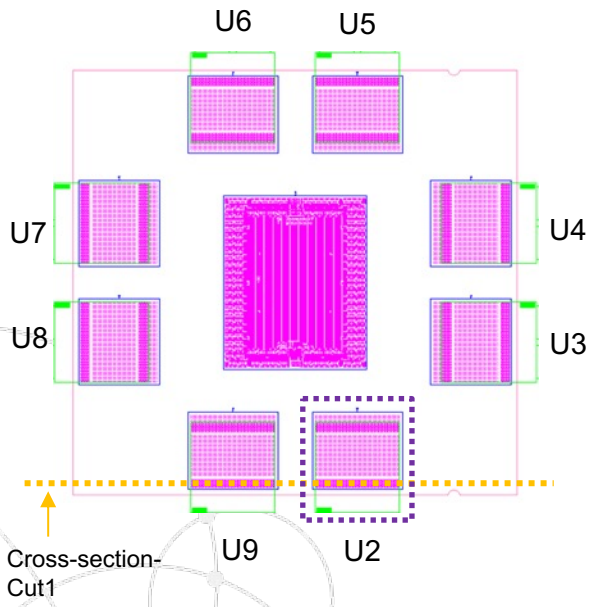
Optical Engine Structure



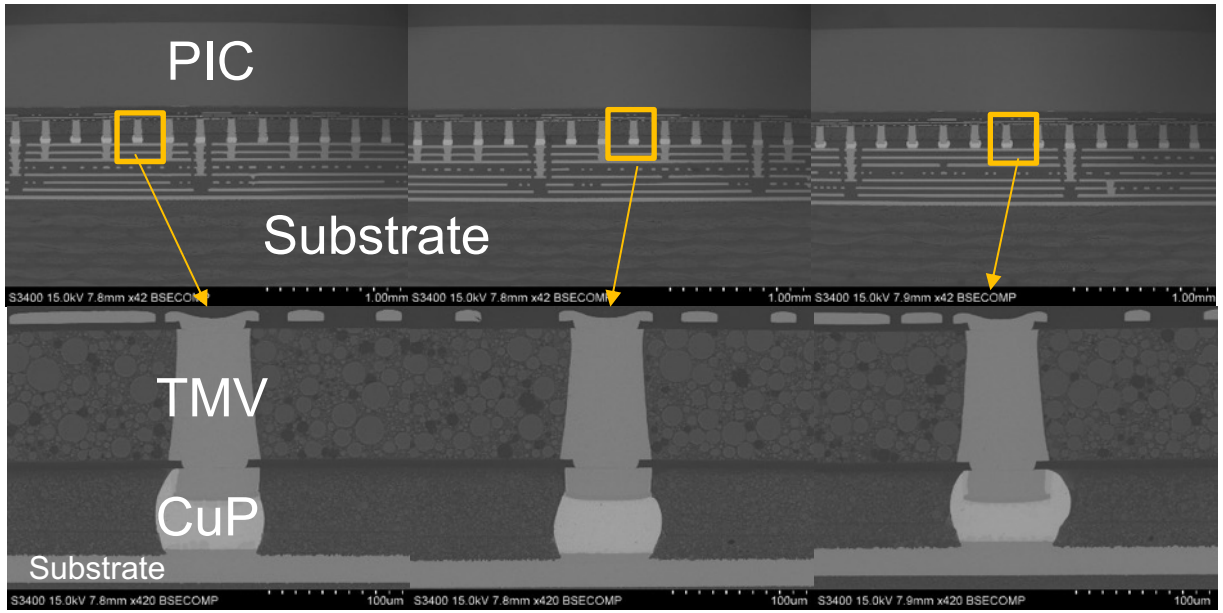


BROADCOM

Optical Engine Cross-section Images

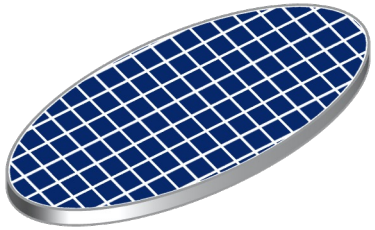


☐ **Cross-section on U2**

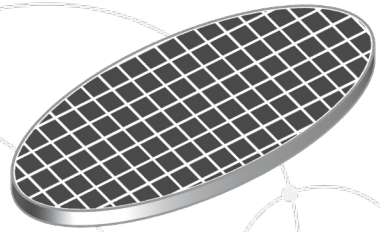


BROADCOM

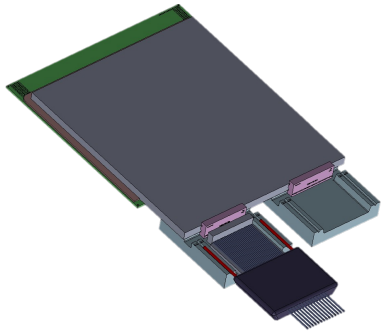
Test Point Insertion



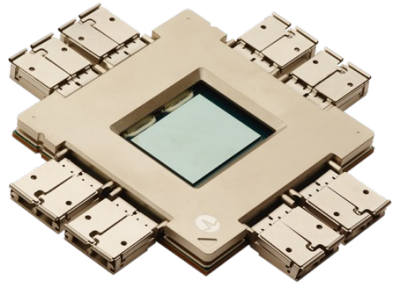
Photonic IC (PIC)
Optical Sort



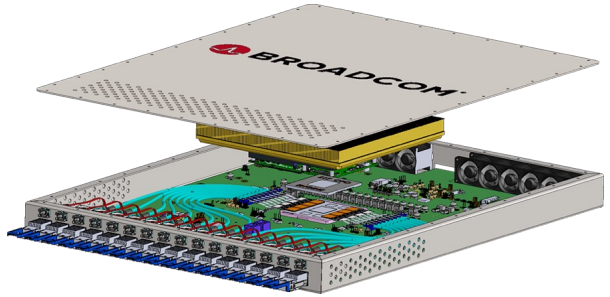
Electrical IC (EIC)
Wafer Sort



Optical Engine Test



CPO Test

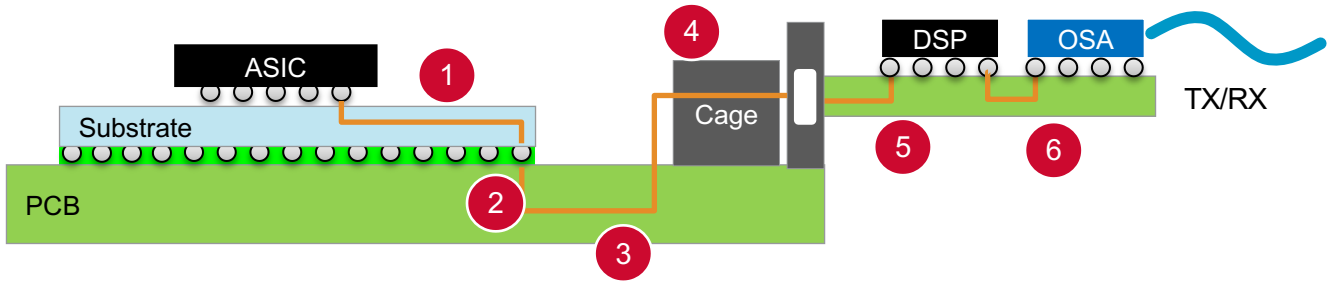


System Test

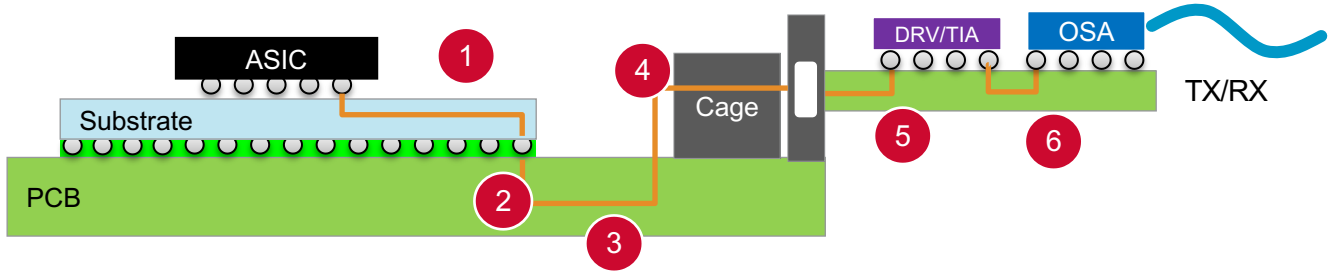
BROADCOM

CPO Insertion Loss Savings vs. Pluggables

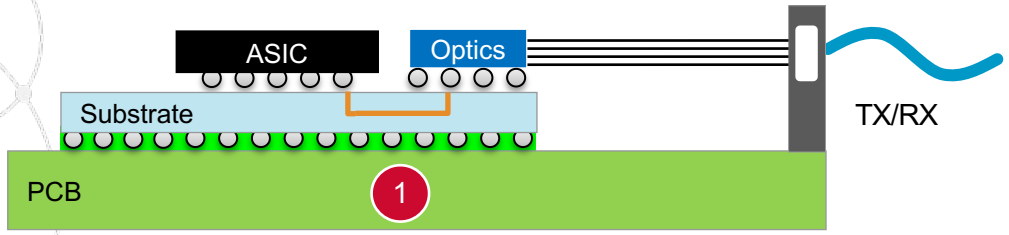
DSP Pluggable



LPO Pluggable



CPO



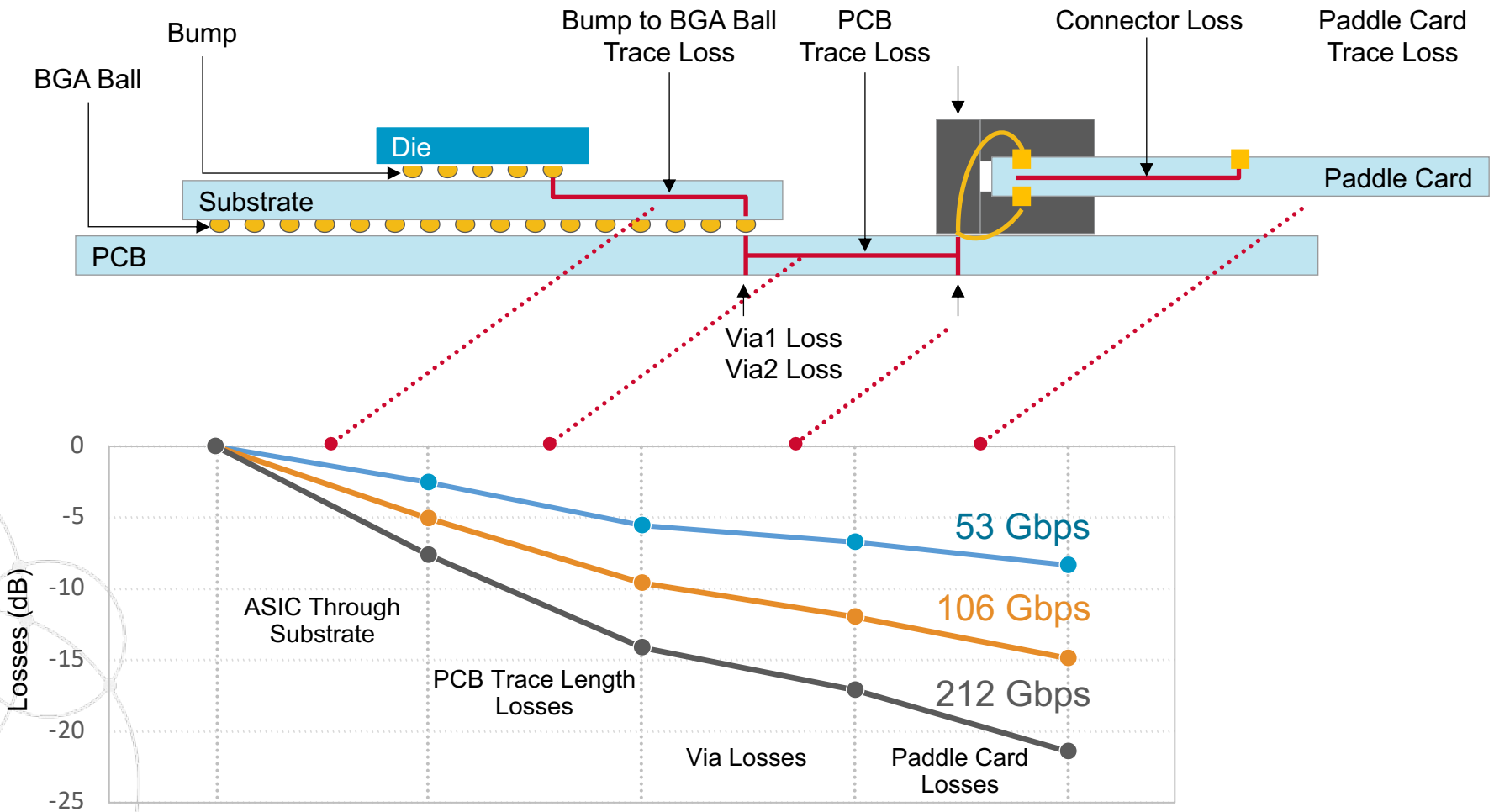
>30%
Cost Savings

>12dB
Insertion Loss savings

1. ASIC through substrate
2. Via Losses
3. PCB Trace Loss
4. Connector Losses
5. Module PCB Losses
6. OSA Interconnect loss

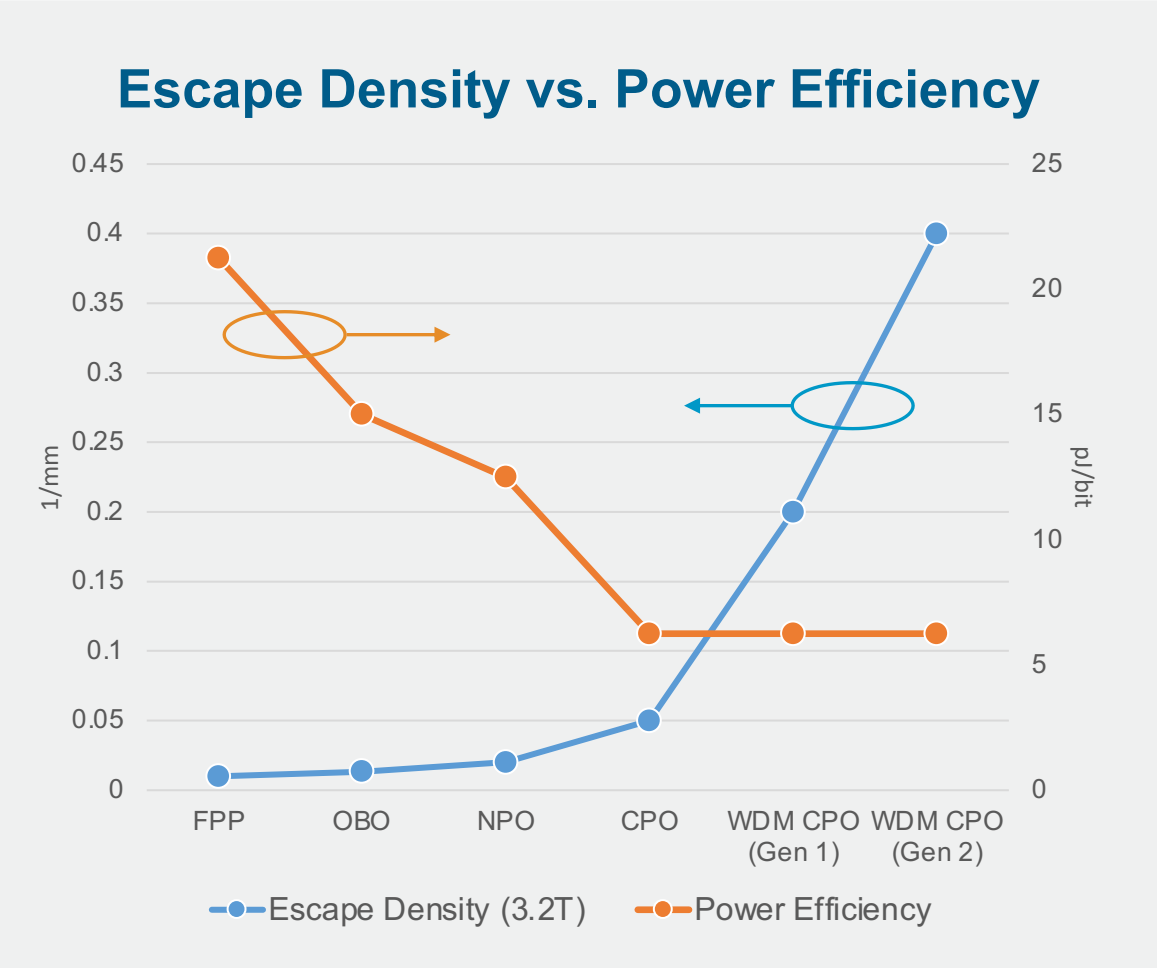
BROADCOM

Copper I/O Approaching a Limit



BROADCOM

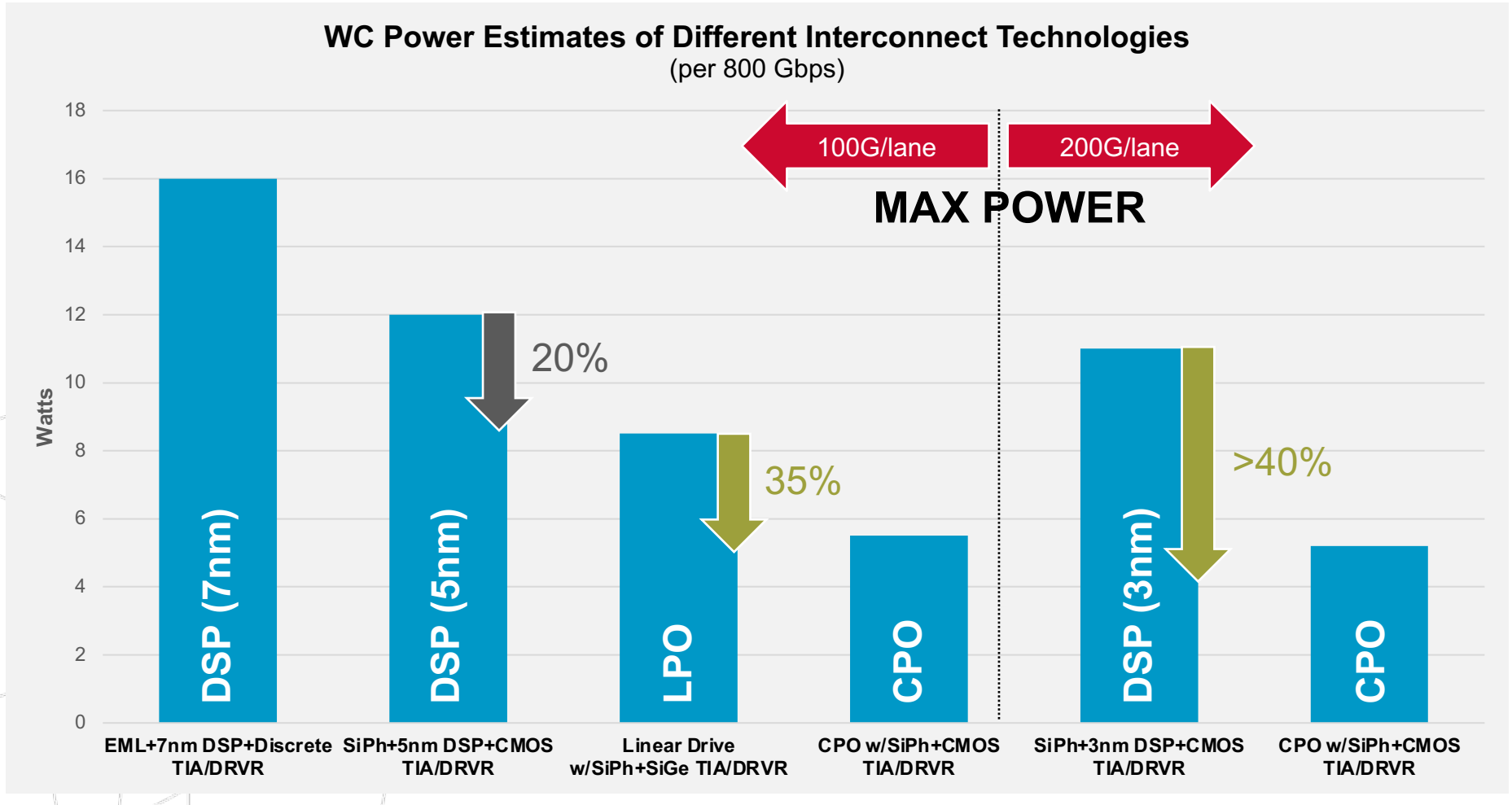
Optimizing Electrical to Optical Conversion Efficiency



Exponential Benefit in I/O Escape Density and Power Density with Immediate Conversion

BROADCOM

CPO Power Savings vs. Pluggables

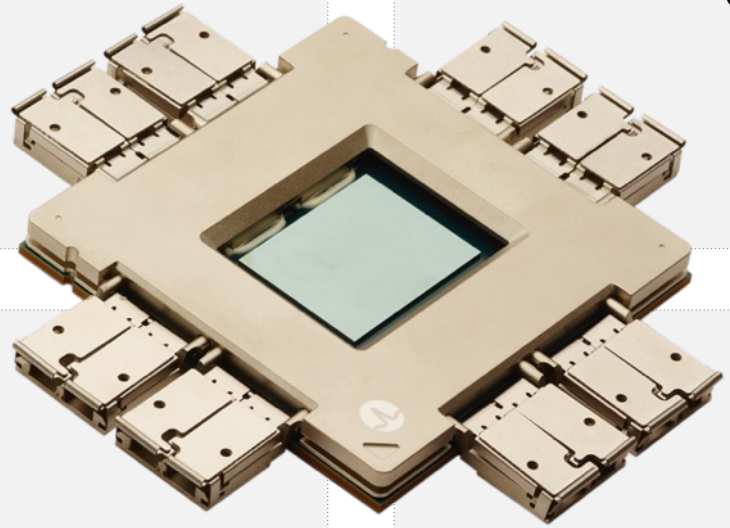


>40%

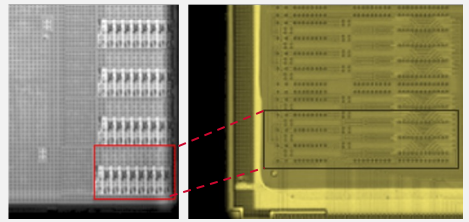
CPO Power Savings @ 200G/lane

TH5-Bailly CPO: Sampling

FOWLP OE Attach

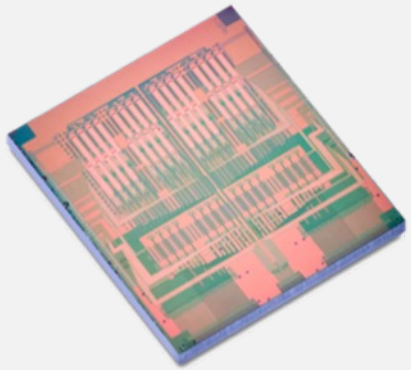


64 channel EIC with CMOS driver and TIA



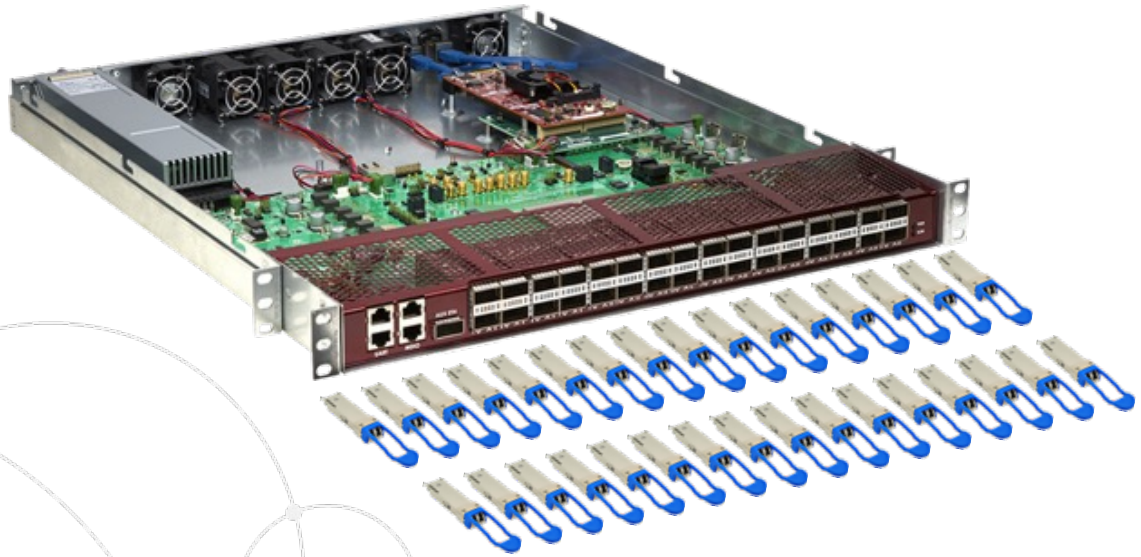
ODM System Integration

64 channel FR4 PIC with integrated mux/demux



BROADCOM

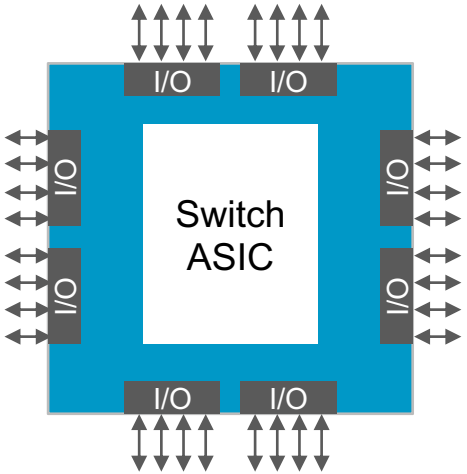
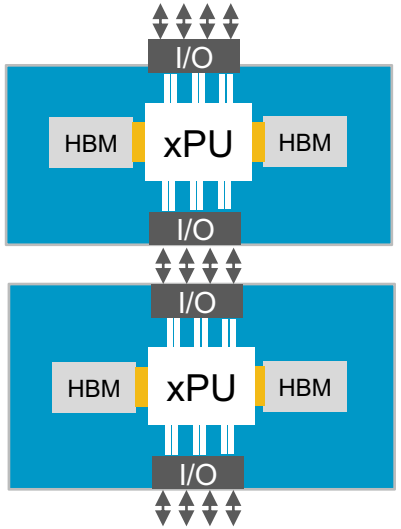
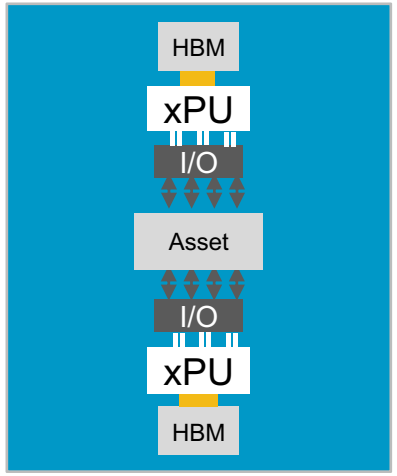
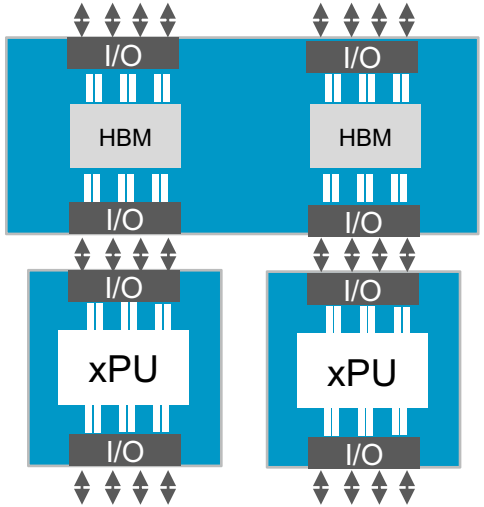
System Level Simplification Using Co-Packaged Optics



Signification reduction in board and system complexity

BROADCOM

Architectural Migrations Leveraging I/O Bandwidth

	High-Density Switch interconnect	GPU to GPU Interconnect	Resource Pooling	Memory Disaggregation
				
Bandwidth	25.6-51.2Tb/s	2.4-4.8Tb/s	8Tb/s	8Tb/s
Power Density	< 10 pJ/bit	< 5 pJ/bit	< 5 pJ/bit	< 5 pJ/bit
Latency	µs	µs	µs	100s ns

BROADCOM

BROADCOM®

Thank You


BROADCOM®
connecting everything®