



February 6-8, 2024
Santa Clara Convention Center
ChipletSummit.com



UCIe™: A Progress Report for 2024

Presented by:

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UCle consortium Form Factor & Compliance WG co-chair

Agenda

- UCIe recap
- UCIe progress over the past year
 - Spec rev1.1 summary
 - New areas/coverage
- Future Directions and Conclusions

Universal Chiplet Interconnect Express (UCIe):

An Open Standard for Chiplets

Guiding principles of UCIe



1. Open Ecosystem with Plug-and-play
2. Backward compatible evolution when appropriate to ensure investment protection
3. Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
4. Continuously innovate to meet the needs of evolving compute landscape

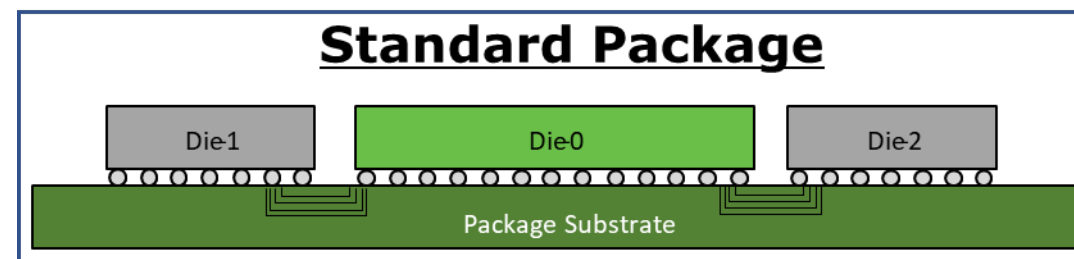
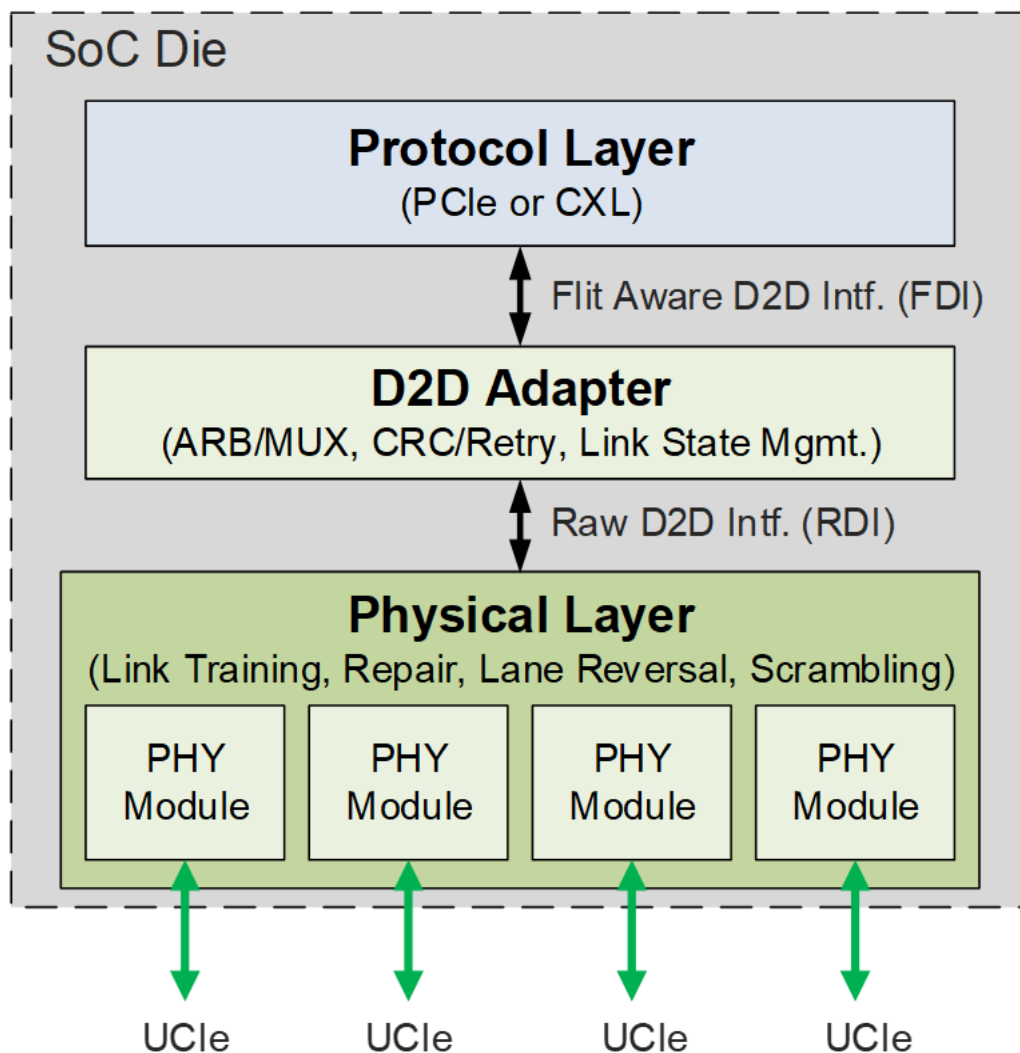
(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)

Key ingredient of an open chiplet ecosystem to enable multi-chiplet architectures from different vendors to create application-specific System-in-Package (SiP) designs



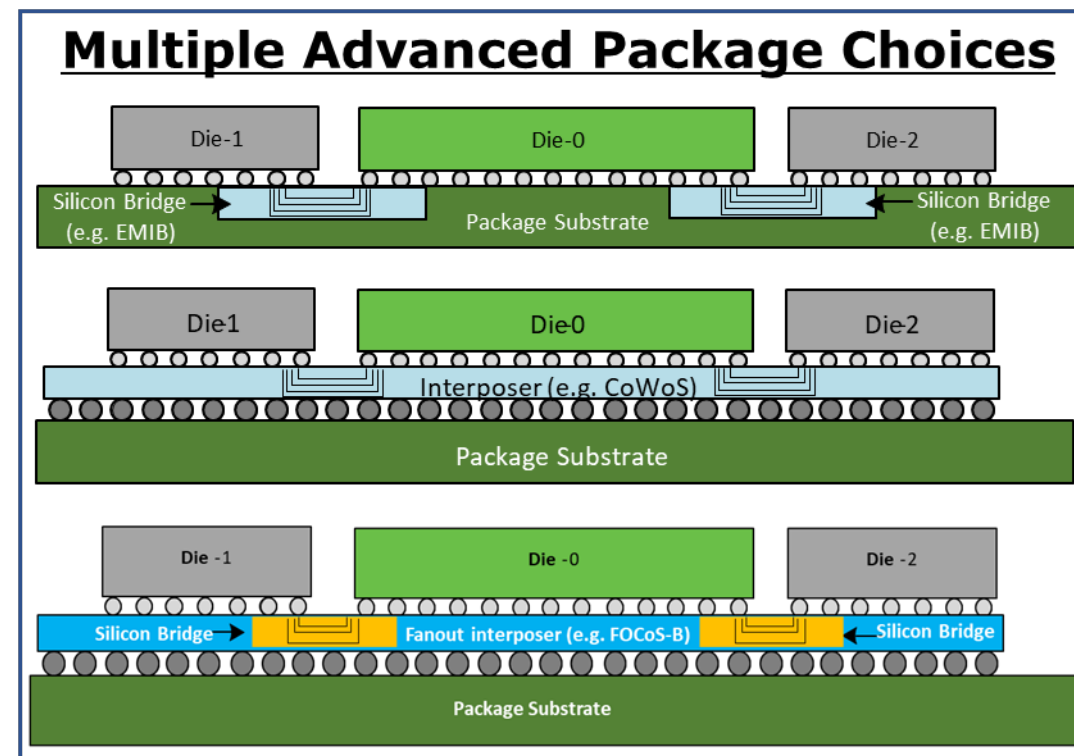
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UCle Technology



Bump Pitch:
100 um to 130 um

Channel Reach:
10 mm (short reach)
25 mm (long reach)



Bump Pitch:
25 um to 55 um

Channel Reach:
2 mm

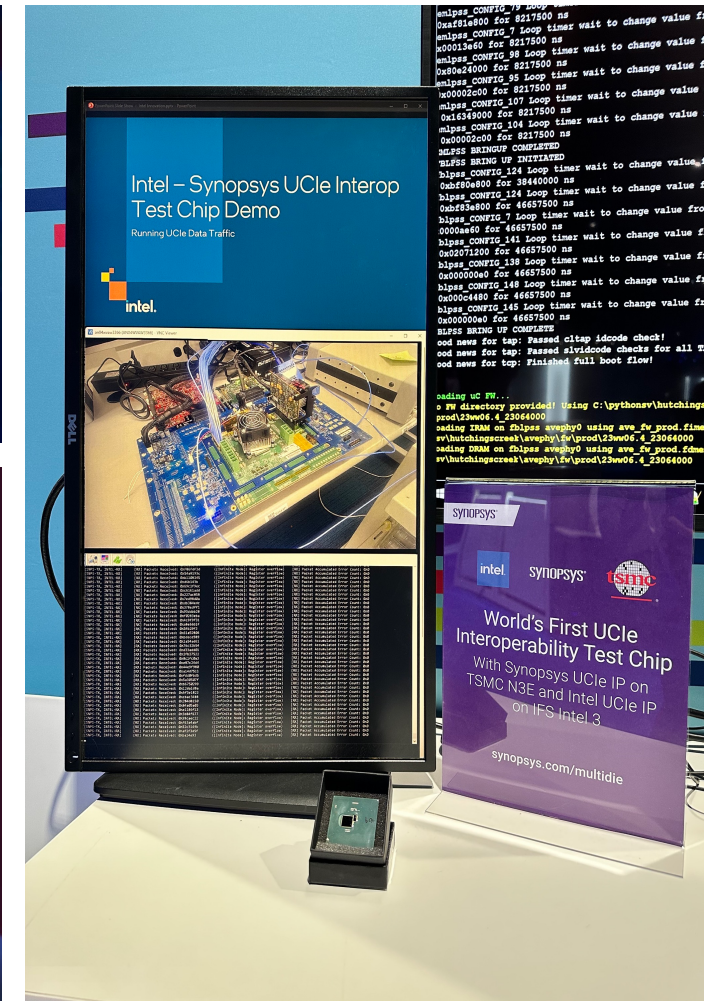
Supported Lane Speeds: 4 GT/s, 8 GT/s, 12 GT/s, 16 GT/s, 24 GT/S, 32 GT/s

First UCle Interop Demonstrated at Intel Innovation

Sept 19, 2023

Interop between independently designed Intel and TSMC chiplets

- Intel3 chiplet using Intel IP
- TSMC chiplet using Synopsys IP
- Packaged by Intel using EMIB



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Introducing UCIe 1.1

Enhancements for **Automotive Segment** Usage

New Usages: Streaming Protocols with Full Stack

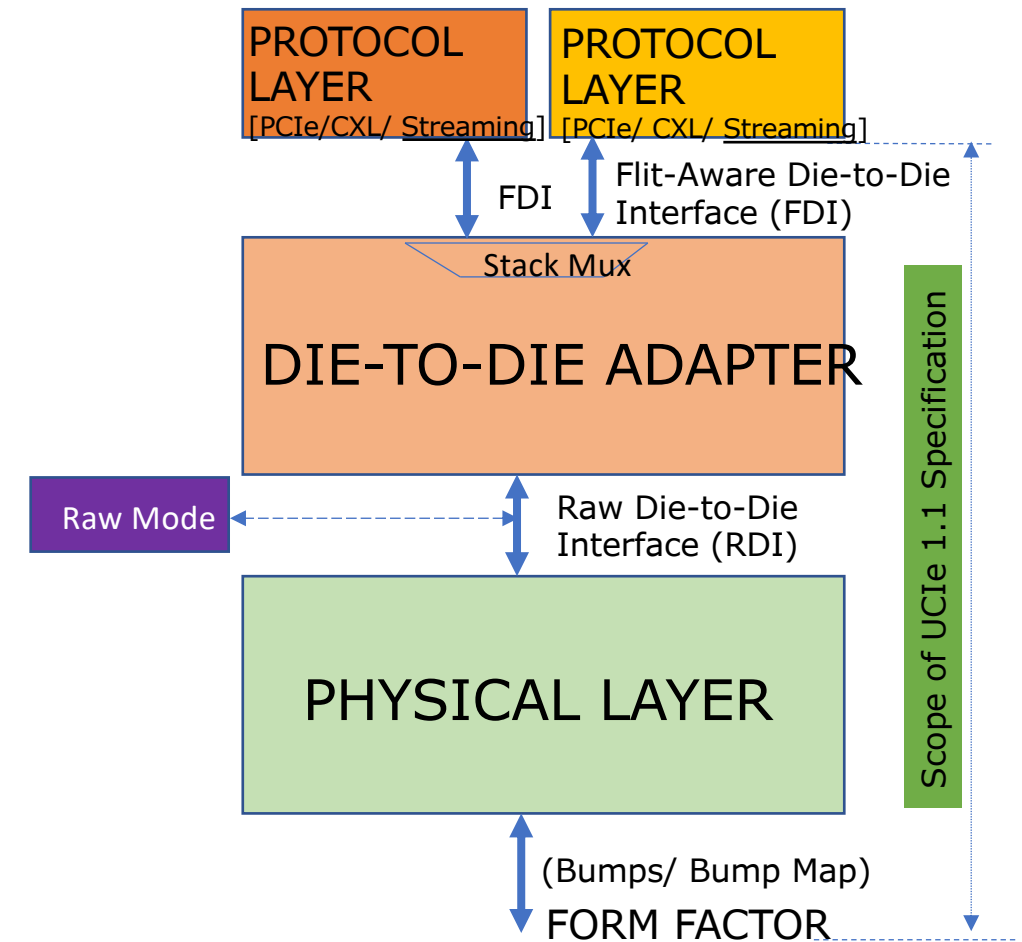
Cost Optimization for **Advanced Packaging**

Enhancements for **Compliance Testing**

UCIe 1.1 is Fully Backward Compatible with UCIe 1.0

UCIe 1.1: Streaming Protocols on Full Stack

- UCIe 1.0 supports Streaming Protocol (e.g., AXI, CHI, SMP coherency protocols, SFI, CPI) only in Raw Mode
- Two enhancements with UCIe 1.1 (raw mode still supported)
 1. Streaming Protocols can use the D2D adapter
 - Enables them to reuse the CRC, Retry etc.
 - Mechanism: map streaming to existing Flit Formats at FDI interface
 2. Streaming Protocols can multiplex with other protocols with on-demand interleaving
 - Enables co-existence of multiple protocols (e.g., streaming for processing, PCIe for discovery, DMA, TLB, error reporting, interrupt, etc.) for different use cases
 - Mechanism: Protocol muxing for Streaming protocol with existing Flit Formats at FDI interface



UCIe-A x64 Bump Maps

- New bumpout configurations for maintaining optimized BW/mm² across allowable bump pitch range
 - 8 and 16-column bump maps added to original 10-column in spec1.0
 - Suggested usage guideline:

uBump Pitch (um)	Max Data Rate by Spec (GT/s)	# of Columns within 388.8um shoreline
25-30	12	16
31-37	16	
38-44	24	
45-50	32	10
51-55	32	8

16Col
Recommended for
25-37um bump pitch

10Col
Recommended for
38-50um bump pitch

8Col
Recommended for
51-55um bump pitch



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UCIe-A x32 Bump Maps

- Newly added x32 bump maps for further Si area & package tech flexibility
 - 8, 10 and 16-columns
 - Suggested usage guideline:

uBump Pitch (um)	Max Data Rate by Spec (GT/s)	# of Columns within 388.8um shoreline
25-30	12	16
31-37	16	
38-44	24	10
45-50	32	
51-55	32	8

Column0	Column1	Column2	Column3	Column4	Column5	Column6	Column7	Column8	Column9	Column10	Column11	Column12	Column13	Column14	Column15	Column16	Column17
col0a	col0b	col0c	col0d	col0e	col0f	col0g	col0h	col0i	col0j	col0k	col0l	col0m	col0n	col0o	col0p	col0q	col0r
col1a	col1b	col1c	col1d	col1e	col1f	col1g	col1h	col1i	col1j	col1k	col1l	col1m	col1n	col1o	col1p	col1q	col1r
col2a	col2b	col2c	col2d	col2e	col2f	col2g	col2h	col2i	col2j	col2k	col2l	col2m	col2n	col2o	col2p	col2q	col2r
col3a	col3b	col3c	col3d	col3e	col3f	col3g	col3h	col3i	col3j	col3k	col3l	col3m	col3n	col3o	col3p	col3q	col3r
col4a	col4b	col4c	col4d	col4e	col4f	col4g	col4h	col4i	col4j	col4k	col4l	col4m	col4n	col4o	col4p	col4q	col4r
col5a	col5b	col5c	col5d	col5e	col5f	col5g	col5h	col5i	col5j	col5k	col5l	col5m	col5n	col5o	col5p	col5q	col5r
col6a	col6b	col6c	col6d	col6e	col6f	col6g	col6h	col6i	col6j	col6k	col6l	col6m	col6n	col6o	col6p	col6q	col6r
col7a	col7b	col7c	col7d	col7e	col7f	col7g	col7h	col7i	col7j	col7k	col7l	col7m	col7n	col7o	col7p	col7q	col7r
col8a	col8b	col8c	col8d	col8e	col8f	col8g	col8h	col8i	col8j	col8k	col8l	col8m	col8n	col8o	col8p	col8q	col8r
col9a	col9b	col9c	col9d	col9e	col9f	col9g	col9h	col9i	col9j	col9k	col9l	col9m	col9n	col9o	col9p	col9q	col9r
col10a	col10b	col10c	col10d	col10e	col10f	col10g	col10h	col10i	col10j	col10k	col10l	col10m	col10n	col10o	col10p	col10q	col10r
col11a	col11b	col11c	col11d	col11e	col11f	col11g	col11h	col11i	col11j	col11k	col11l	col11m	col11n	col11o	col11p	col11q	col11r
col12a	col12b	col12c	col12d	col12e	col12f	col12g	col12h	col12i	col12j	col12k	col12l	col12m	col12n	col12o	col12p	col12q	col12r
col13a	col13b	col13c	col13d	col13e	col13f	col13g	col13h	col13i	col13j	col13k	col13l	col13m	col13n	col13o	col13p	col13q	col13r
col14a	col14b	col14c	col14d	col14e	col14f	col14g	col14h	col14i	col14j	col14k	col14l	col14m	col14n	col14o	col14p	col14q	col14r
col15a	col15b	col15c	col15d	col15e	col15f	col15g	col15h	col15i	col15j	col15k	col15l	col15m	col15n	col15o	col15p	col15q	col15r
col16a	col16b	col16c	col16d	col16e	col16f	col16g	col16h	col16i	col16j	col16k	col16l	col16m	col16n	col16o	col16p	col16q	col16r
col17a	col17b	col17c	col17d	col17e	col17f	col17g	col17h	col17i	col17j	col17k	col17l	col17m	col17n	col17o	col17p	col17q	col17r
col18a	col18b	col18c	col18d	col18e	col18f	col18g	col18h	col18i	col18j	col18k	col18l	col18m	col18n	col18o	col18p	col18q	col18r
col19a	col19b	col19c	col19d	col19e	col19f	col19g	col19h	col19i	col19j	col19k	col19l	col19m	col19n	col19o	col19p	col19q	col19r
col20a	col20b	col20c	col20d	col20e	col20f	col20g	col20h	col20i	col20j	col20k	col20l	col20m	col20n	col20o	col20p	col20q	col20r
col21a	col21b	col21c	col21d	col21e	col21f	col21g	col21h	col21i	col21j	col21k	col21l	col21m	col21n	col21o	col21p	col21q	col21r
col22a	col22b	col22c	col22d	col22e	col22f	col22g	col22h	col22i	col22j	col22k	col22l	col22m	col22n	col22o	col22p	col22q	col22r
col23a	col23b	col23c	col23d	col23e	col23f	col23g	col23h	col23i	col23j	col23k	col23l	col23m	col23n	col23o	col23p	col23q	col23r
col24a	col24b	col24c	col24d	col24e	col24f	col24g	col24h	col24i	col2								

16Col

Recommended for
25-37um bump pitch

[illegible]

10Col

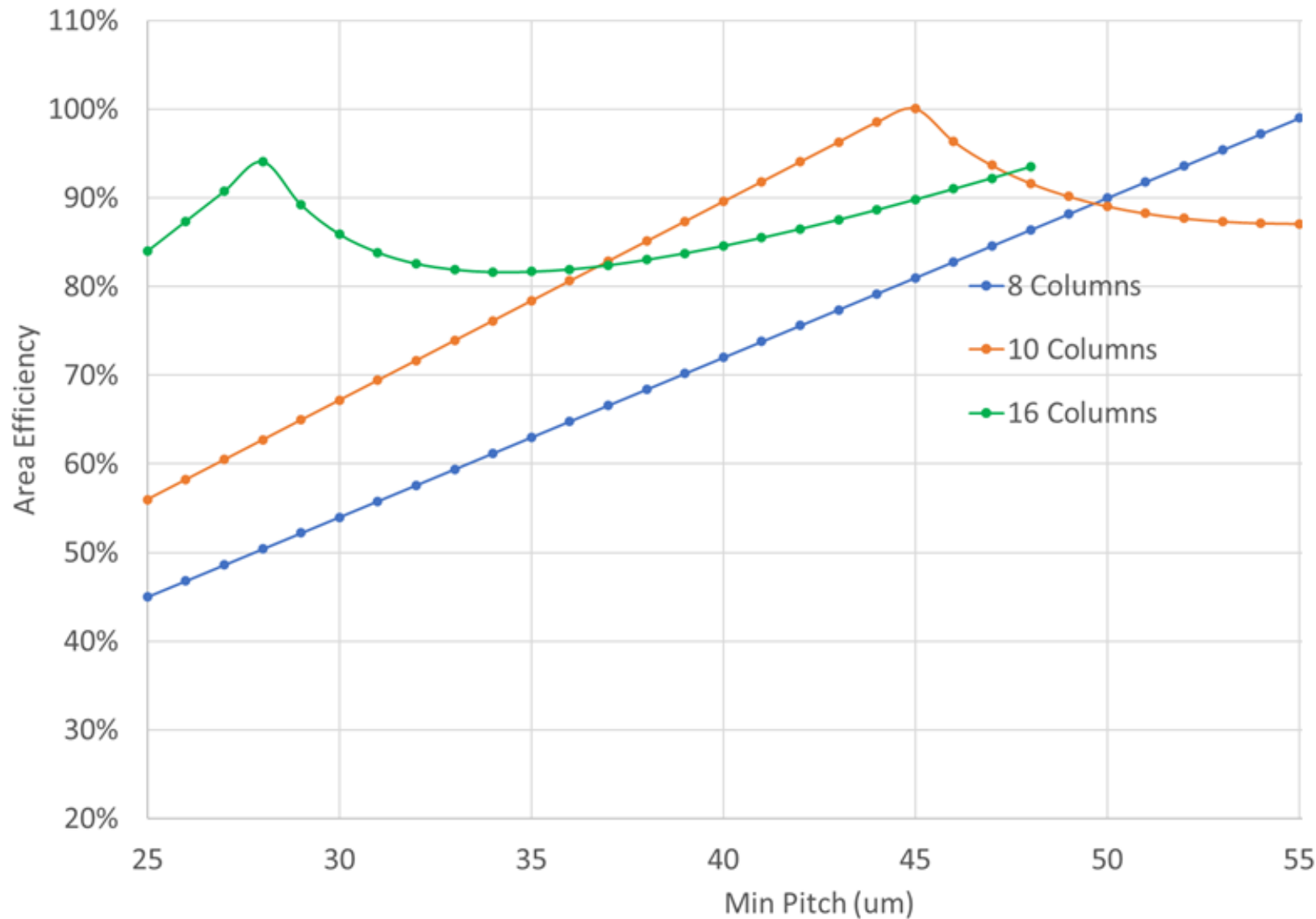
Recommended for
38-50um bump pitch

Column0	Column1	Column2	Column3	Column4	Column5	Column6	Column7
	vss		vss		vss		vss
vss		vss		vss		vss	
	vccio		vccio		vccio		vccio
rxcsbRD		rxcsb		rxdatasb		rxdatasbRD	
	txdatasbRD		txdatasb		txcsb		txcsbRD
txdata5		txdata23		rxdata30		rxdata13	
	txdata22		txckp		rxdata14		rxdataRD0
txdata6		vss		vss		rxdata12	
	txdata21		txckn		rxdata15		vss
txdata7		txdata24		rxdata31		rxdata11	
	txdata20		vss		vss		rxdata0
vss		txdata25		rxdataRD1		rxdata10	
	txdata19		txckRD		rxdata16		rxdata1
txdata4		vss		vss		rxdata9	
	txdata18		txtrk		rxdata29		vss
txdata3		txdata26		rxvldRD		rxdata8	
	txdata17		vss		rxdata28		rxdata2
vss		txdata27		rxvld		vss	
	txdata8		txvld		rxdata27		rxdata3
vccio		vccio		vccfwldio		vccfwldio	
	txdata9		txvldRD		rxdata26		vss
txdata2		txdata28		rxtrk		rxdata17	
	txdata10		vss		vss		rxdata4
vss		txdata29		rxckRD		rxdata18	
	txdata11		txdataRD1		rxdata25		rxdata7
txdata1		txdata16		vss		rxdata19	
	vss		txdata31		rxdata24		vss
txdata0		txdata15		rxckn		rxdata20	
	txdata12		vss		vss		rxdata6
vss		txdata14		rxckp		rxdata21	
	txdata13		txdata30		rxdata23		rxdata5
txdataRD0		vss		vss		rxdata22	
	vccio		vccio		vccfwldio		vccfwldio
vccio		vccio		vccfwldio		vccfwldio	

8Col

Recommended for
51-55um bump pitch

UCIe-A area/column type efficiency

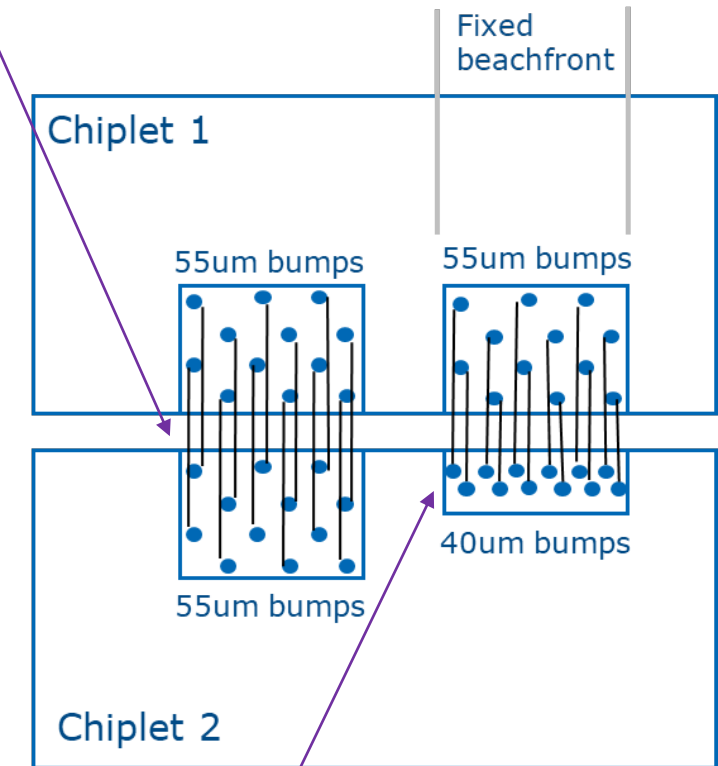


- Points of overlap are the optimal cross-over points between recommended 8/10/16-column bump maps
- At the lower bump pitch range, >80% area efficiency is acceptable given overall magnitude of PHY depth is lower
- As bump pitch increases, >90% area efficiency is desired due to the much bigger PHY depth (um)
 - Example: 10% of 1000um is greater than 20% of 400um

UCIe-A Interoperability

- Advanced package planning of key parameters up front for interop across IDMs/OSATs:
 - PHY beachfront must be defined to balance BW/mm capability and mechanical compatibility
 - Inter-generational compatibility across bump pitch range
 - Fixed beachfront (388.8um) per PHY module &
 - Signal ordering rules
 - Comprehensive PHY placement & rotation/mirroring rules

CoWos or EMIB or
similar tight-pitch tech



- With the reduction of bump pitch, the number of rows decrease while the number of columns increase
- Interop is enabled by a fixed beachfront & following signal ordering rules

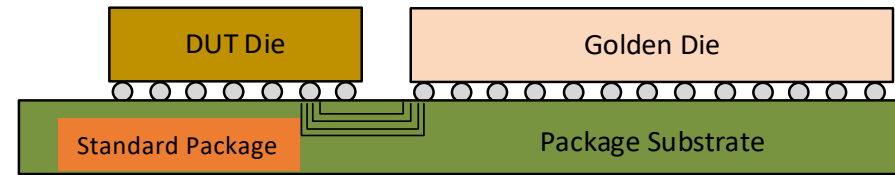
Compliance & Interop

- Spec 1.1 enhanced with compliance setup & tests
- Standard package & advance package
- Inter-connectivity setup & testing – active in FFCWG now
- Two options for compliance setup
 1. Reference package with Golden Die and DUT
 2. Custom package with Golden Die and DUT
- Compliance types
 1. Up to RDI: Electrical & Channel only
 2. Up to FDI: Electrical, Channel & protocol/streaming

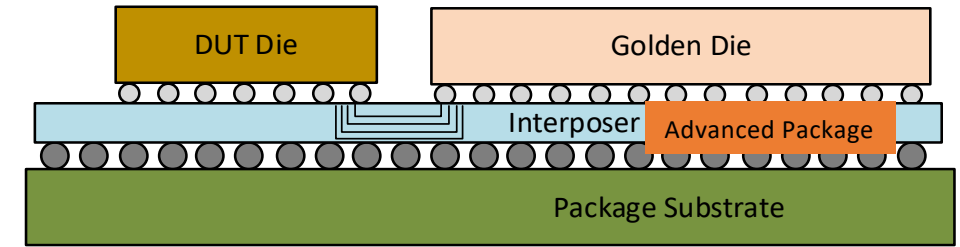
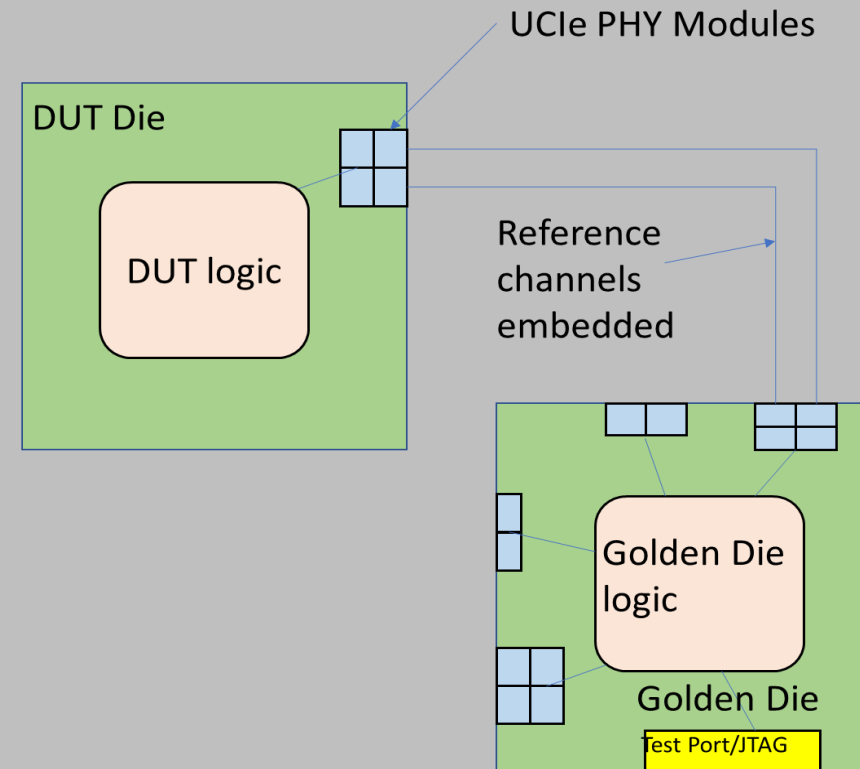
UCIe Compliance: Setup

Ingredients

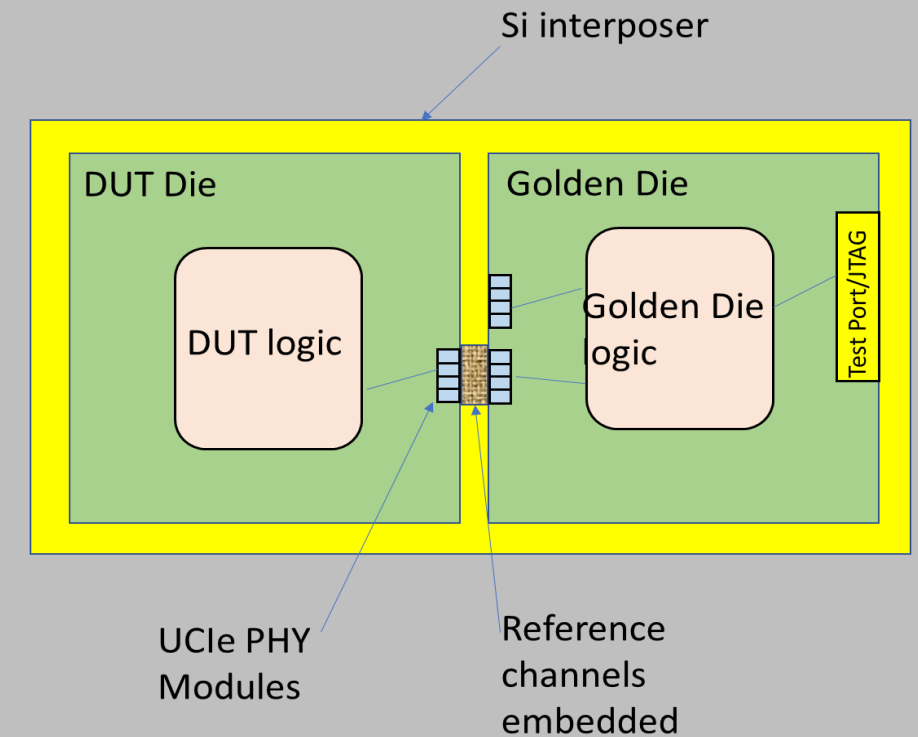
- Known good package with Reference Channels
- Golden Die
- DUT



Reference Known Good Package
(Standard Laminate)



Reference Known Good Package
(Si Interposer, Si Bridge, FO/RDL, etc..)



UCIe 1.1: Automotive Enhancements

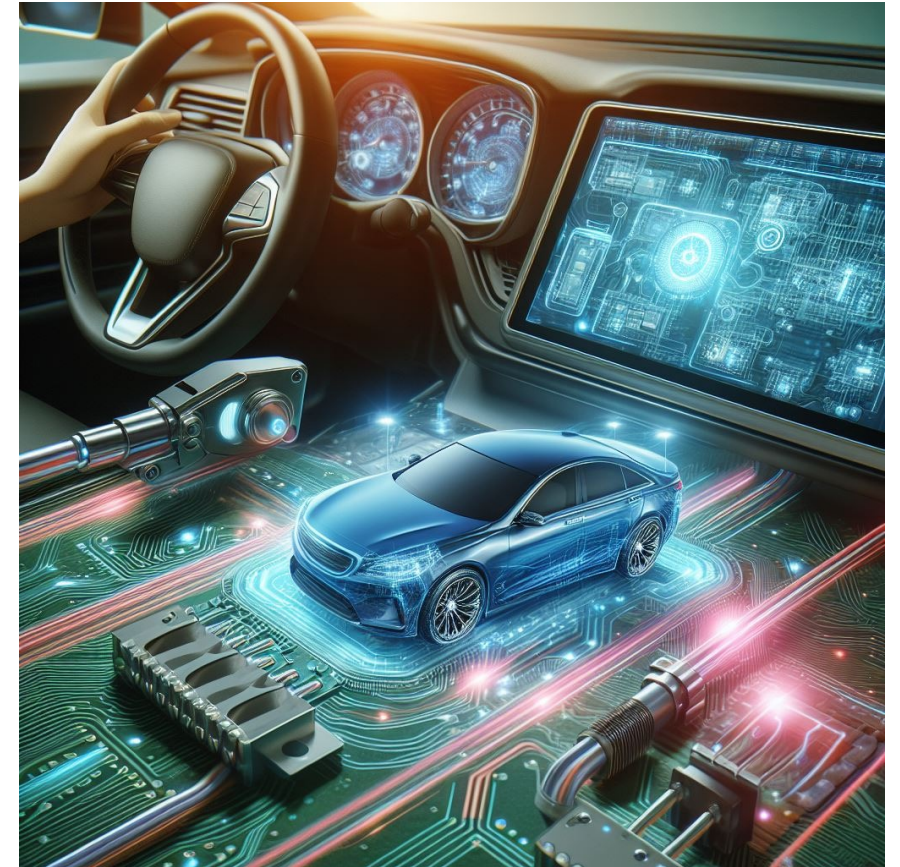
Automotive compute workloads are growing into what used to be supercomputer level.

Automotive SoCs challenges:

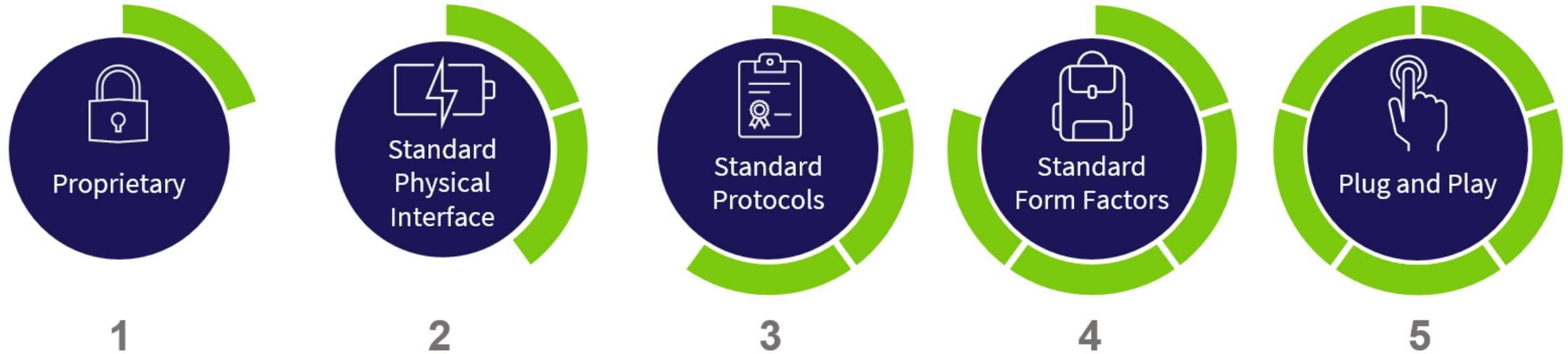
- Cost
- Flexibility
- Time-to-Market

Industry is looking to chiplets. Safety Integrity is critical. System reliability requirement translates into additional I/O features.

- Preventive Monitoring
- Run-time Testability of Link Health
- Field Repairability



Stages of Chiplet Evolution



UCIe Workgroups and Key Initiatives

Workgroups

- Electrical
- Form Factor & Compliance
- Manageability & Security
- Marketing
- Protocol
- Systems and Software
- Automotive

Key Initiatives

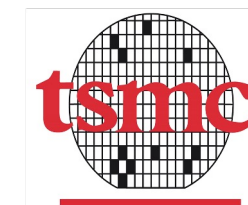
- UCIe 3D
- Interoperability & Compliance
- Manageability & Security
 - Management Transport
 - Memory Access Protocol
 - MCTP
 - Test and Debug
 - Power Management

130+ Member Companies and growing!

Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive The open chiptlet ecosystem.

JOIN US!



Thank You

www.UCIexpress.org



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