UCIe™
Universal Chiplet Interconnect Express

UCIe™: A Progress Report for 2024

Presented by:

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UCIe consortium Form Factor & Compliance WG co-chair

Agenda

- UCIe recap
- UCIe progress over the past year
  - Spec rev1.1 summary
  - New areas/coverage
- Future Directions and Conclusions

Universal Chiplet Interconnect Express (UCIe):

An Open Standard for Chiplets

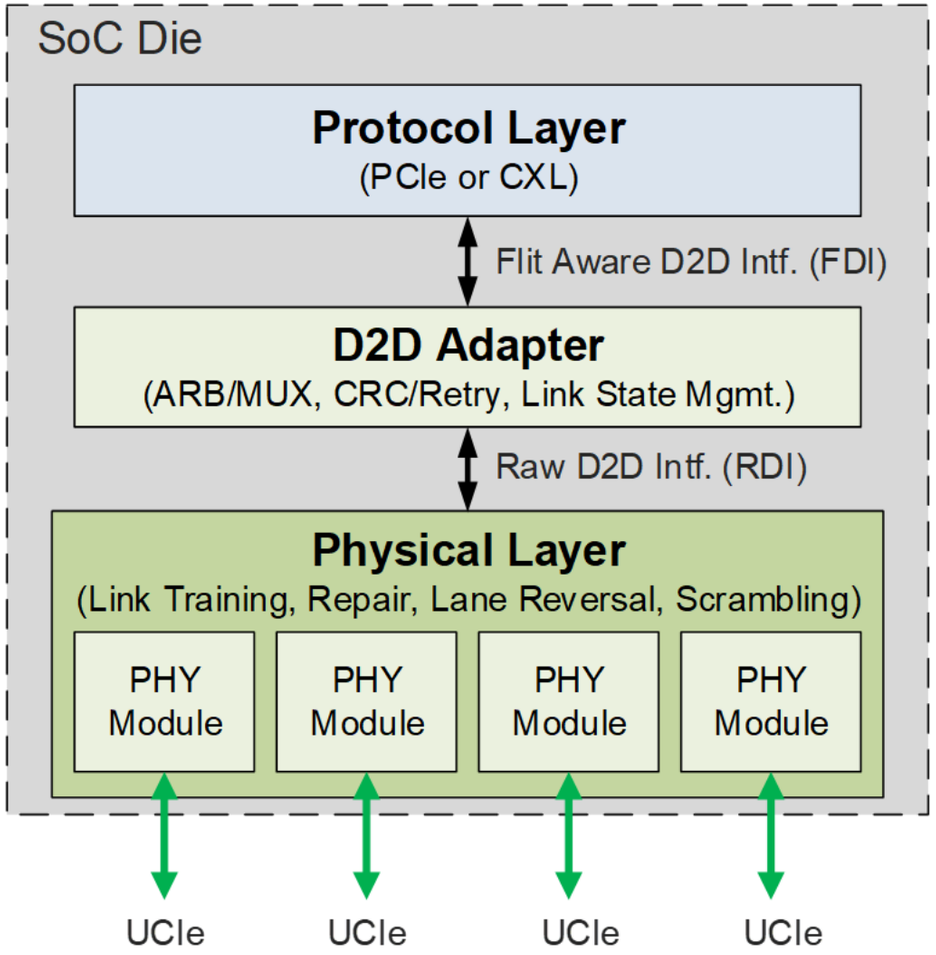
Guiding principles of UCIe

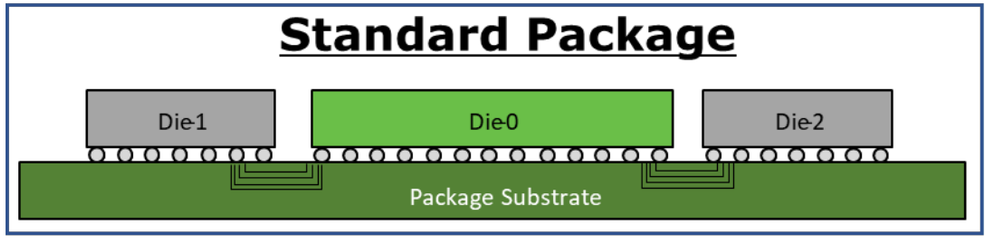
1. Open Ecosystem with Plug-and-play
2. Backward compatible evolution when appropriate to ensure investment protection
3. Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
4. Continuously innovate to meet the needs of evolving compute landscape

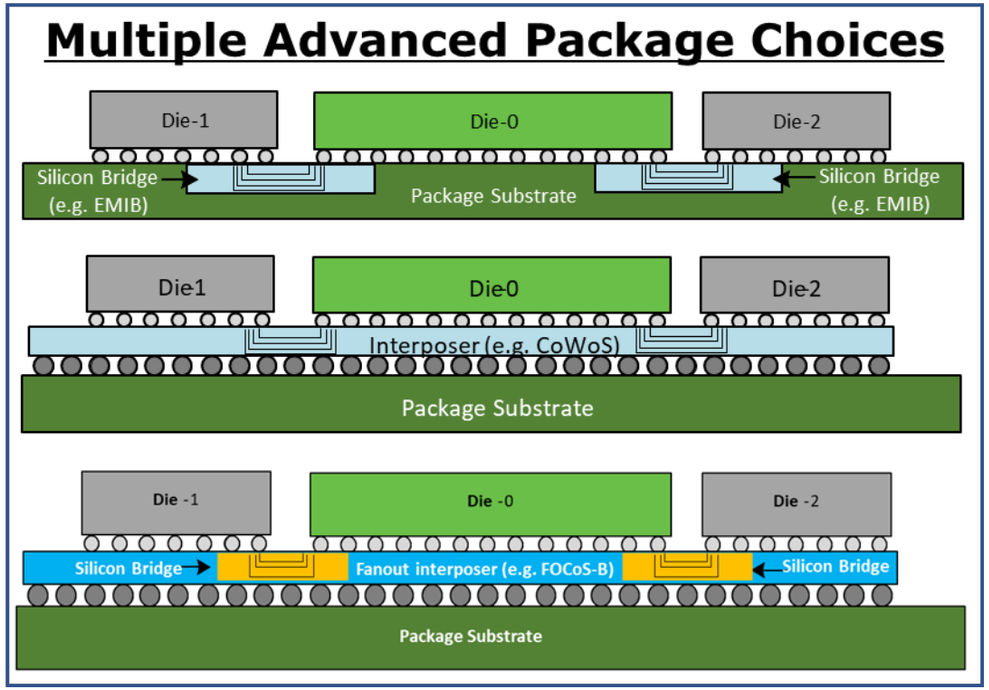
(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)

Key ingredient of an open chiplet ecosystem to enable multi-chiplet architectures from different vendors to create application-specific System-in-Package (SiP) designs

UCIe Technology







Bump Pitch:
100 um to 130 um

Channel Reach:
10 mm (short reach)
25 mm (long reach)

Bump Pitch:
25 um to 55 um

Channel Reach:
2 mm

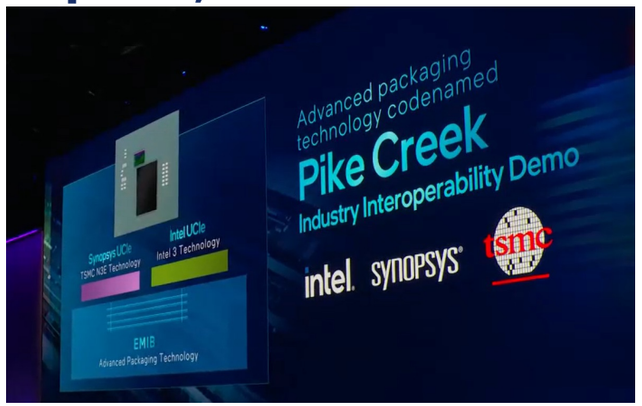
Supported Lane Speeds: 4 GT/s, 8 GT/s, 12 GT/s, 16 GT/s, 24 GT/S, 32 GT/s

First UCIe Interop Demonstrated at Intel Innovation

Sept 19, 2023

<u>Interop between independently designed Intel and TSMC chiplets</u>

- Intel3 chiplet using Intel IP
- TSMC chiplet using Synopsys IP
- Packaged by Intel using EMIB



UCIe™
Universal Chiplet Interconnect Express

Introducing UCIe 1.1

Enhancements for **Automotive Segment** Usage

New Usages: Streaming Protocols with Full Stack

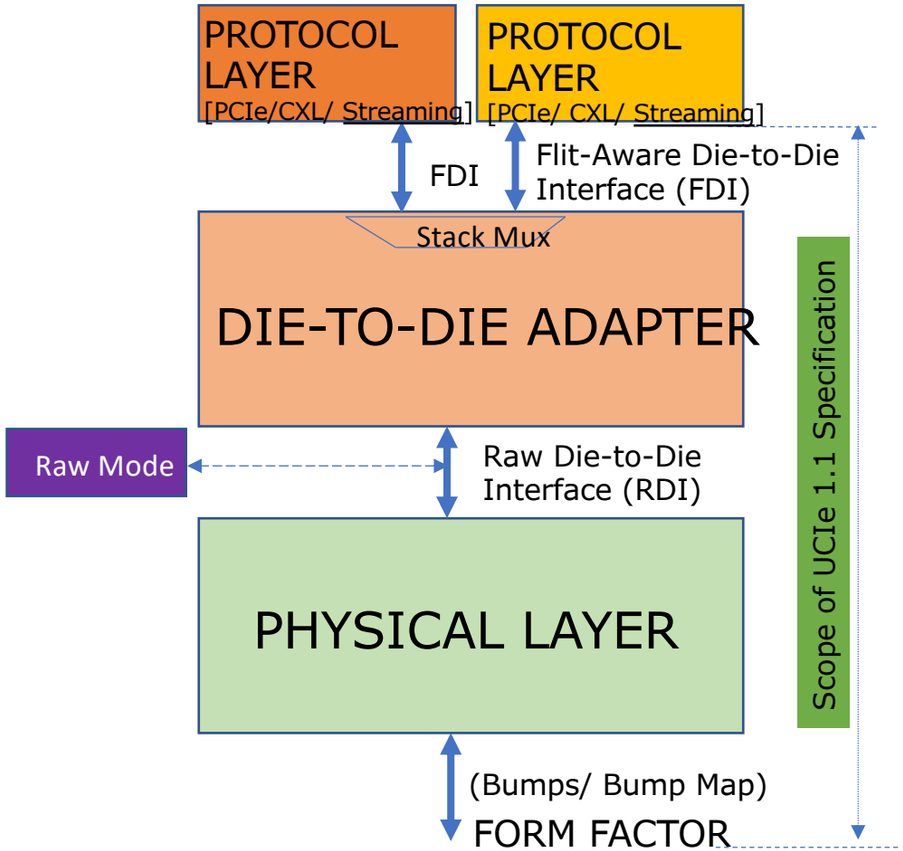
Cost Optimization for **Advanced Packaging**

Enhancements for **Compliance Testing**

UCIe 1.1 is Fully Backward Compatible with UCIe 1.0

UCIe 1.1: Streaming Protocols on Full Stack

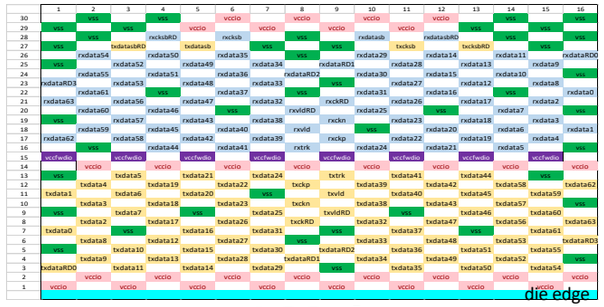
- UCIe 1.0 supports Streaming Protocol (e.g., AXI, CHI, SMP coherency protocols, SFI, CPI) only in Raw Mode
- Two enhancements with UCIe 1.1 (raw mode still supported)
  1. Streaming Protocols can use the D2D adapter
     - Enables them to reuse the CRC, Retry etc.
     - Mechanism: map streaming to existing Flit Formats at FDI interface
  2. Streaming Protocols can multiplex with other protocols with on-demand interleaving
     - Enables co-existence of multiple protocols (e.g., streaming for processing, PCIe for discovery, DMA, TLB, error reporting, interrupt, etc.) for different use cases
     - Mechanism: Protocol muxing for Streaming protocol with existing Flit Formats at FDI interface



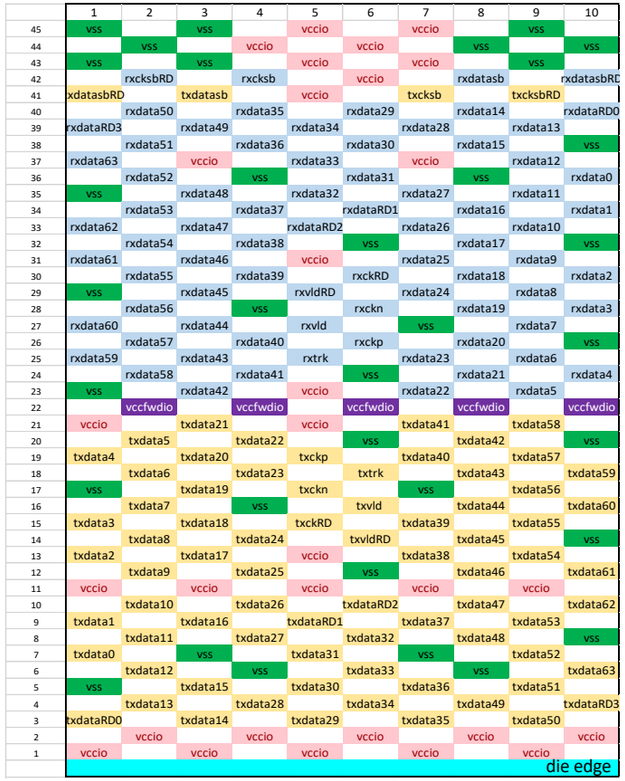
UCIe-A x64 Bump Maps

- New bumpout configurations for maintaining optimized BW/mm^2 across allowable bump pitch range
  - 8 and 16-column bump maps added to original 10-column in spec1.0
  - Suggested usage guideline:

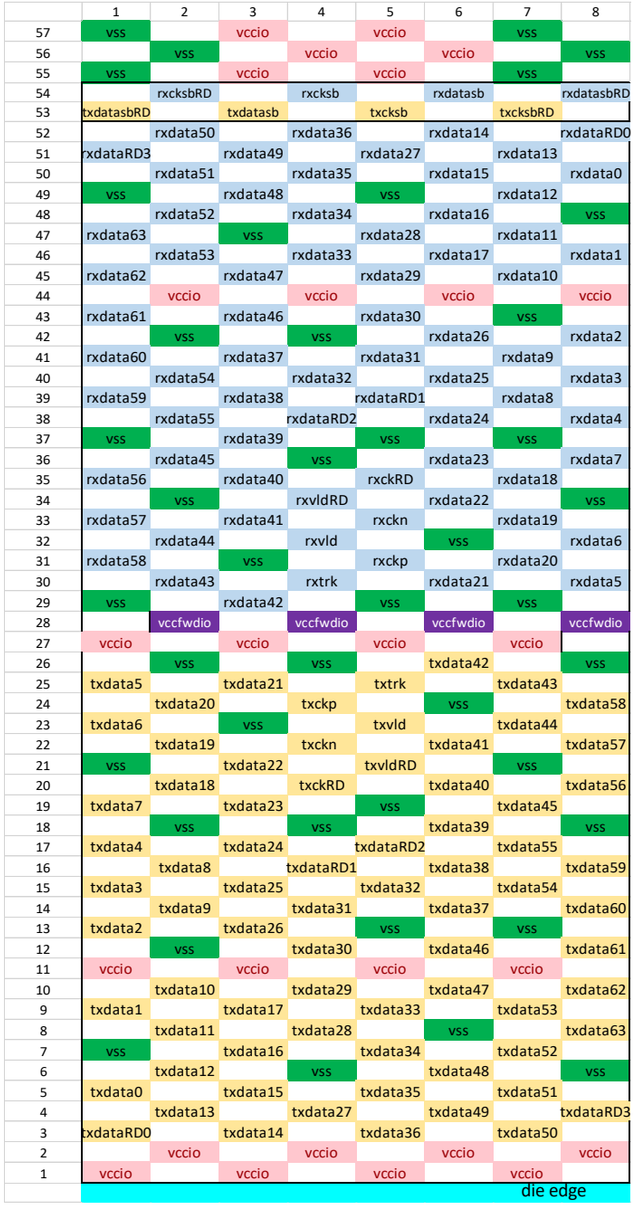
uBump Pitch (um)	Max Data Rate by Spec (GT/s)	# of Columns within 388.8um shoreline
25-30	12	
31-37	16	16
38-44	24	10
45-50	32	
51-55	32	8



16Col
Recommended for
25-37um bump pitch



10Col
Recommended for
38-50um bump pitch



8Col
Recommended for
51-55um bump pitch

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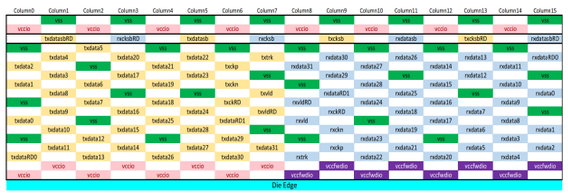
UCIe-A x32 Bump Maps

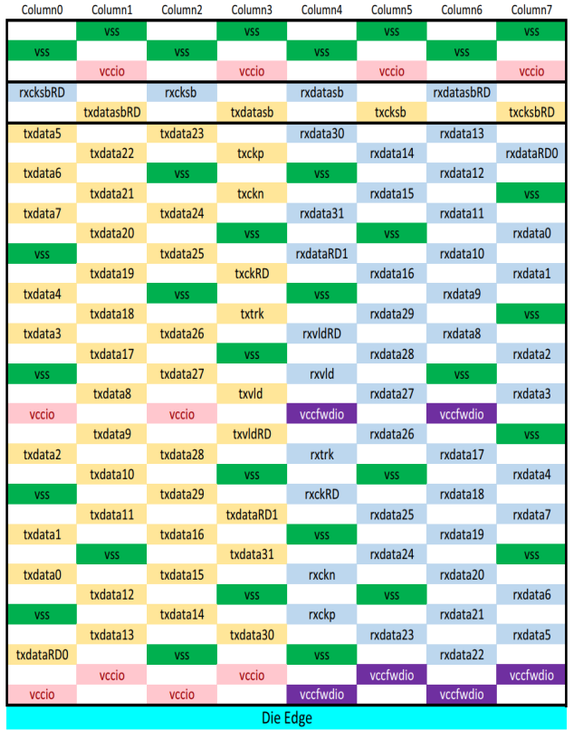
- Newly added x32 bump maps for further Si area & package tech flexibility
  - 8, 10 and 16-columns
  - Suggested usage guideline:

uBump Pitch (um)	Max Data Rate by Spec (GT/s)	# of Columns within 388.8um shoreline
25-30	12	16
31-37	16	
38-44	24	10
45-50	32	
51-55	32	8



16Col
Recommended for
25-37um bump pitch

10Col
Recommended for
38-50um bump pitch



8Col
Recommended for
51-55um bump pitch

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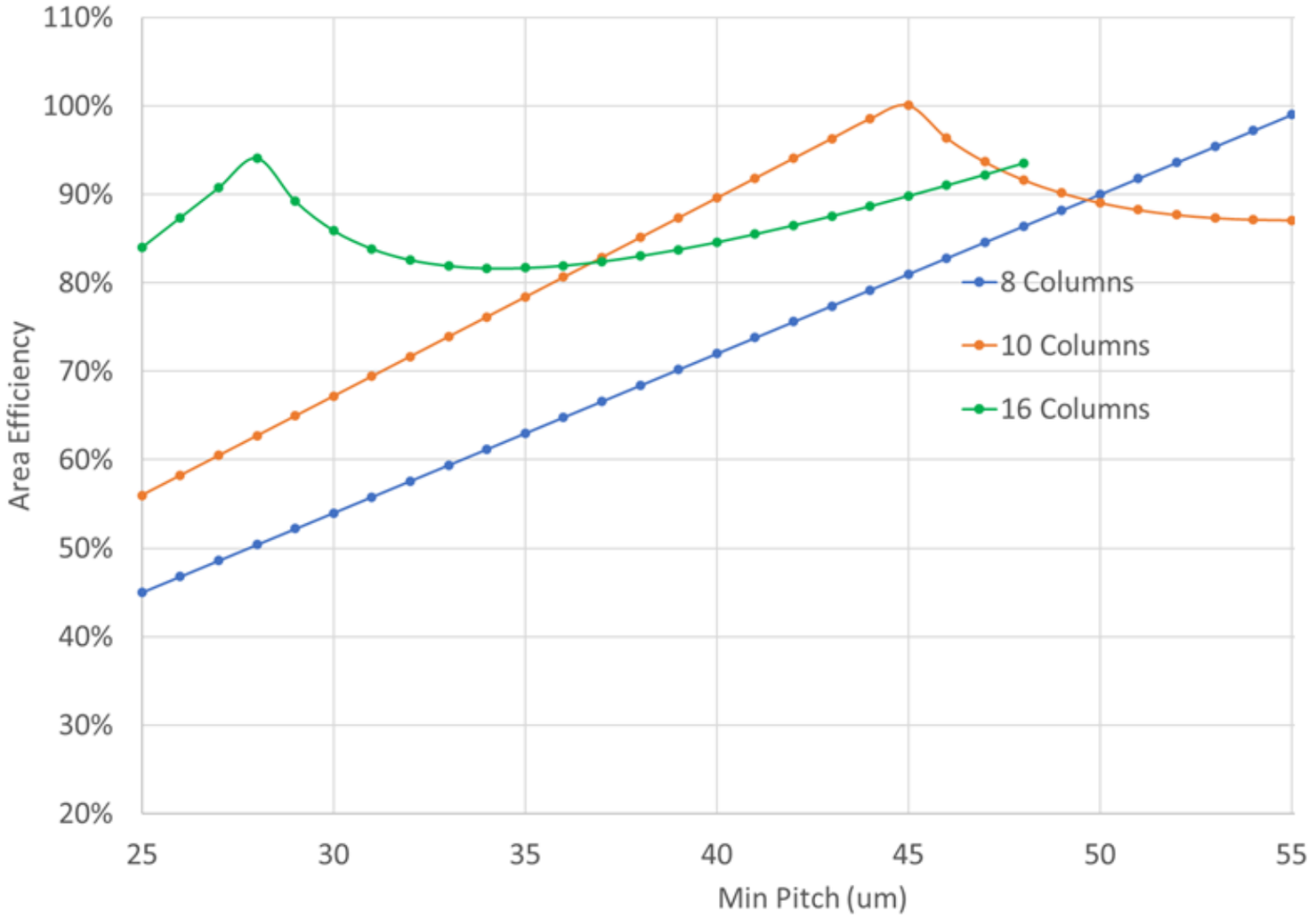
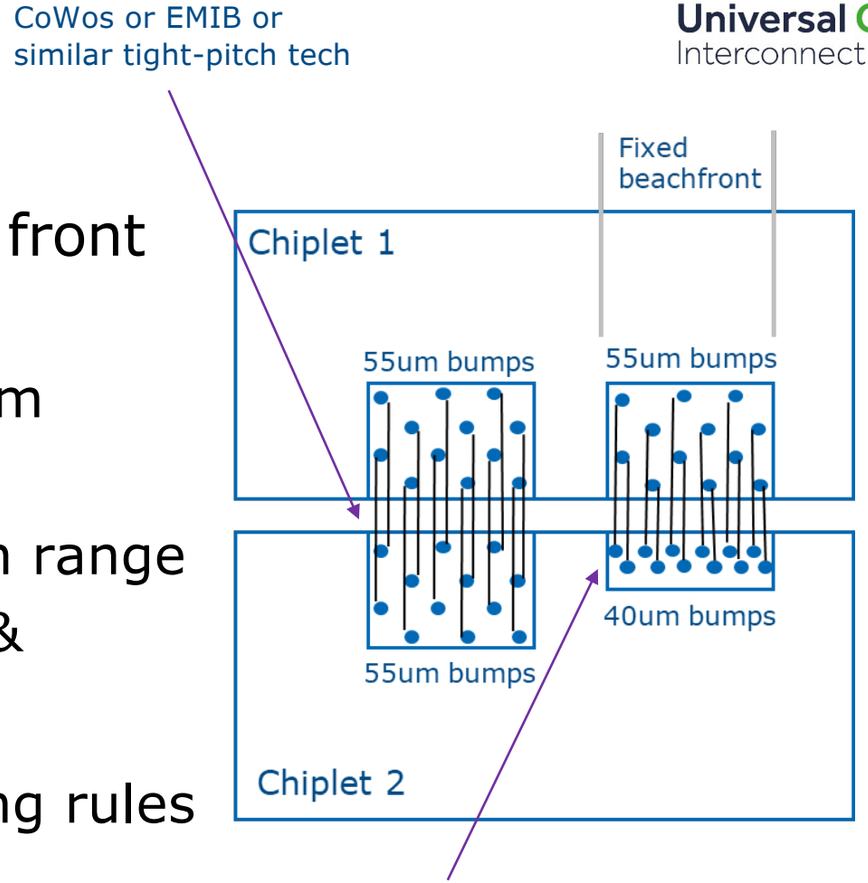
UCIe-A area/column type efficiency



- Points of overlap are the optimal cross-over points between recommended 8/10/16-column bump maps
- At the lower bump pitch range, >80% area efficiency is acceptable given overall magnitude of PHY depth is lower
- As bump pitch increases, >90% area efficiency is desired due to the much bigger PHY depth (um)
  - Example: 10% of 1000um is greater than 20% of 400um

UCIe-A Interoperability

- Advanced package planning of key parameters up front for interop across IDMs/OSATs:
  - PHY beachfront must be defined to balance BW/mm capability and mechanical compatibility
  - Inter-generational compatibility across bump pitch range
    - Fixed beachfront (388.8um) per PHY module &
    - Signal ordering rules
  - Comprehensive PHY placement & rotation/mirroring rules



- With the reduction of bump pitch, the number of rows decrease while the number of columns increase
- Interop is enabled by a fixed beachfront & following signal ordering rules

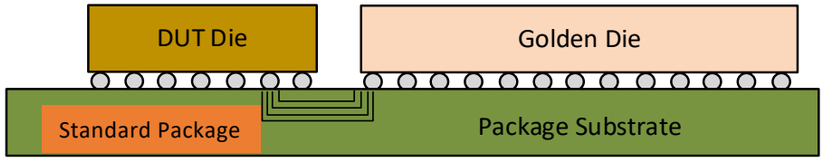
Compliance & Interop

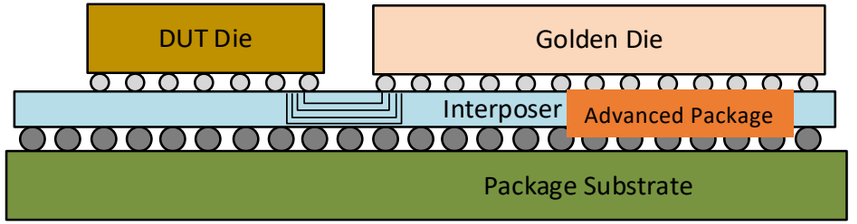
- Spec 1.1 enhanced with compliance setup & tests
- Standard package & advance package
- Inter-connectivity setup & testing – active in FFCWG now
- Two options for compliance setup
  1. Reference package with Golden Die and DUT
  2. Custom package with Golden Die and DUT
- Compliance types
  1. Up to RDI: Electrical & Channel only
  2. Up to FDI: Electrical, Channel & protocol/streaming

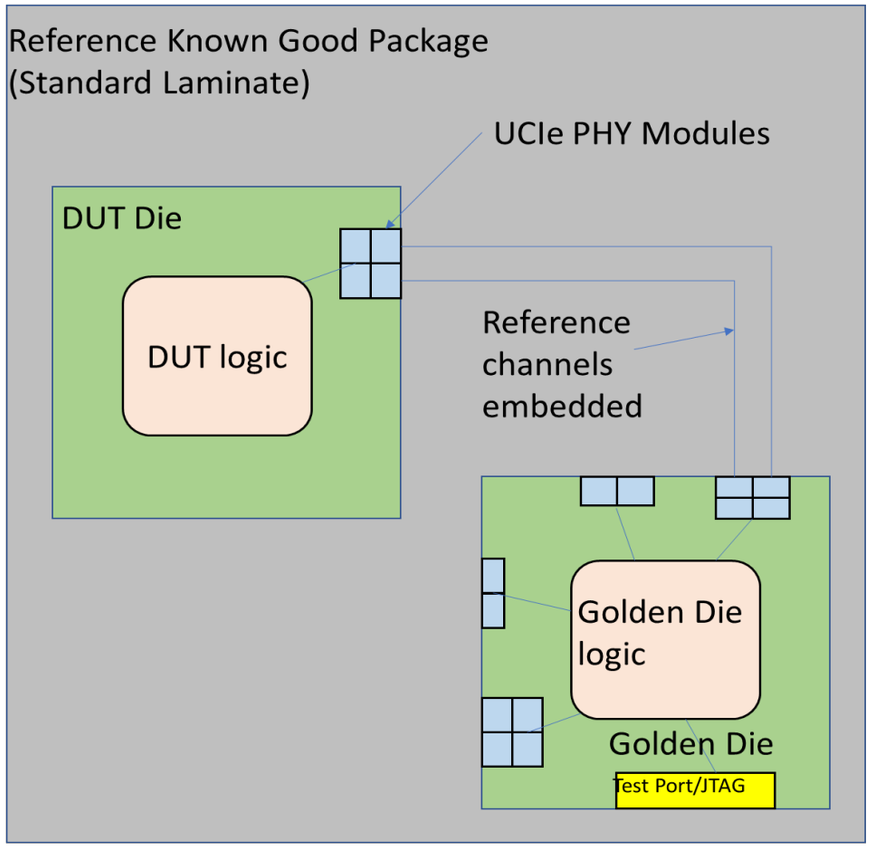
UCIe Compliance: Setup

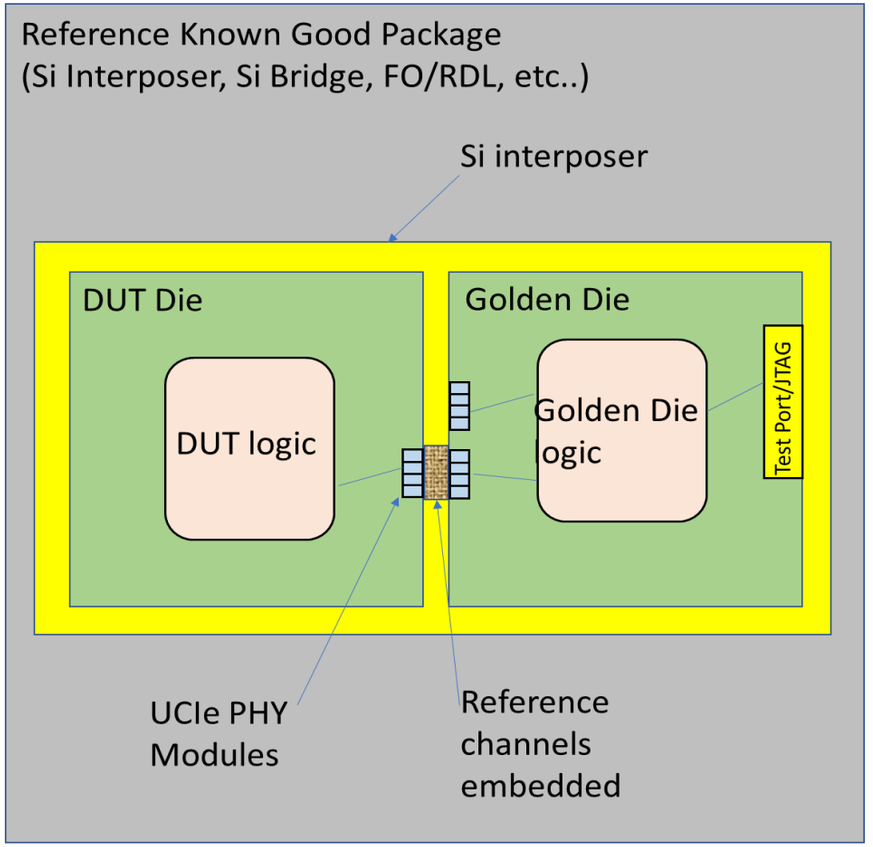
Ingredients

- Known good package with Reference Channels
- Golden Die
- DUT







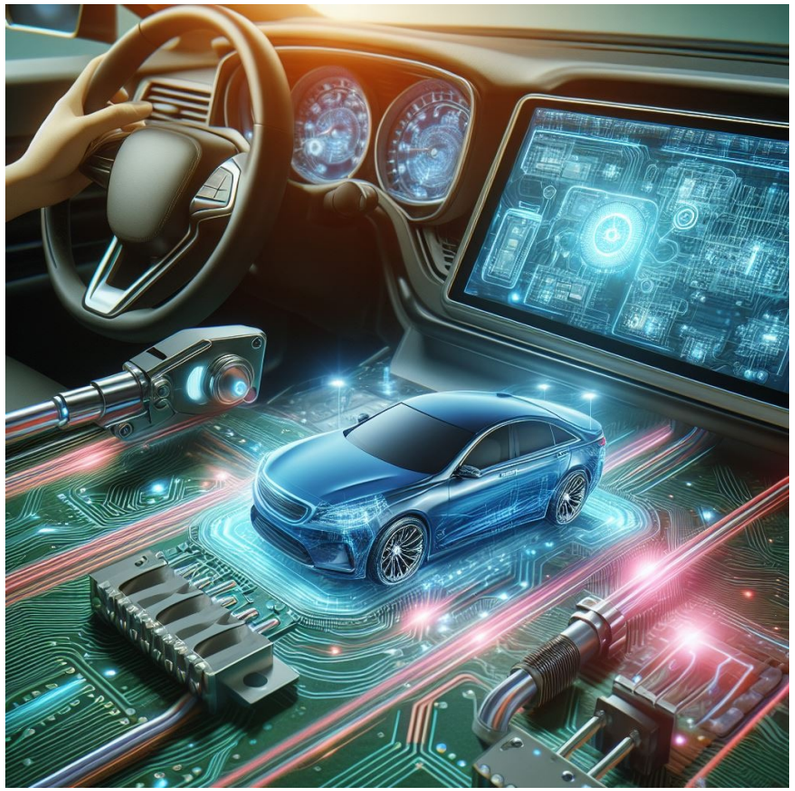


UCIe 1.1: Automotive Enhancements

Automotive compute workloads are growing into what used to be supercomputer level.

Automotive SoCs challenges:

- Cost
- Flexibility
- Time-to-Market



Industry is looking to chiplets. Safety Integrity is critical. System reliability requirement translates into additional I/O features.

- ➢ Preventive Monitoring
- ➢ Run-time Testability of Link Health
- ➢ Field Repairability

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Stages of Chiplet Evolution

UCIe Workgroups and Key Initiatives

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Workgroups

- Electrical
- Form Factor & Compliance
- Manageability & Security
- Marketing
- Protocol
- Systems and Software
- Automotive

Key Initiatives

- UCIe 3D
- Interoperability & Compliance
- Manageability & Security
  - Management Transport
  - Memory Access Protocol
  - MCTP
  - Test and Debug
  - Power Management

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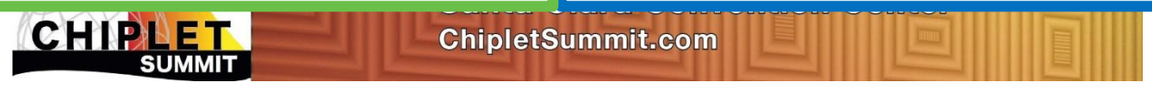
130+ Member Companies and growing!

Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive
The open chiplet ecosystem.

JOIN US!

Alibaba Group
AMD
arm
ASE GROUP
Google Cloud
intel
Meta
Microsoft
NVIDIA
Qualcomm
SAMSUNG
tsmc



Thank You

www.UCIexpress.org

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