New 3D IC design kits cover both design and packaging

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Anthony Mastroianni | Siemens EDA

Tutorial E, Design Methods, Feb 6, 2024

Agenda

1 Background of chipletization and packaging

2 A 3D-IC example to motivate design kit need

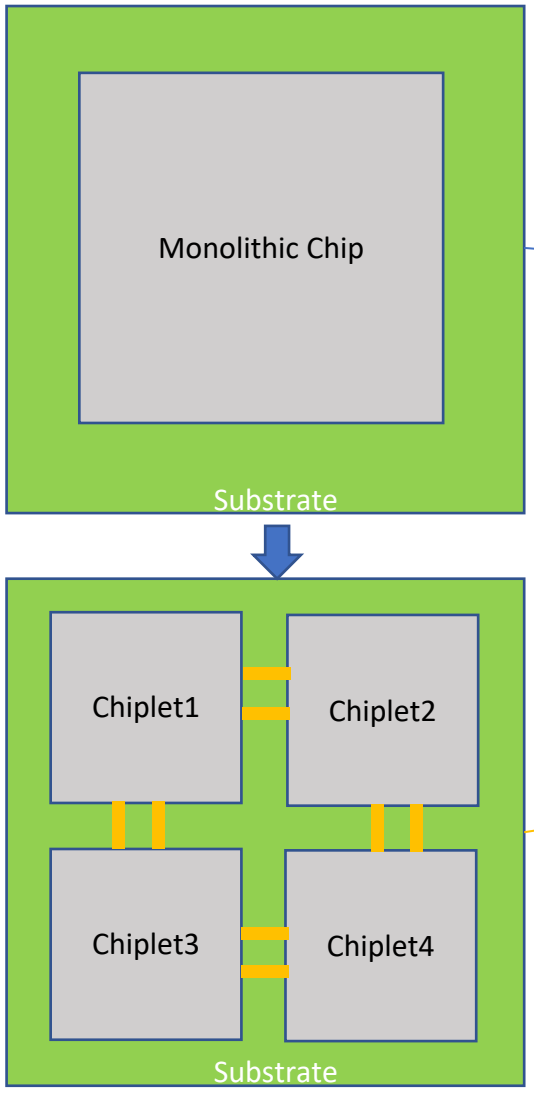
3 3D-IC Design Kits under development at OCP

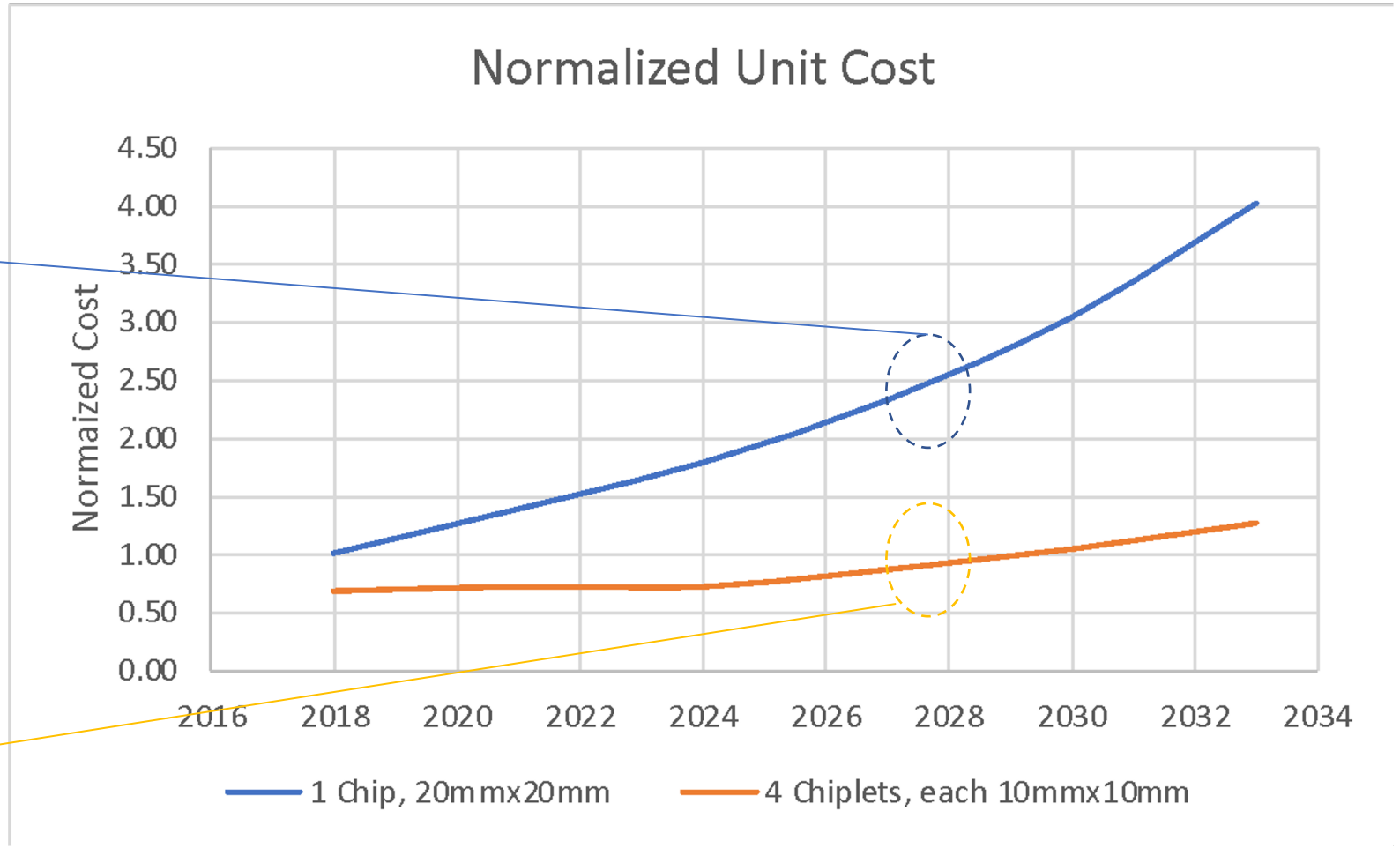
4 Summary and Q&A

Background

Chipletizing large silicon dies

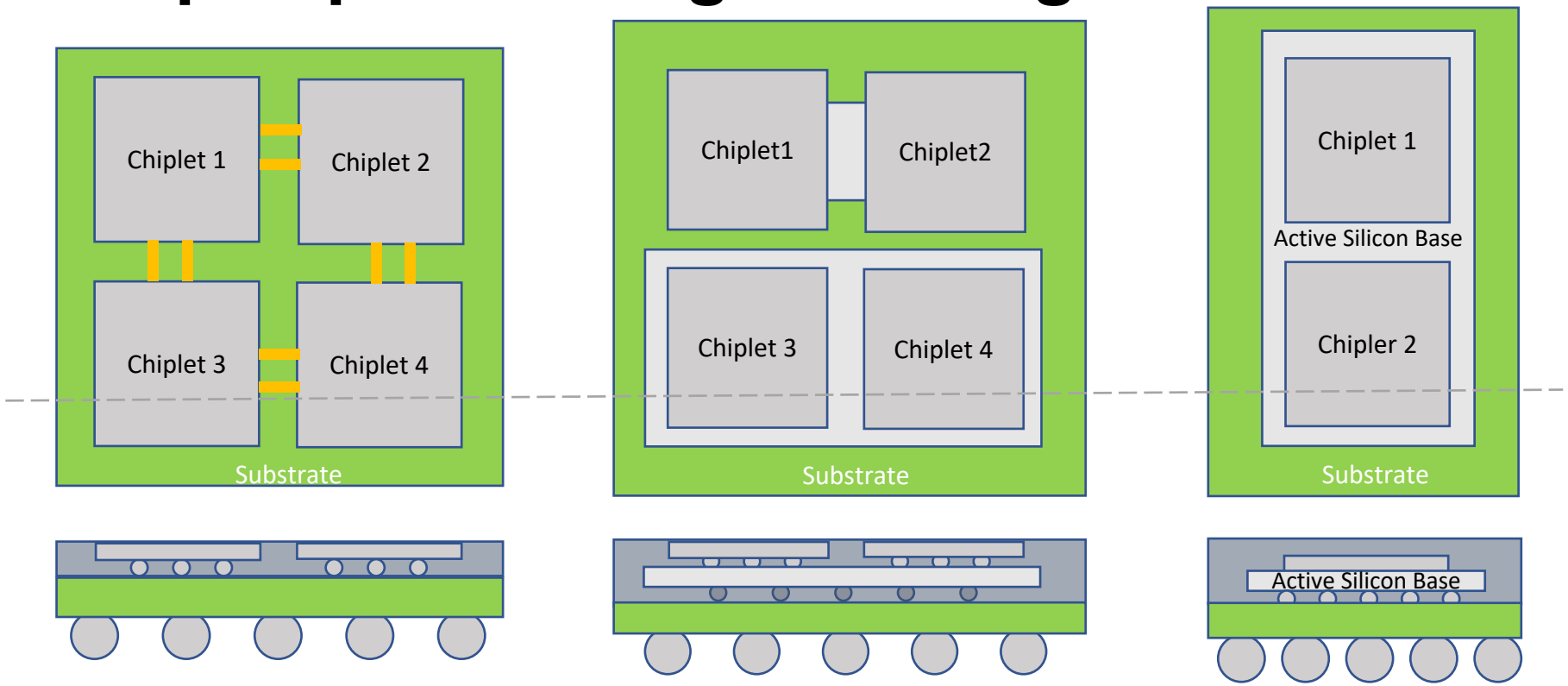
Benefits of chiplets (cost)





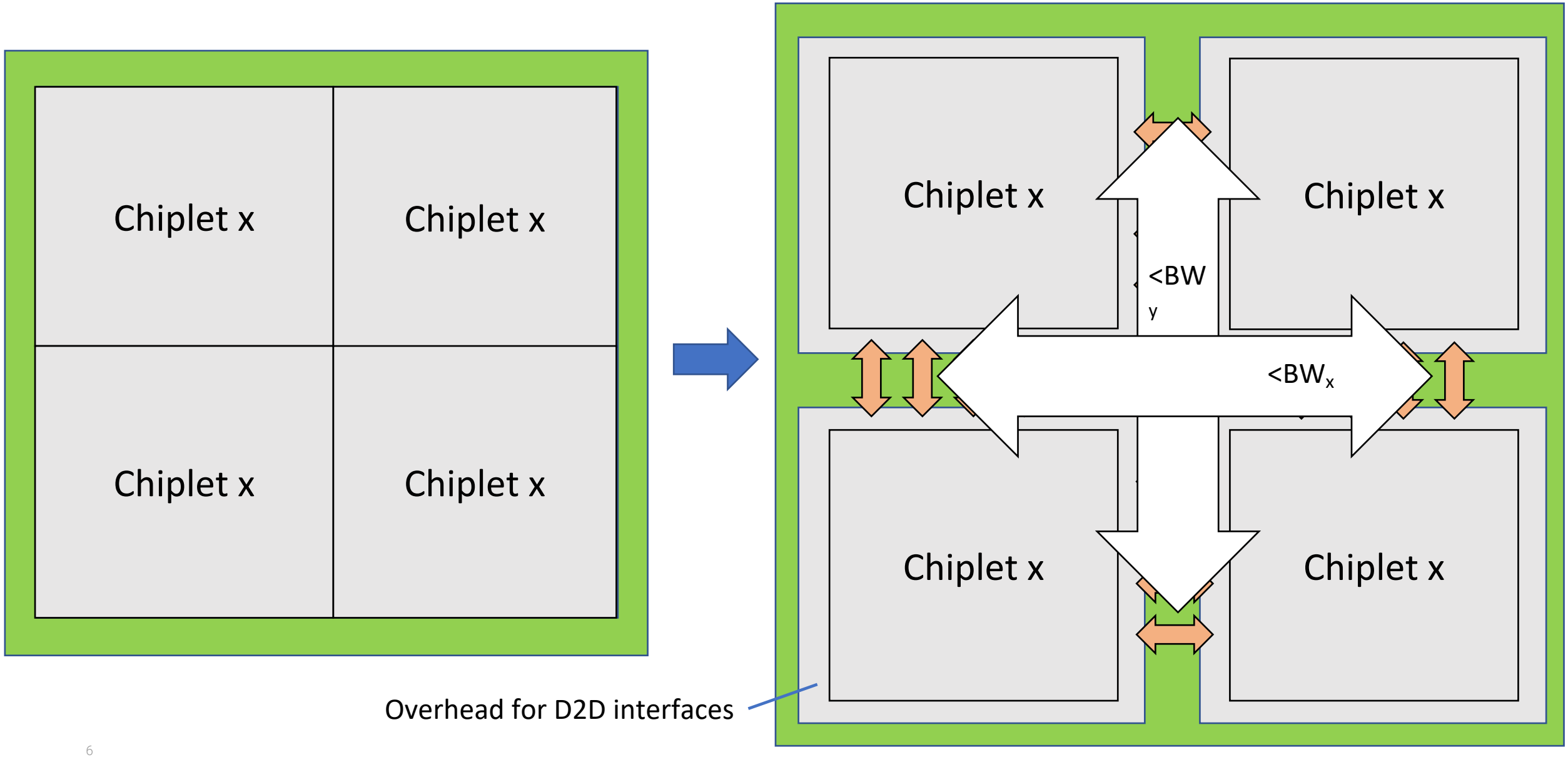
With proper architecture and design, Chiplets enable cost optimization.
(Need to Control Overhead Cost)

Chiplet partitioning and integration



	2D Side by Side MCM	2.xD Interposers + Bridges	3D-IC
New Technology	Chiplets, Fine Pitch Substrates	Chiplets, Fine pitch Interposers	Chiplets, Cu-Cu Bonding in Fab
Applications	CPU, GPU, AMS, SIP, RF	HBM, IoT/zGlue, CPU	HPC and more
Opportunities	Fine Pitch Substrate, Thermal	Thermal, Performance	Thermal, Performance

Uniform chiplet partitioning



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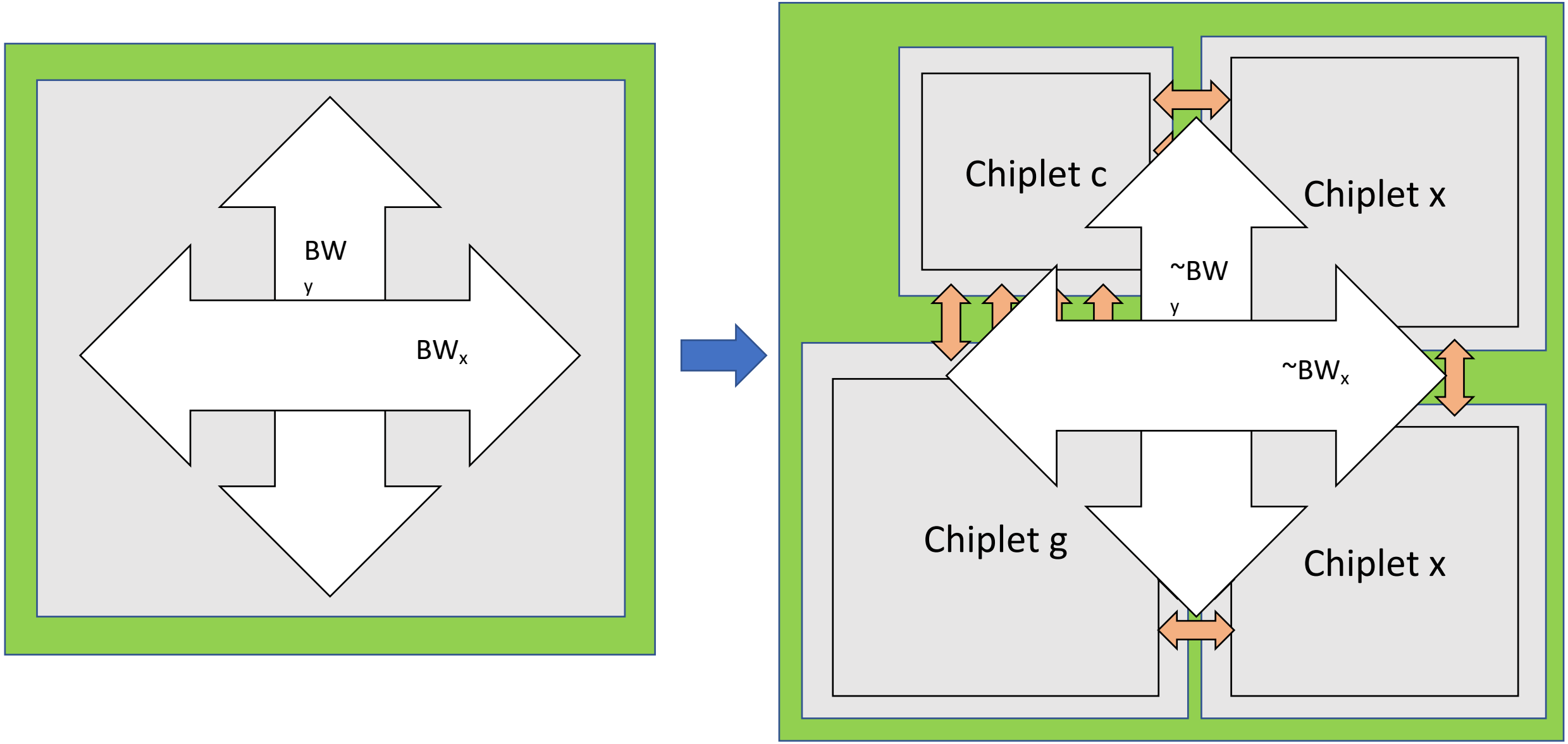
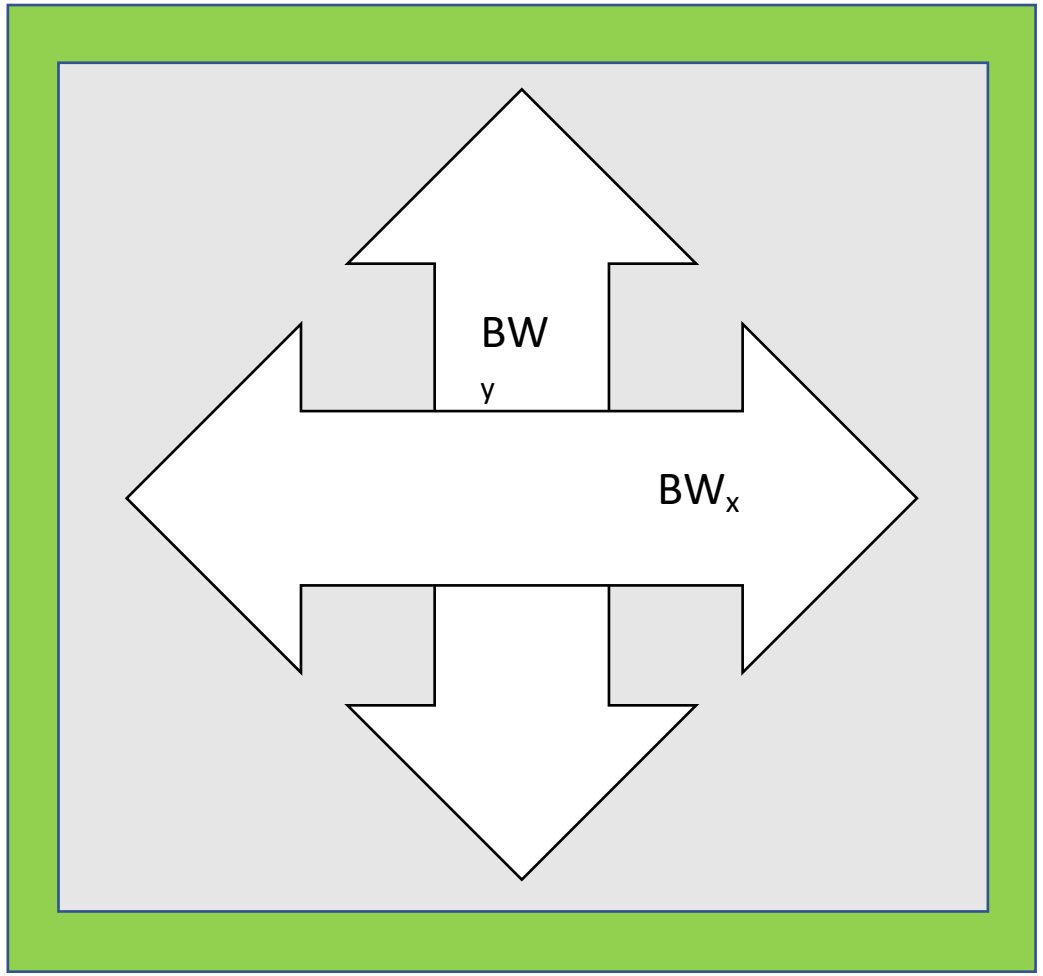
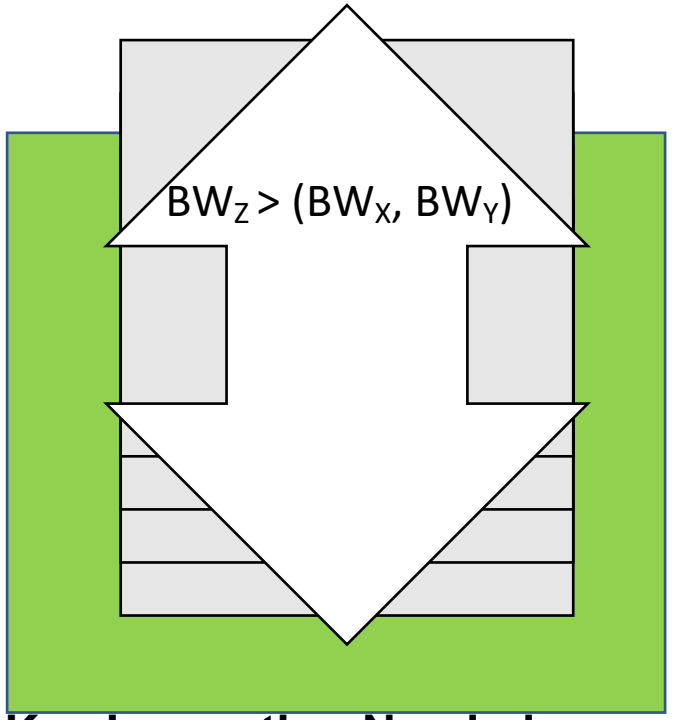
Functional chiplet partitioning



3D-IC chiplet partitioning

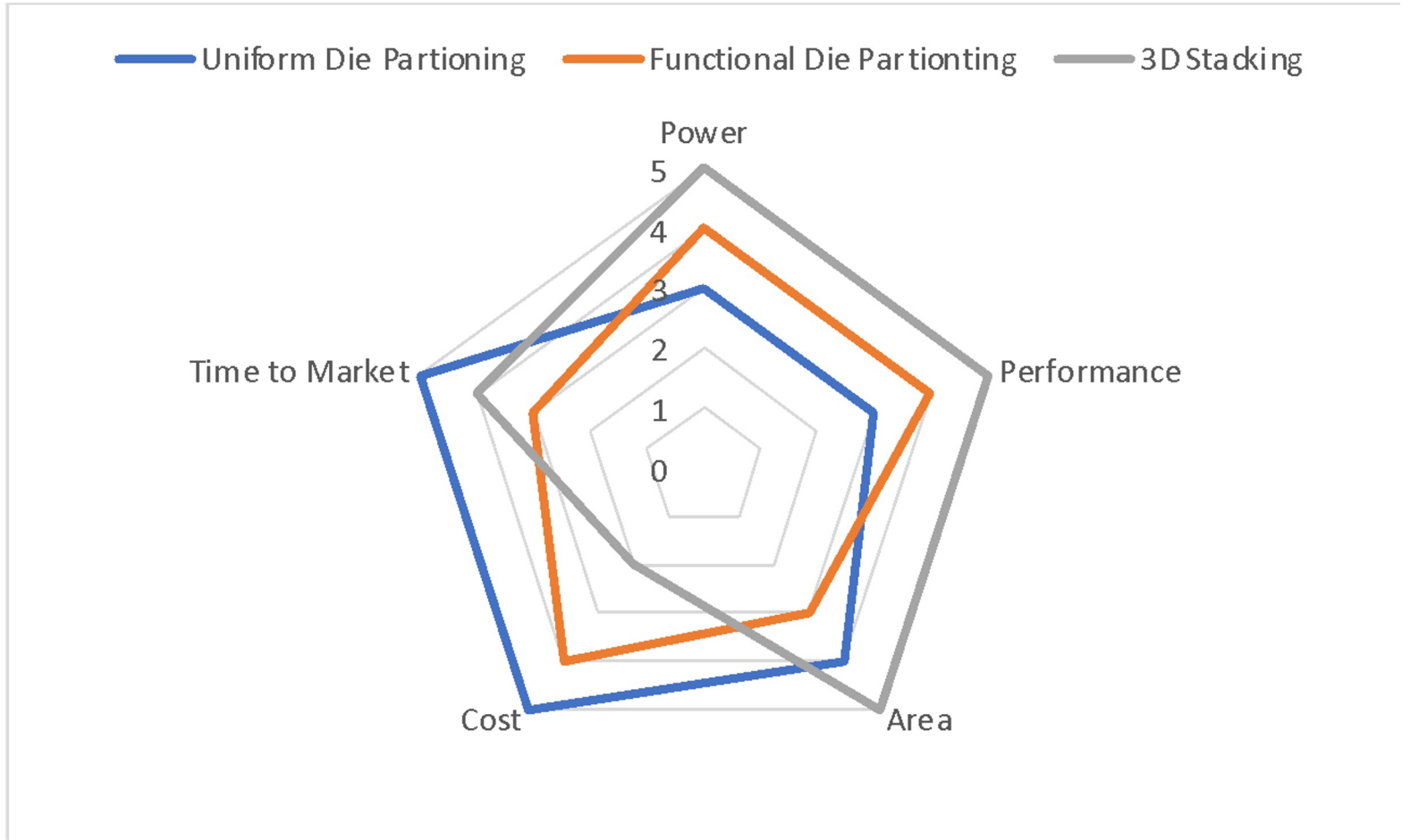




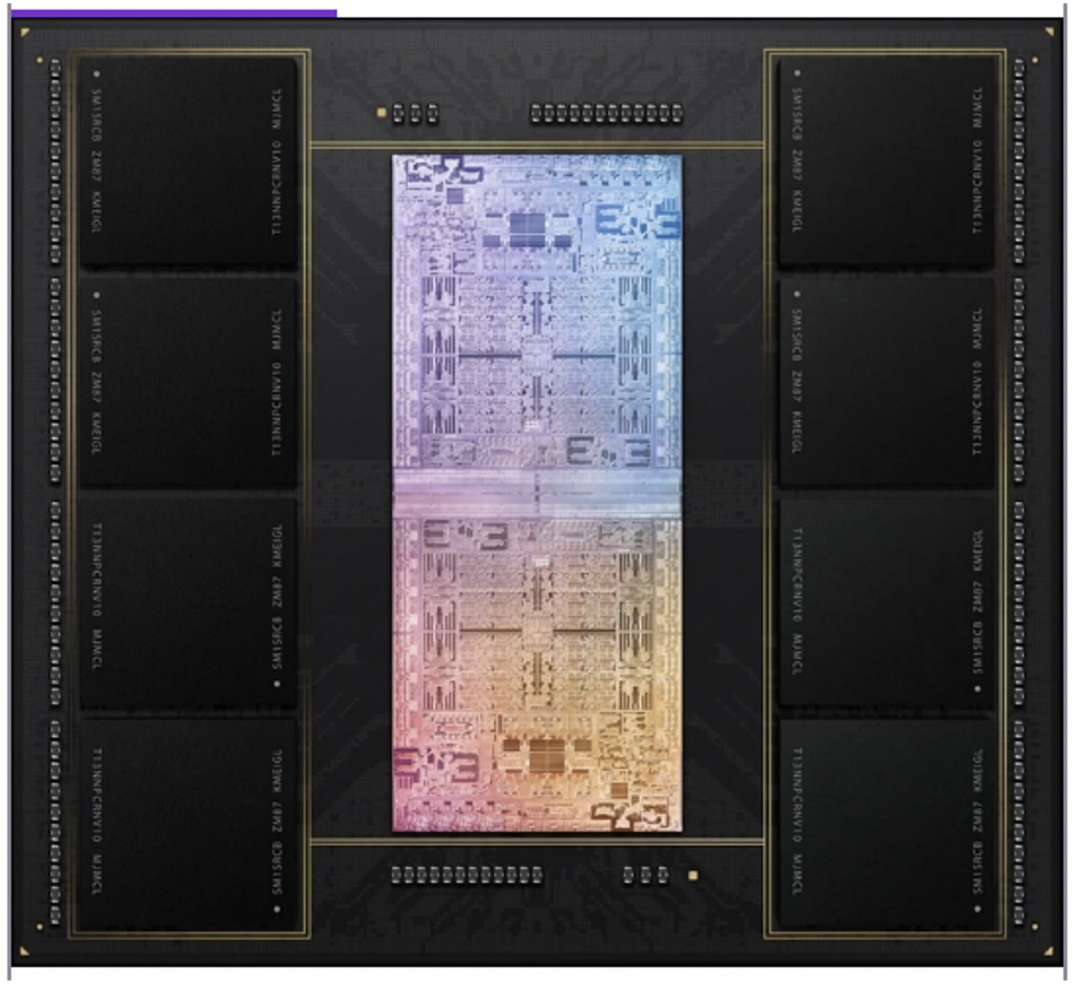
Key Innovation Needed:

- Vertical Bonding Technologies
- Heat Removal Technologies

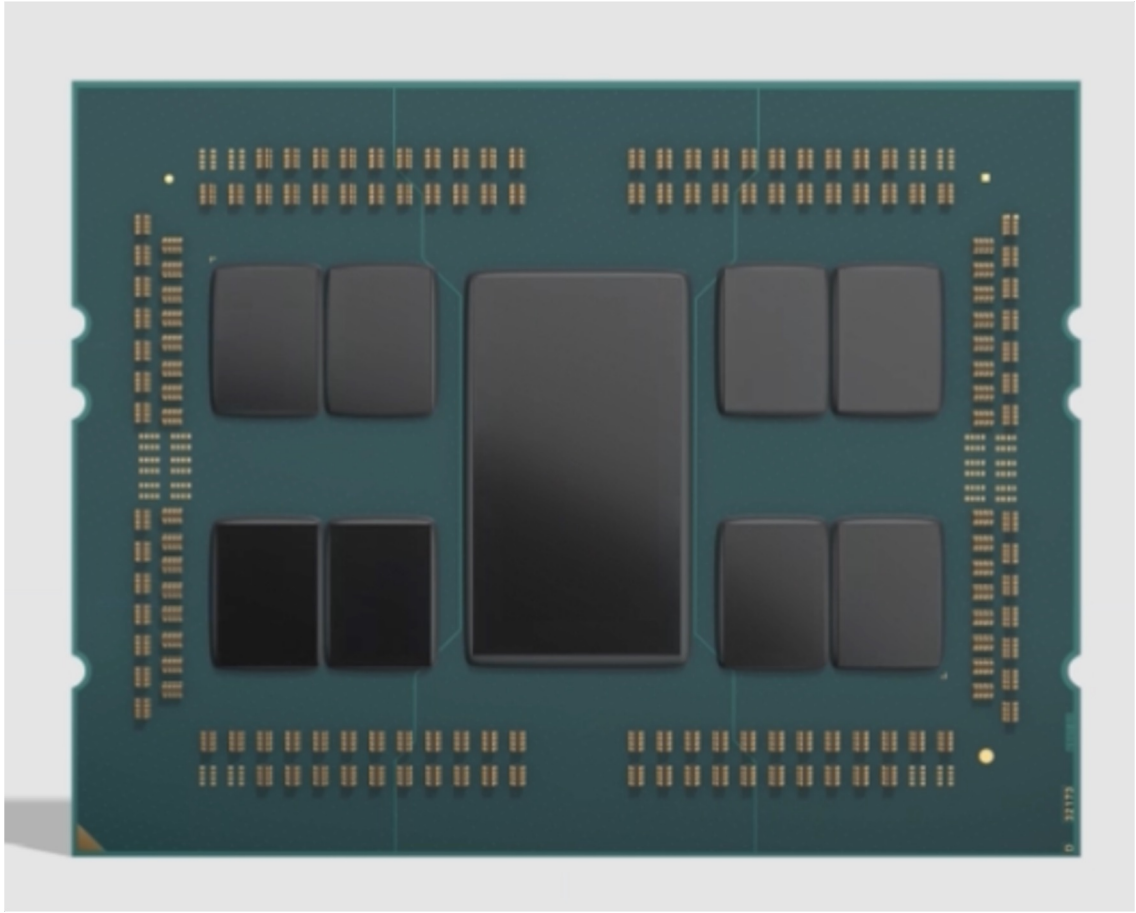
Chiplet partitioning



Chiplet partitioning examples

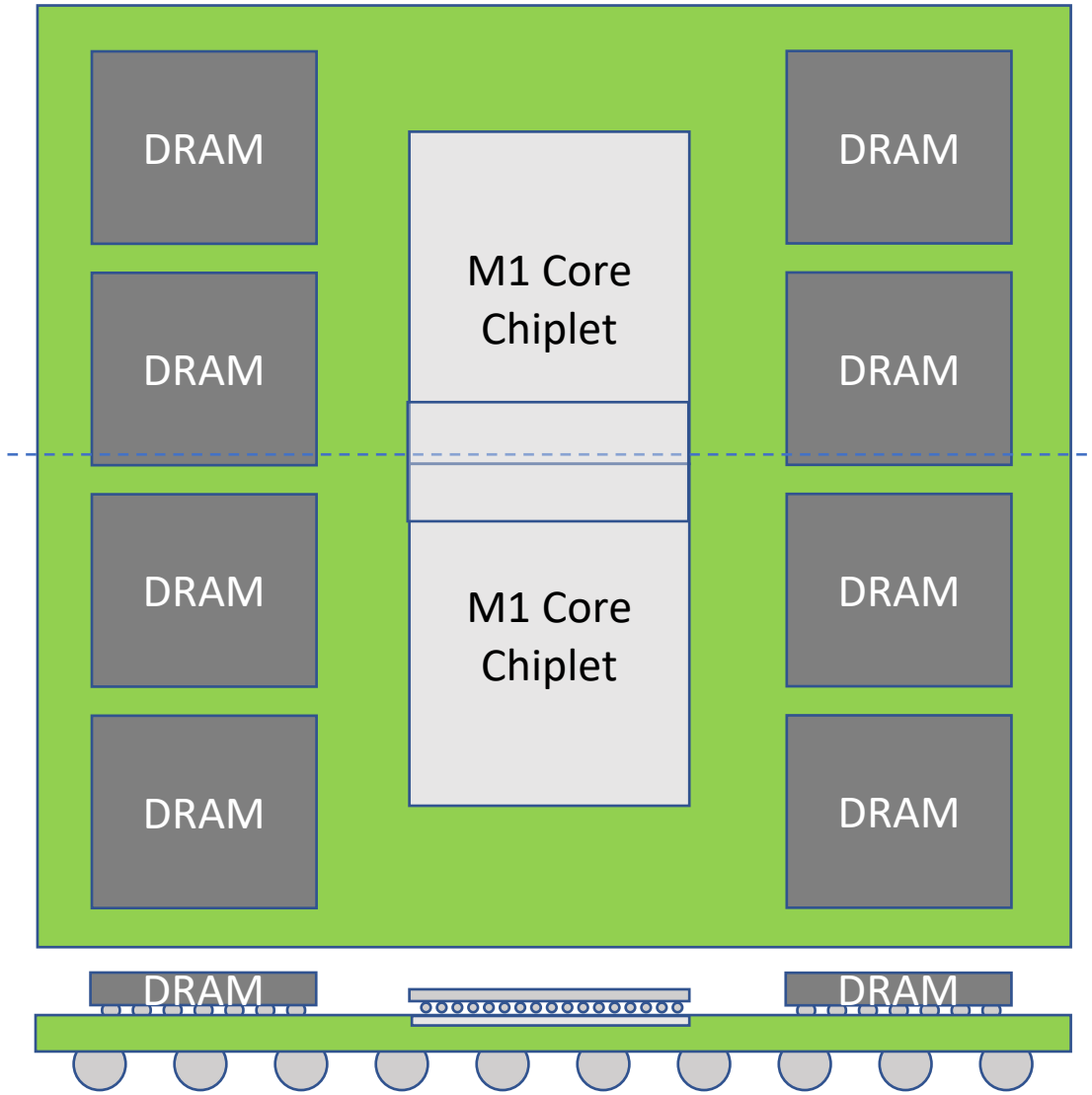


Apple M1 Ultra (2022/5nm)



AMD EPYC (2018/7nm)

Chiplet partitioning examples



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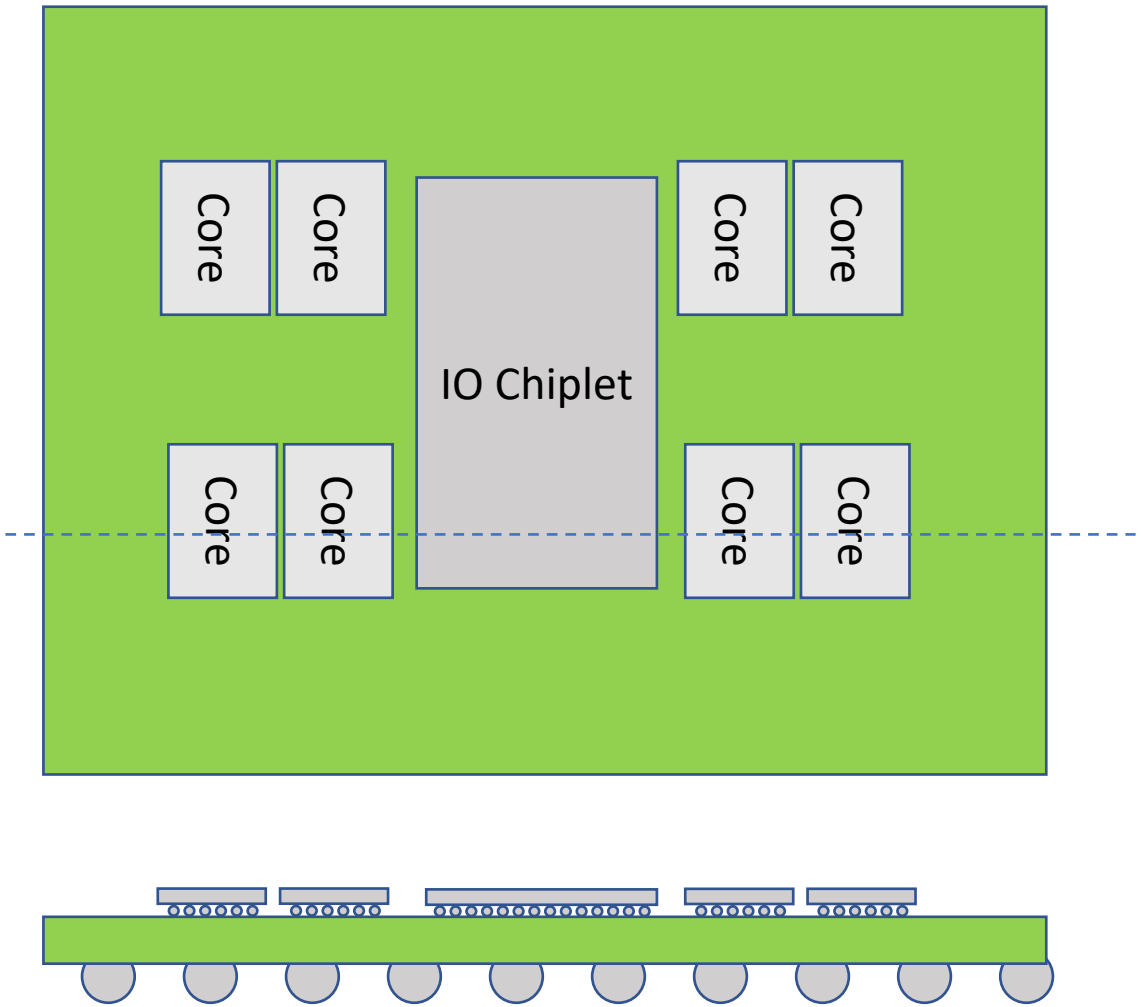

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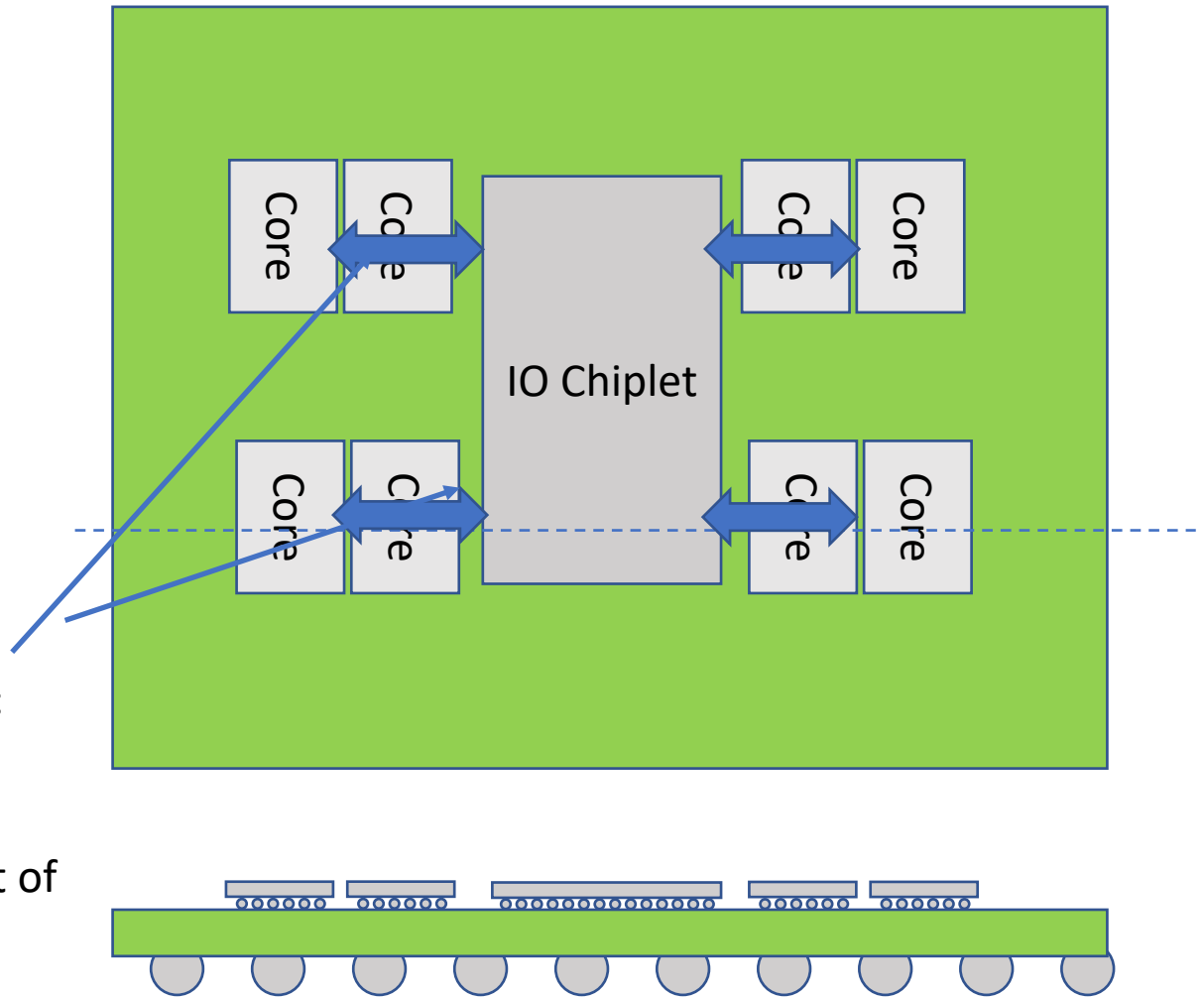
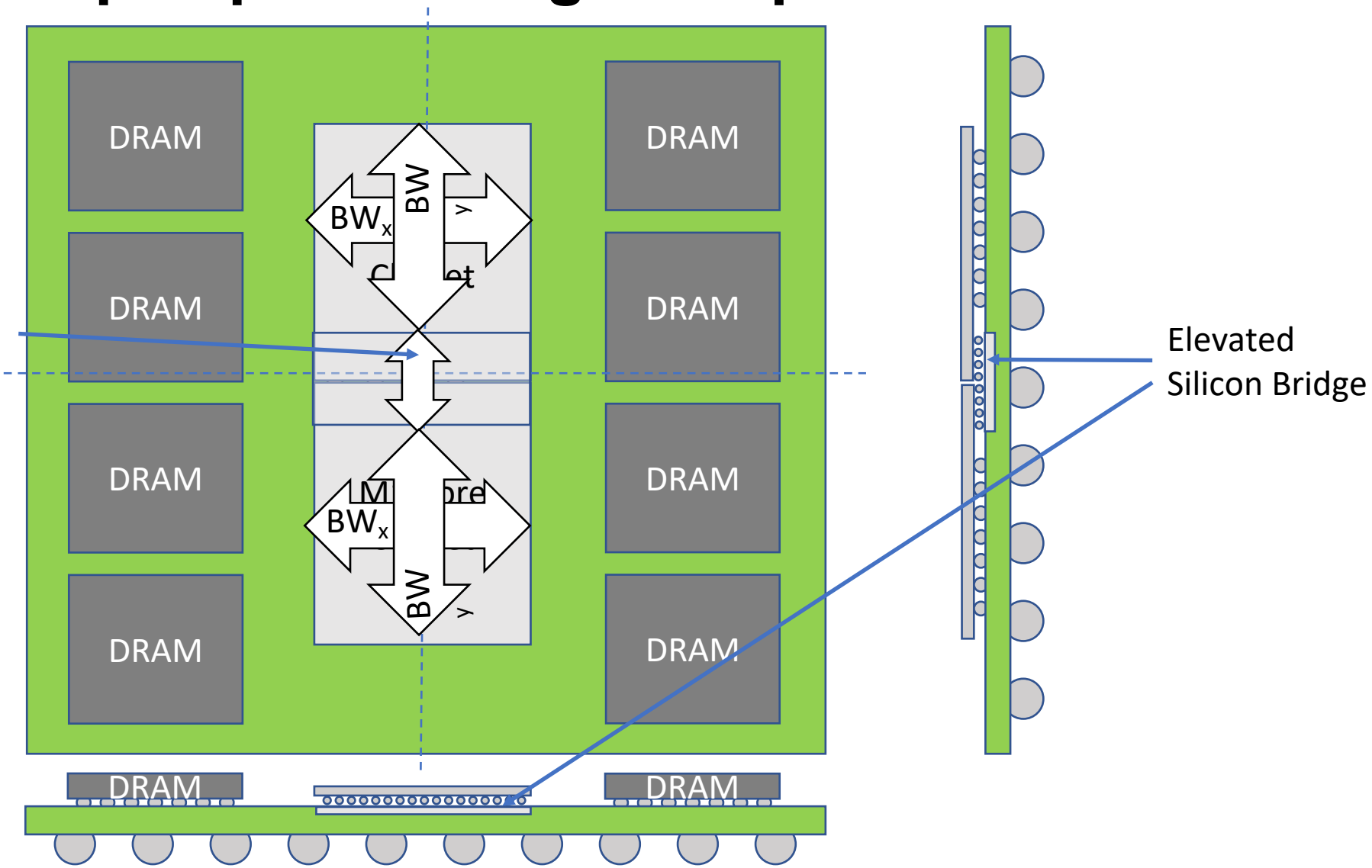


- SerDes based Infinity Fabric
- D2D Parallel Interfaces can improve PPA but at the cost of design complexity

AMD EPYC

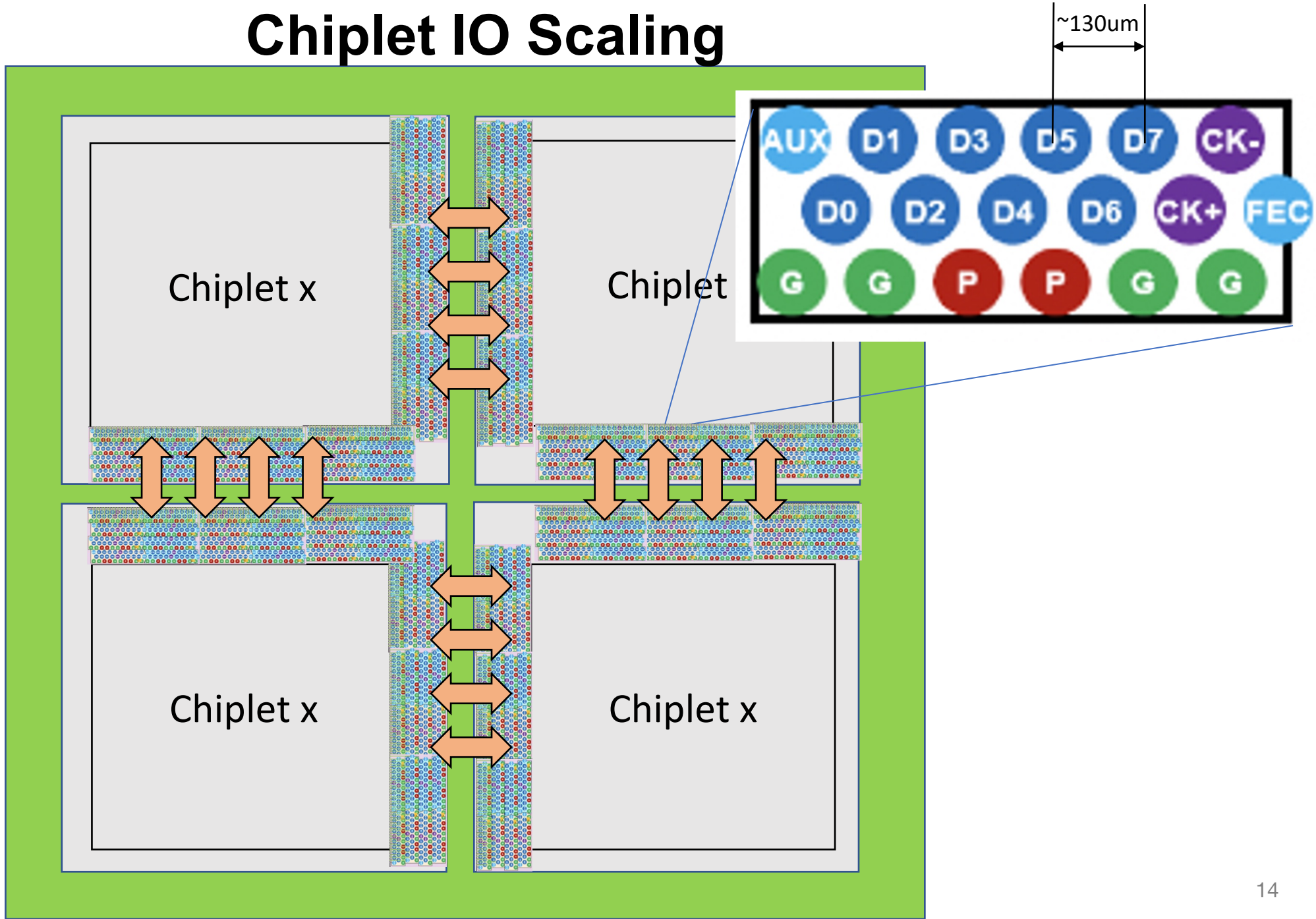
Chiplet partitioning examples

Band Width = 2.5TB/s UltraFusion
~10000 wires



Apple M1 Ultra (2022/5nm)

Chiplet IO Scaling



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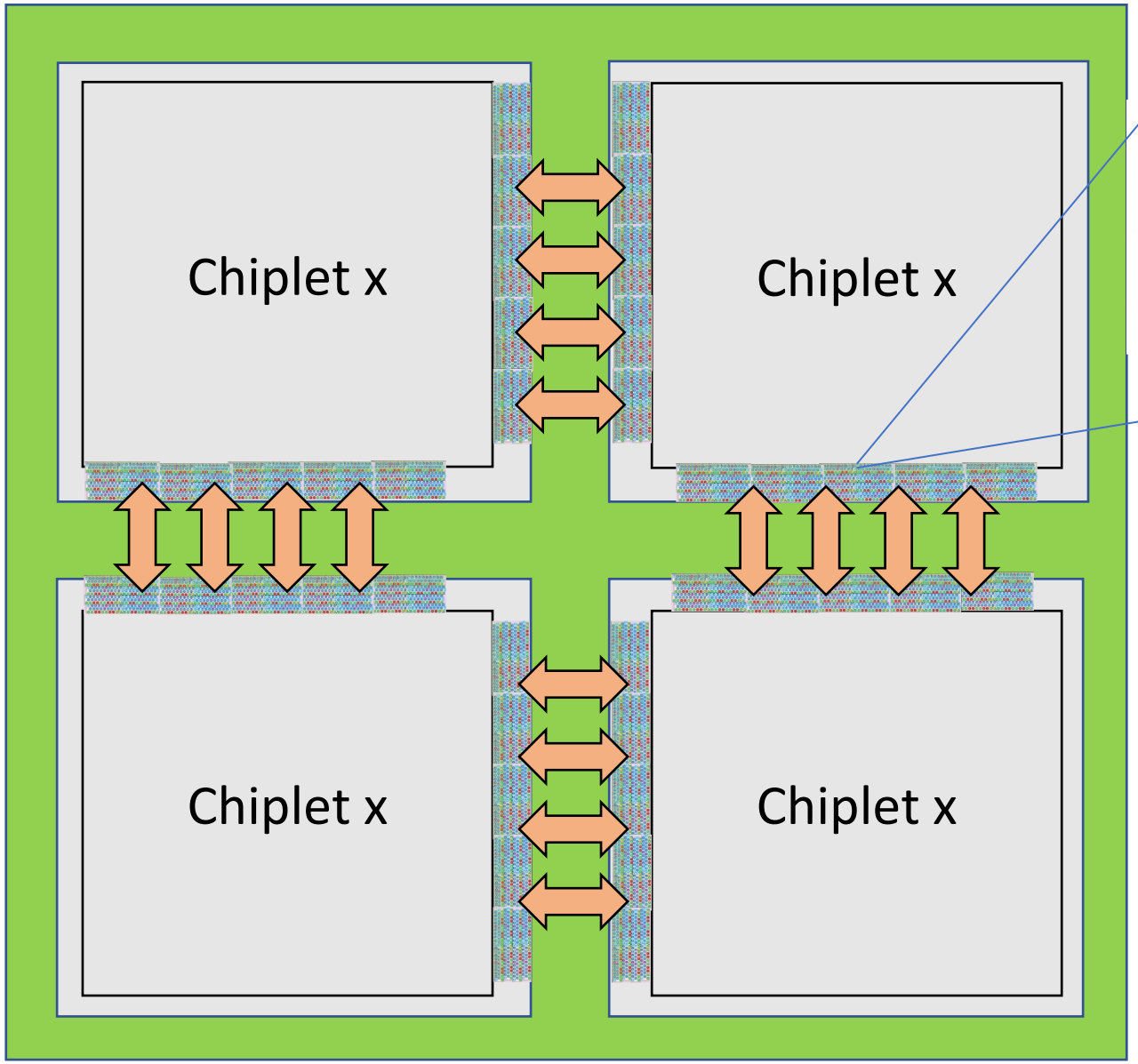
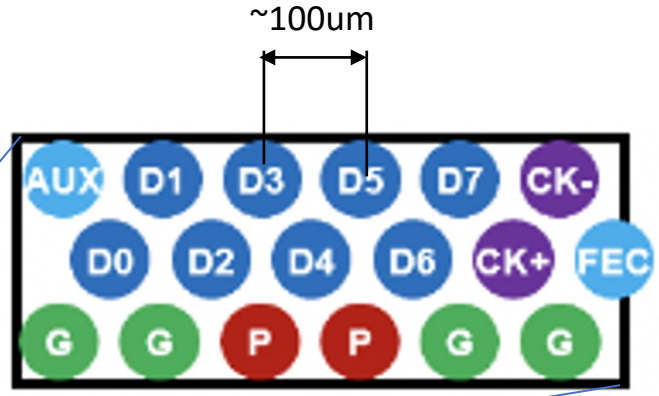
Chiplet IO Scaling





Dennard Scaling

Transistor Scaling: 0.7

Freq: 1.4 x

Power Reduction: 0.5 x

Chiplet Scaling

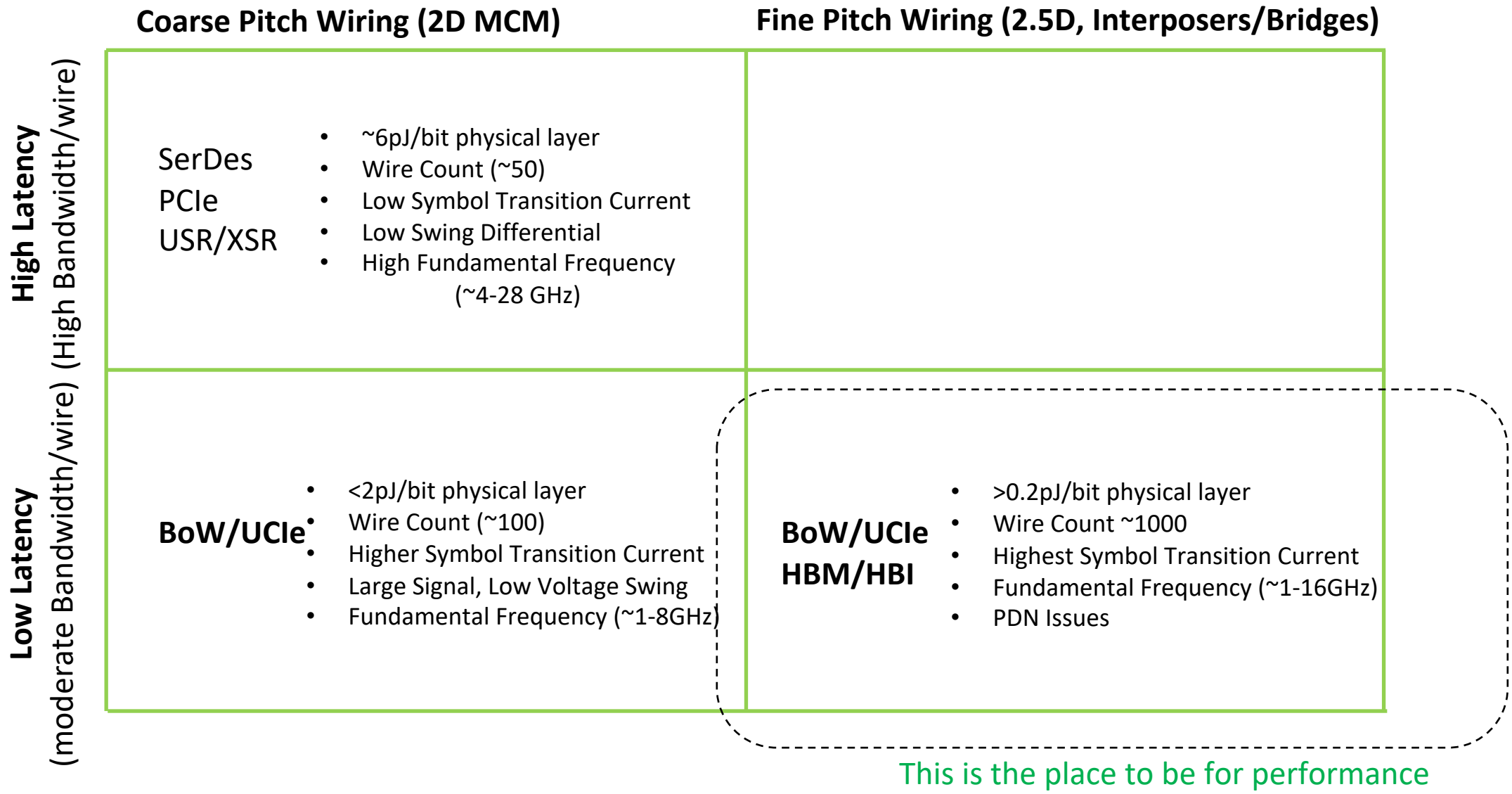
IO Scaling: 0.77 x (130->100)

Bandwidth: 1.7 x

D2D area overhead: 0.77 x

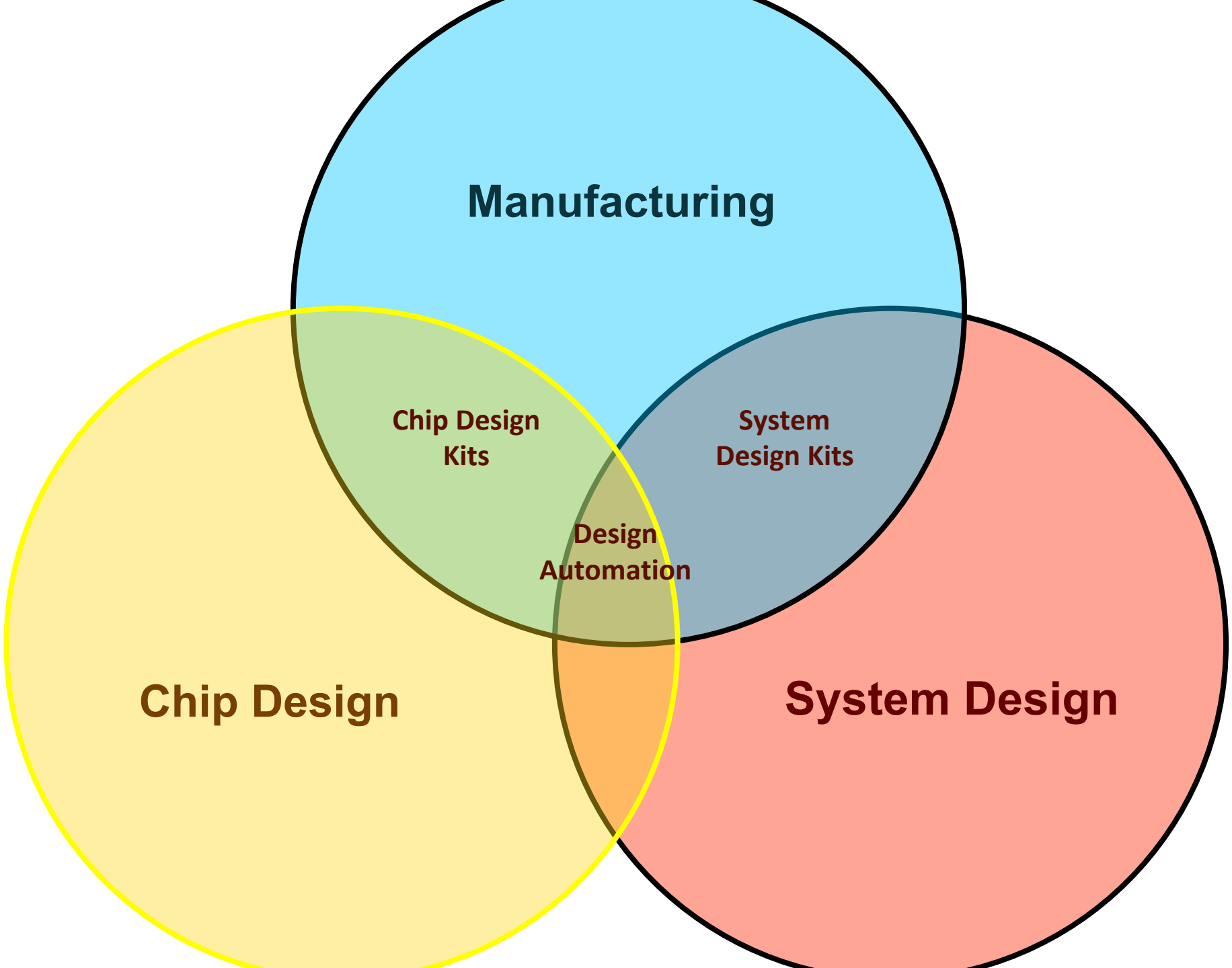
15

Chiplet die-to-die IO

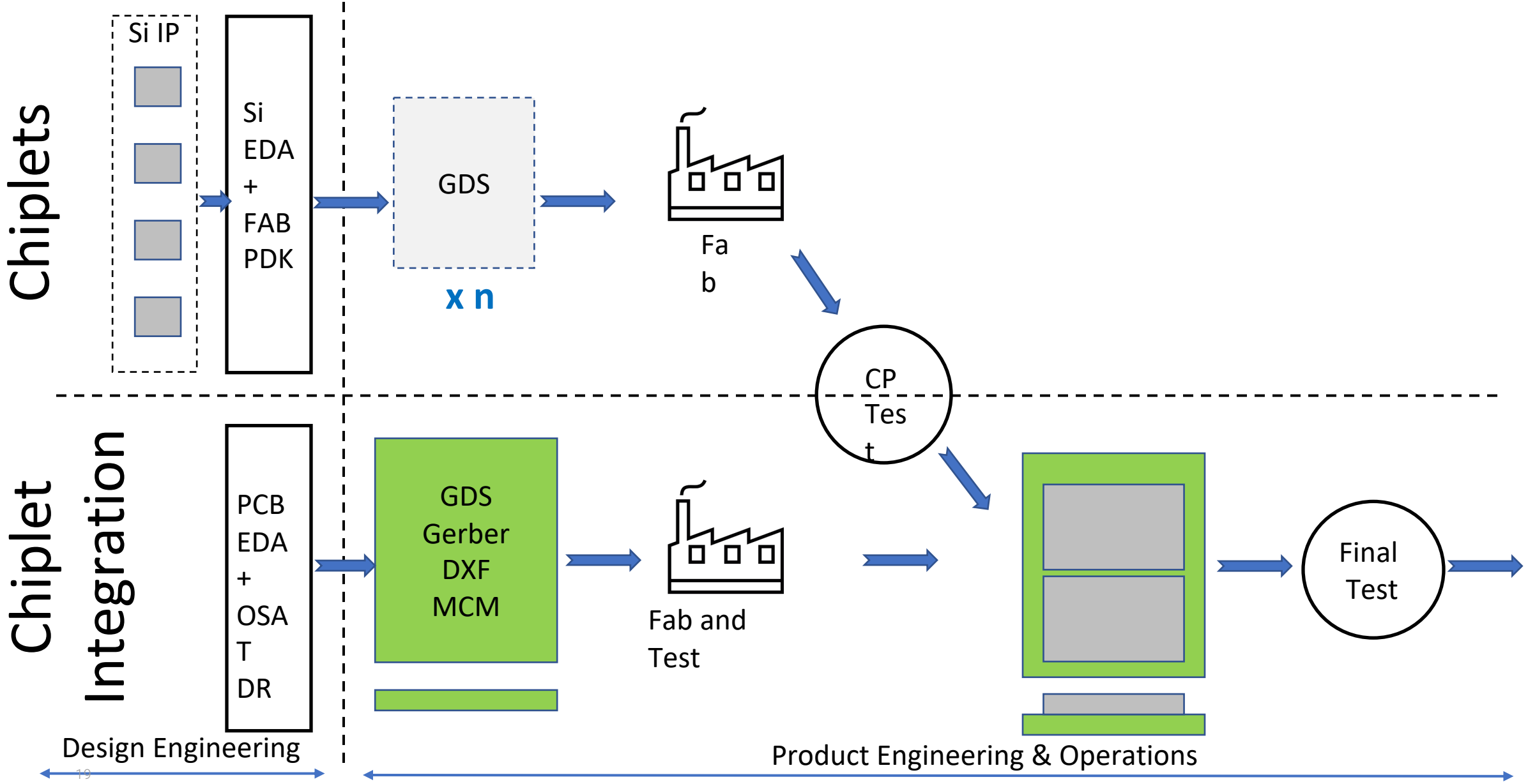


3DIC design example

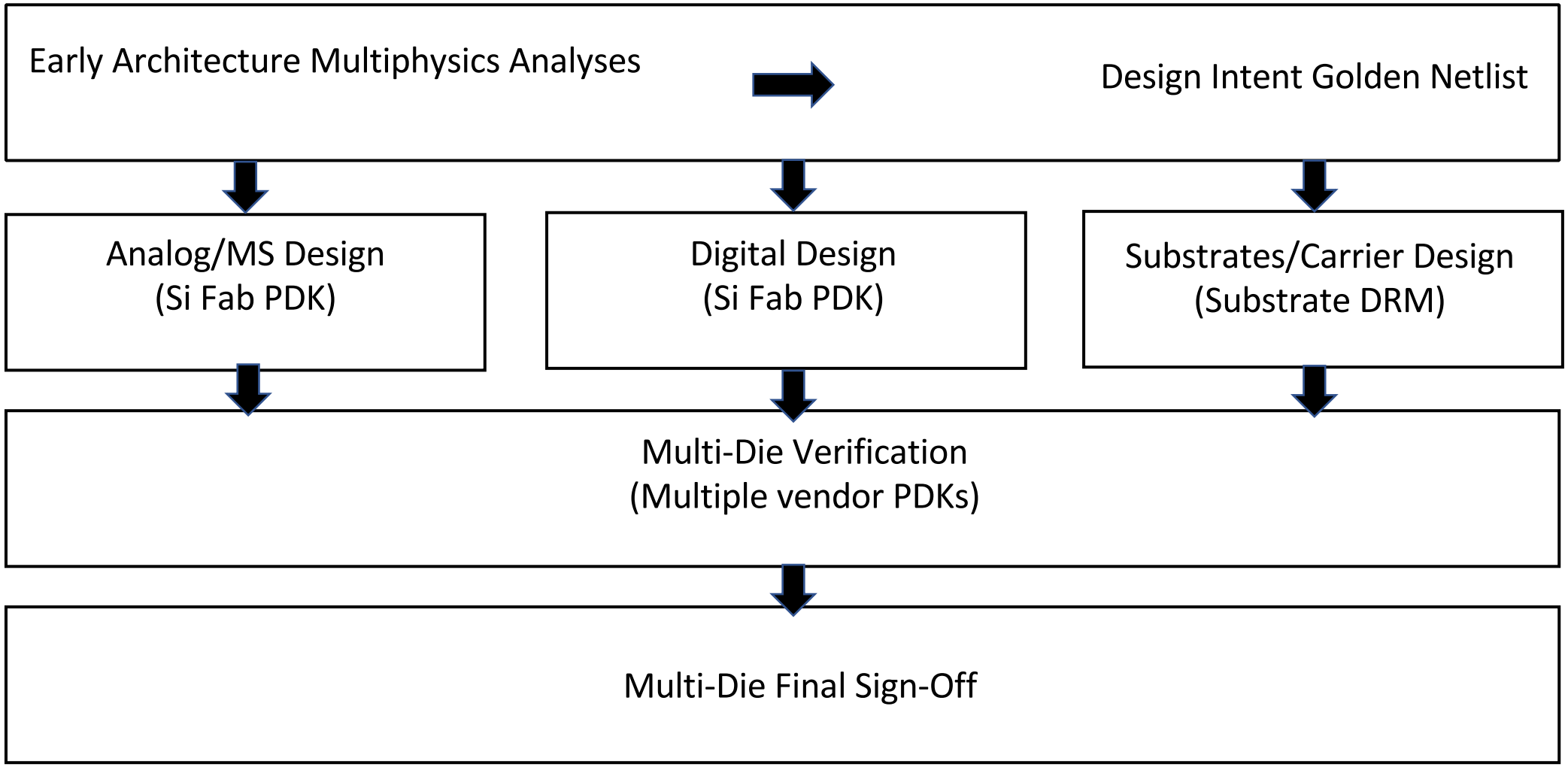
Chiplet stacking by zGlue


Manufacturing
Chip Design Kits
System Design Kits
Design Automation
Chip Design
System Design

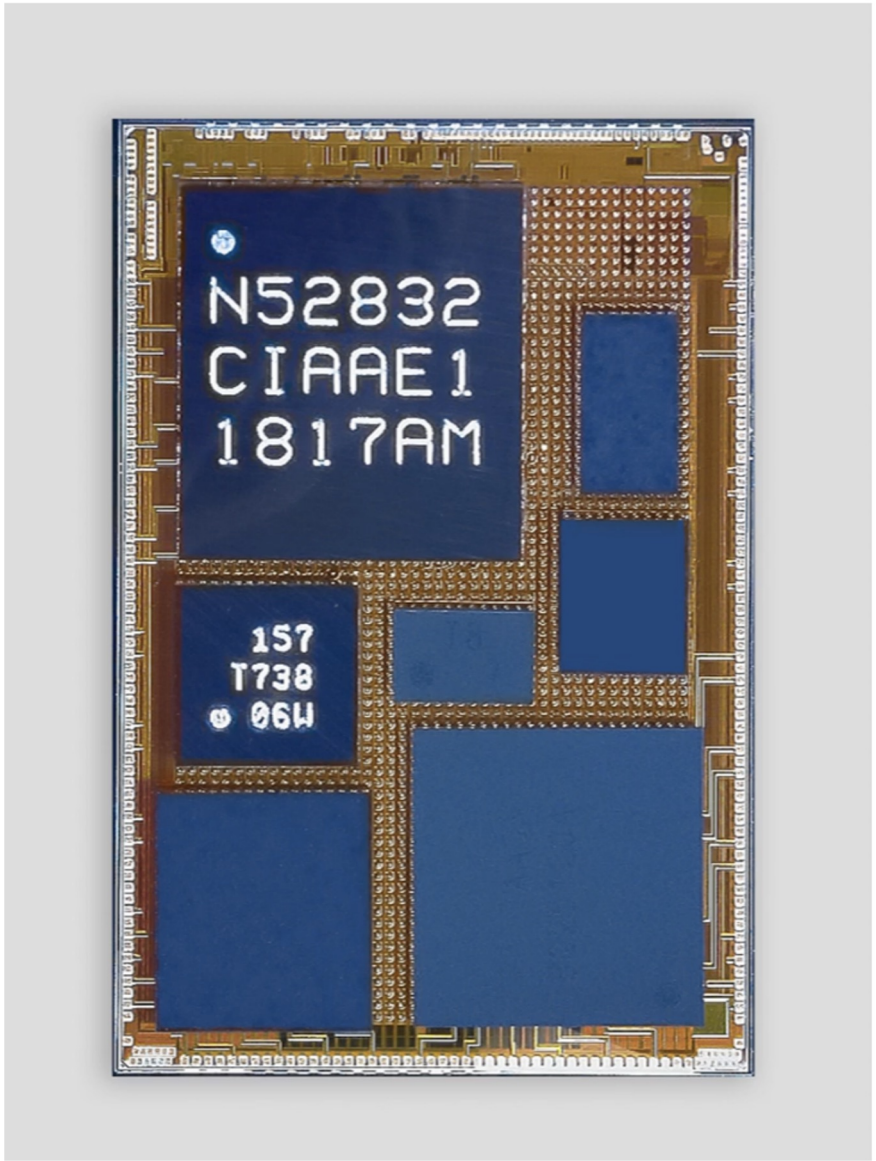
Complex chiplet manufacturing flow

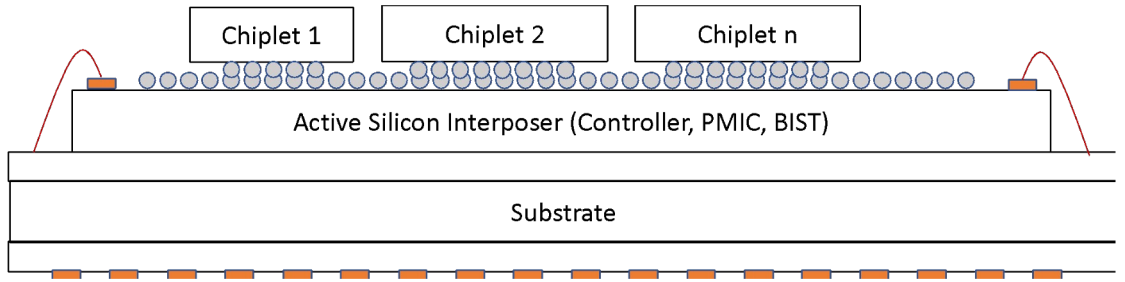


Chiplet Integration Workflow

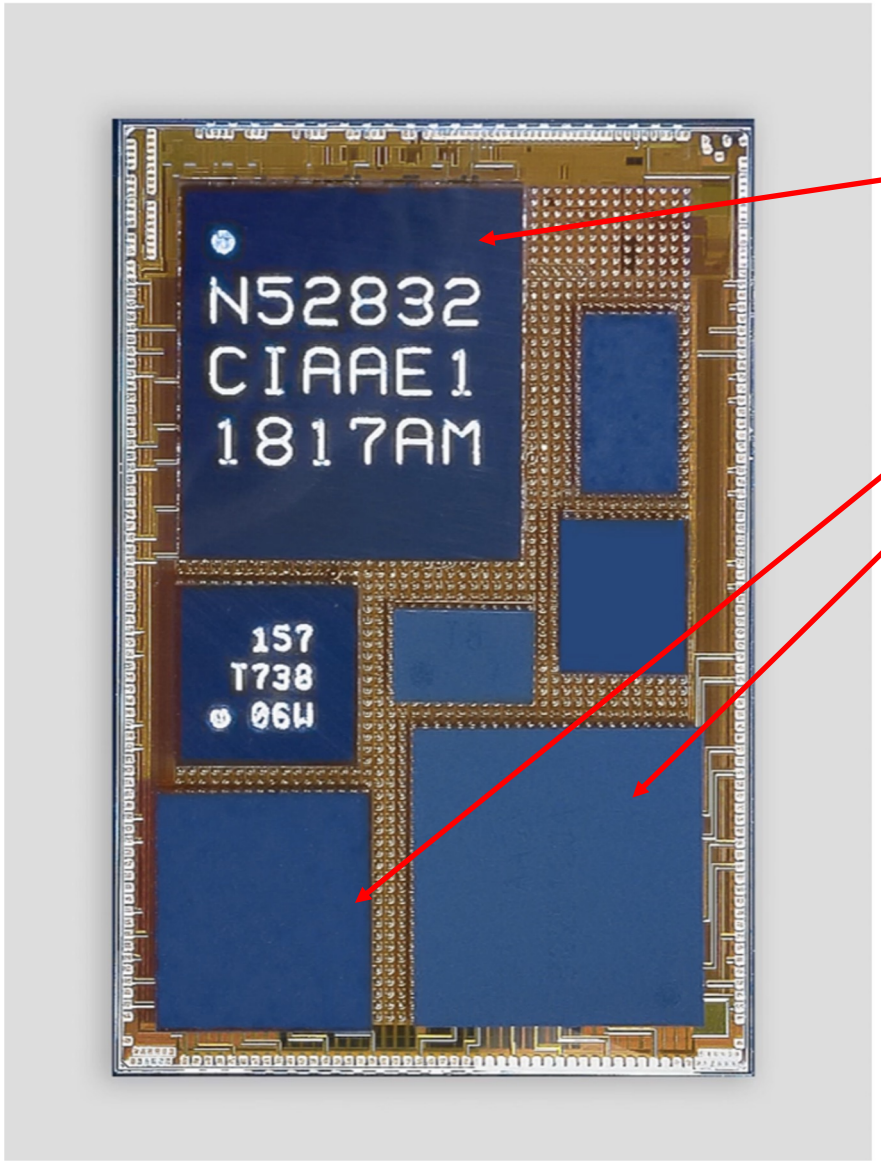


zGlue 3D-IC


N52832
CIAAE1
1817AM
157
T738
06W


Chiplet 1
Chiplet 2
Chiplet n
Active Silicon Interposer (Controller, PMIC, BIST)
Substrate

zGlue 3D-IC

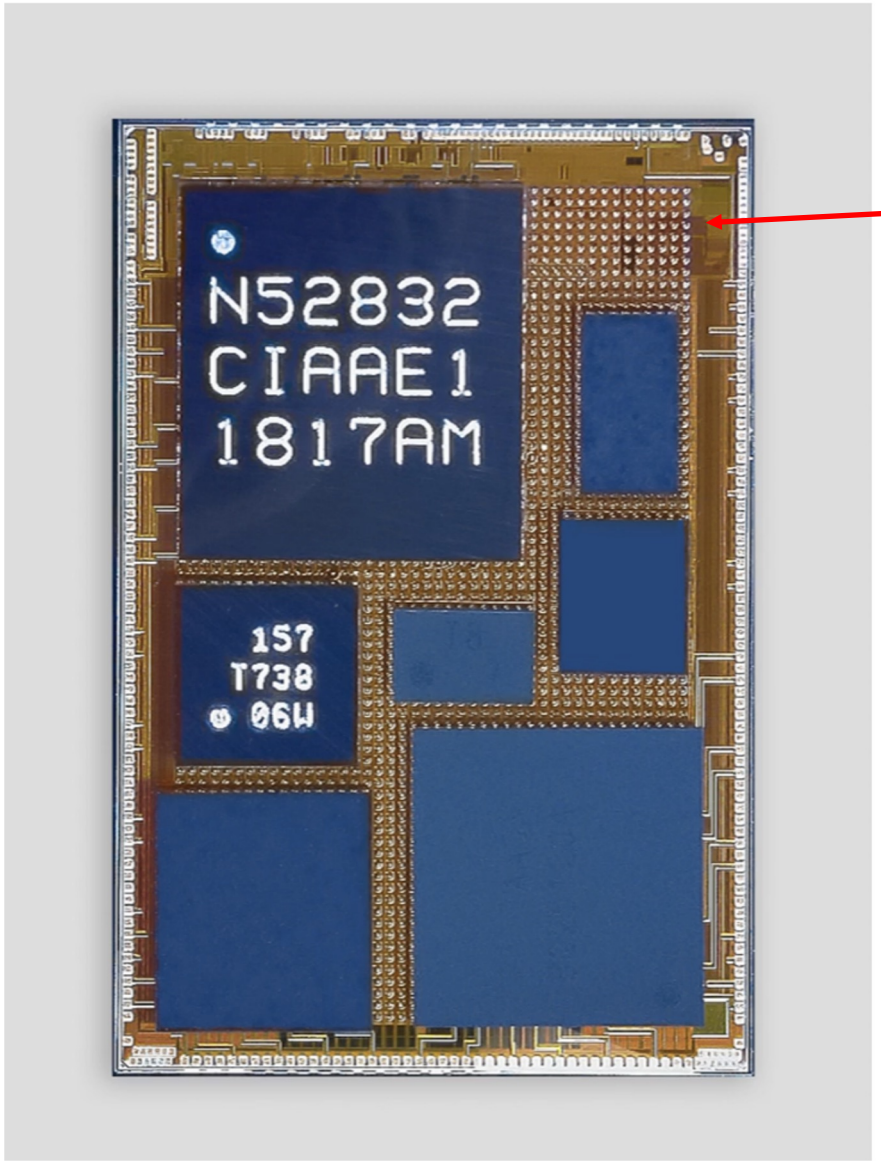


Leading node Si Fab + Bumping

Foundry PDKs, Bumping PDK

ICC/Virtuoso/Calibre (Si Design Tool Chain)

zGlue 3D-IC

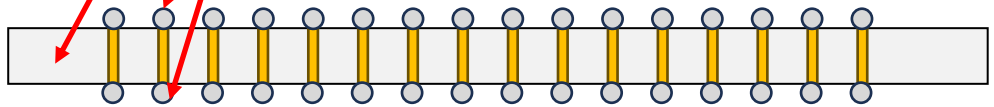


Interposer/Base Die Si Fab + TSV+ Front/Back RDL Bumping

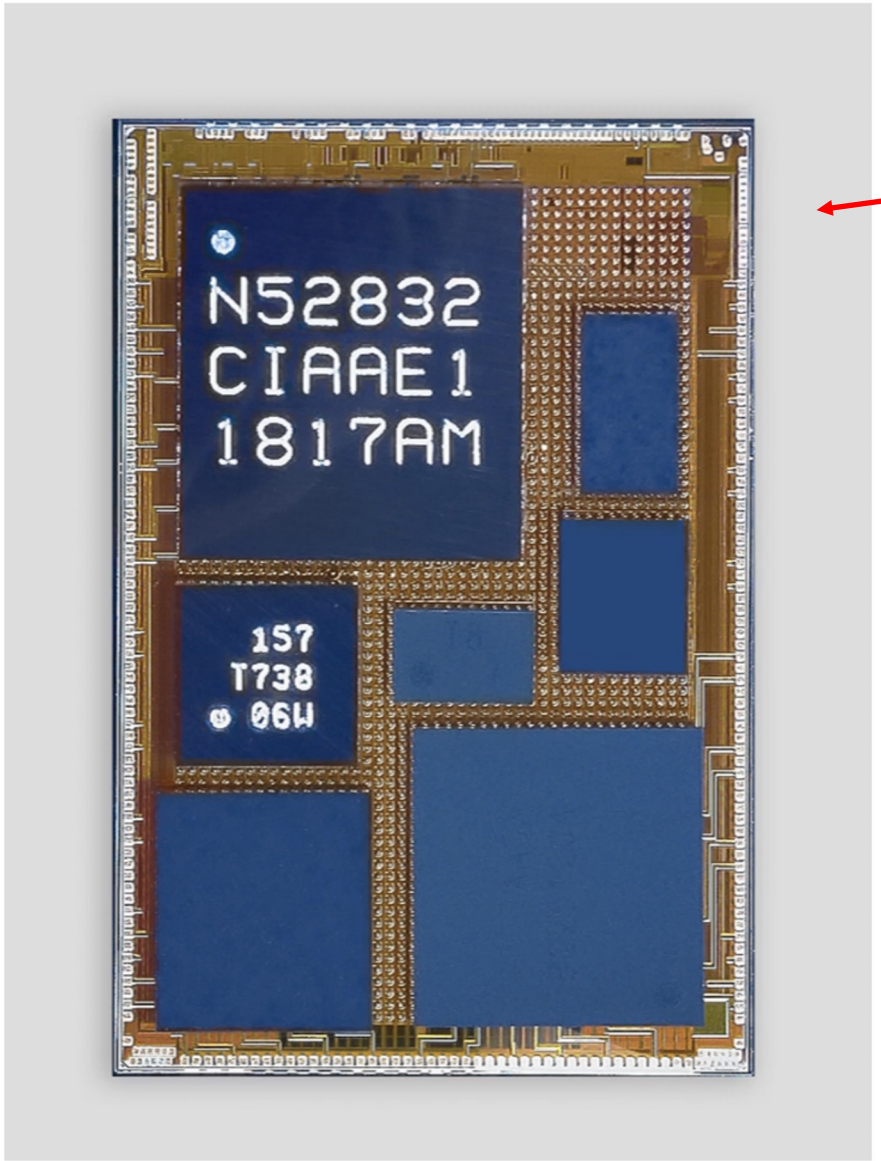
Si Fab PDK

MEOL FS/BS Bumping PDK

Virtuoso, ICC (Si Design Tool Chain)



zGlue 3D-IC

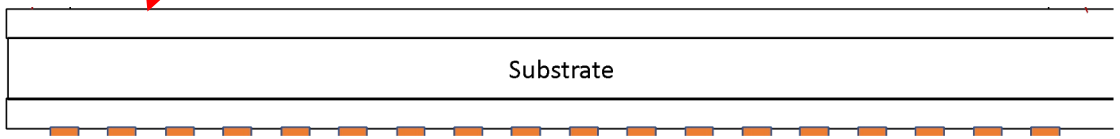


Substrate Fab

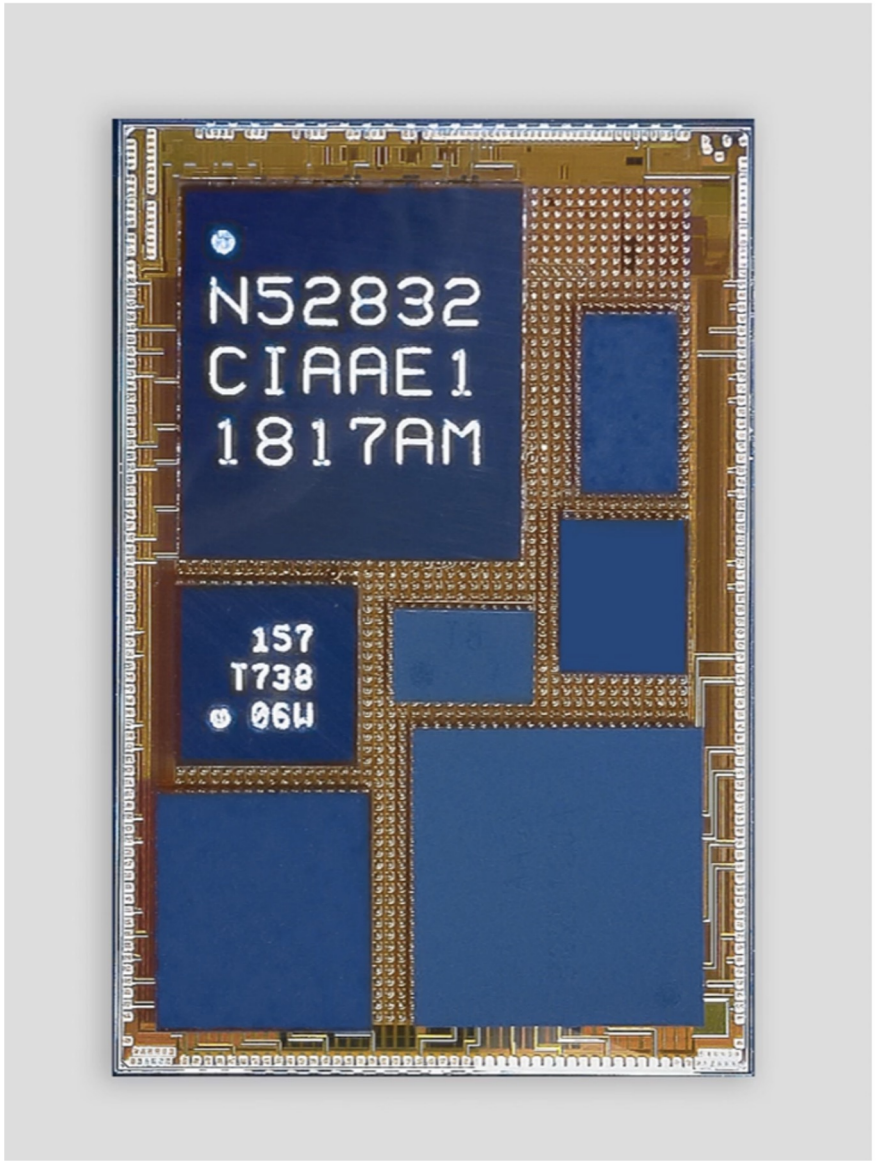
Substrate Design DRM

Allegro/Xpedition (PCB tools repurposed)

Calibre/Assura don’t check DRC on substrate design databases. You can convert to GDS and check there.



zGlue 3D-IC



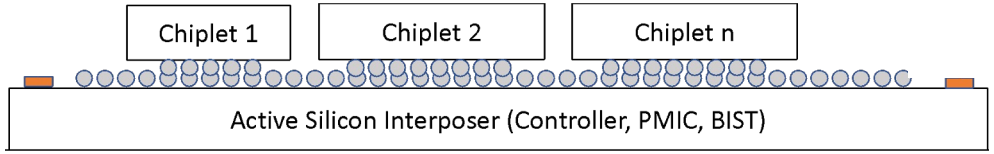
Assembly Step#1

Chiplet on interposer/base-die wafer

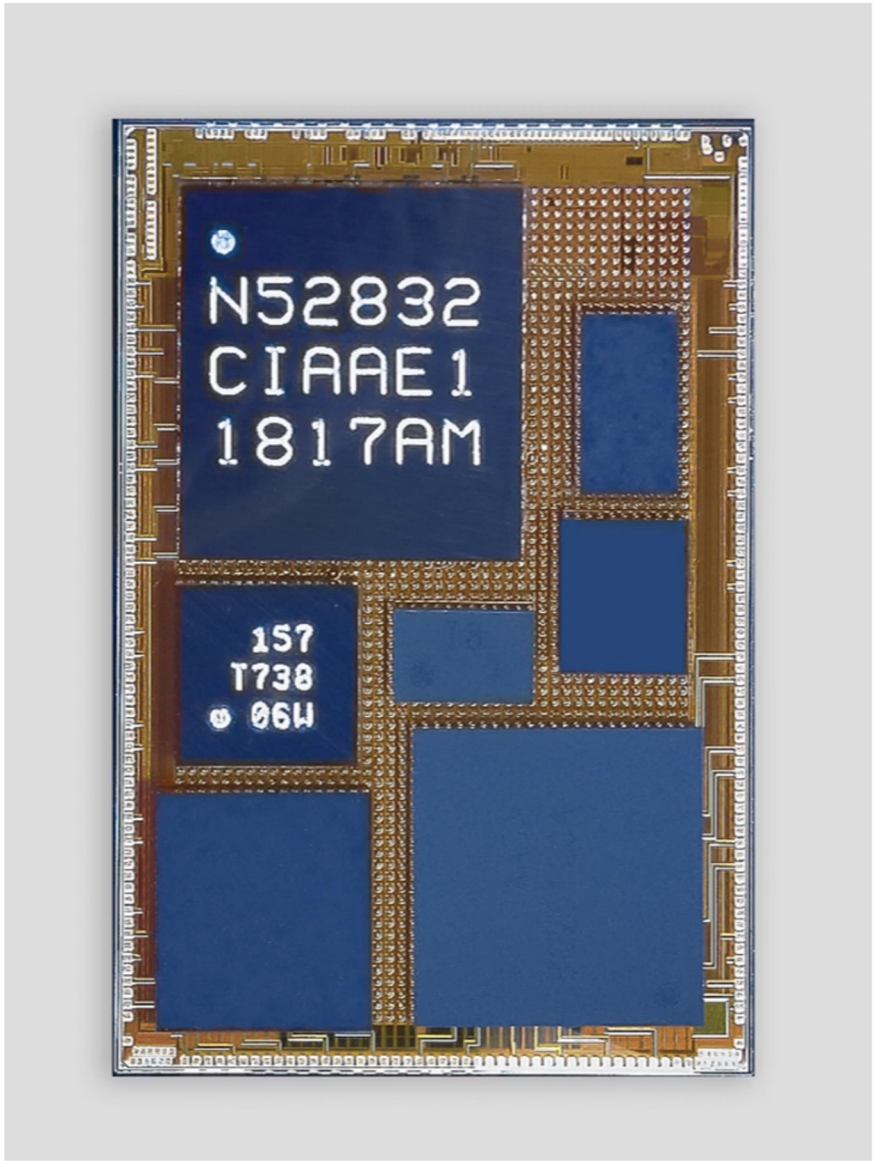
1- Inter-die spacing for underfill application

2- Die to edge spacing

3- Fully custom design and manufacturing



zGlue 3D-IC



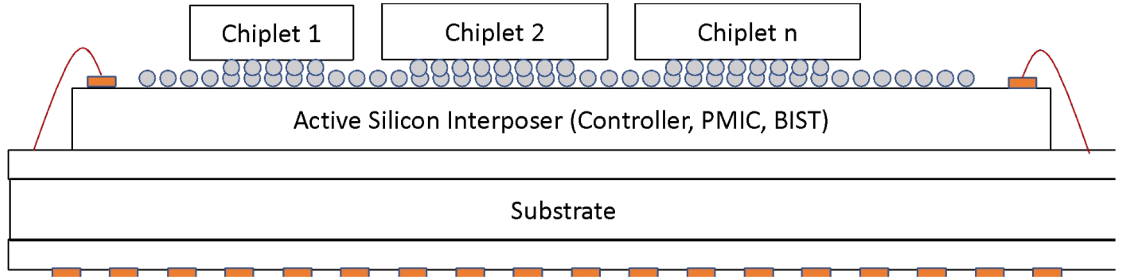
Assembly Step#2

Chiplet on interposer/base-die on the substrate

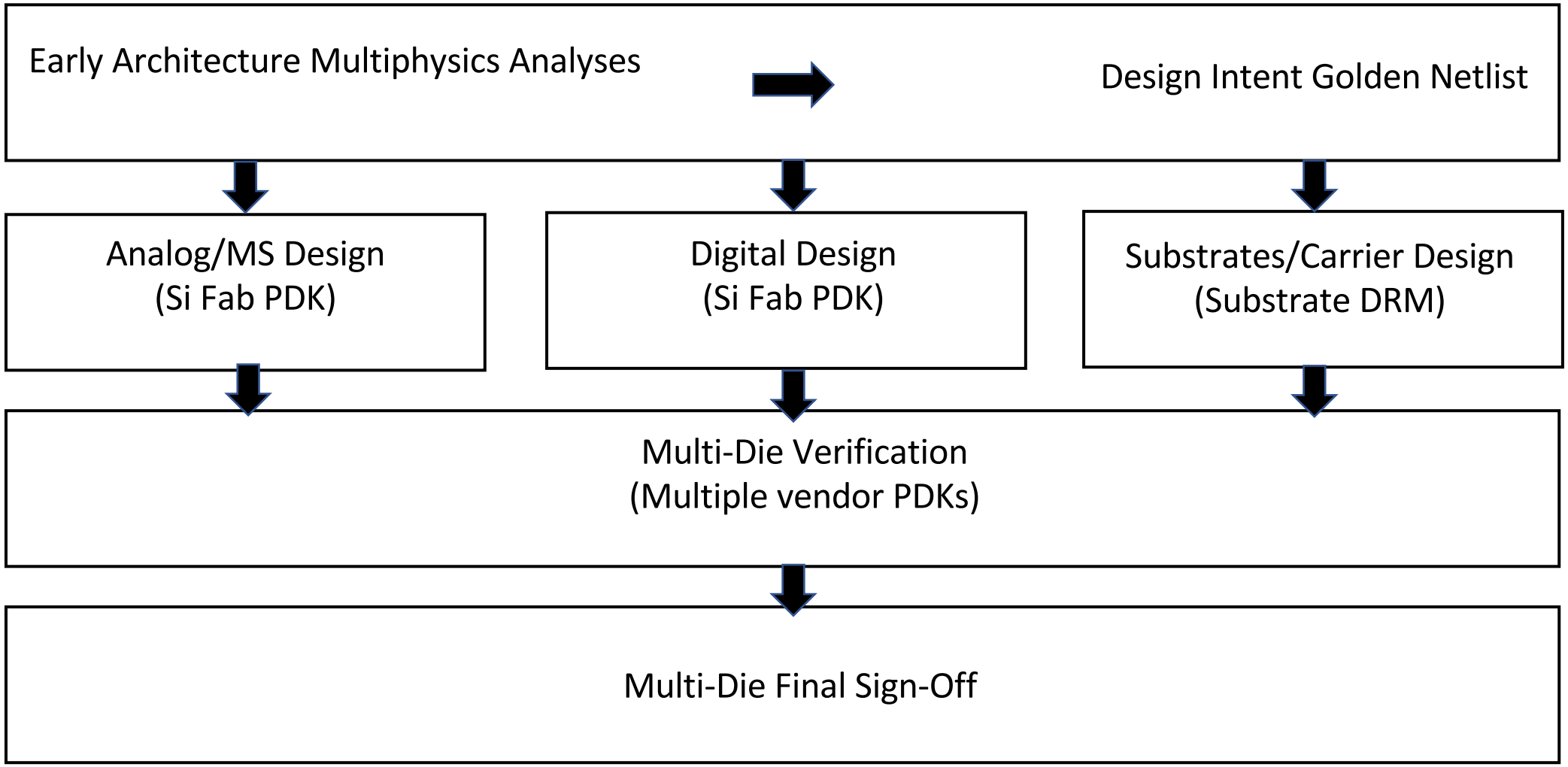
1- Stack-stack, Die-stack spacing

2- Die to edge spacing

3- Fully custom design and manufacturing



Chiplet Integration Workflow



Package Assembly Design Kit

Chiplet	• Bumping Rulesets • TSV Rulesets
Interposer	• TSV Rulesets • Front/Back RDL Bumping Rulesets
Substrate	• Design Rule Manual (pain point) • Stack-up
Assembly	• Inter die/stack spacing • Placement • Stack-up
Test	• Probe pad design rules

3D IC design kits (3DK) by ODSA/CDX

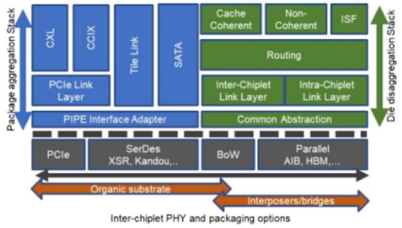
Open chiplet economy

Acknowledgement: Work by volunteers of ODSA/CDX Workstream
James Wong, David Ratchkov, Anthony Mastroianni, Jawad Nasrullah

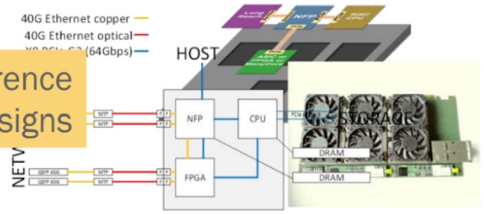
Facilitating a Chiplet Ecosystem

ODSA Charter

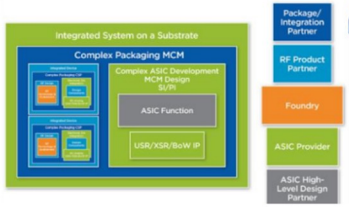
Open D2D Interface



Reference Designs

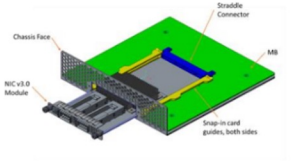


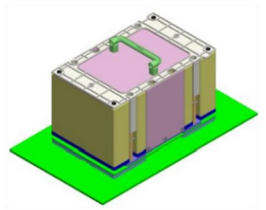
Reference Workflows

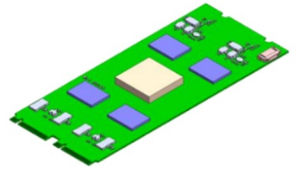


Integrate best in class chiplets from multiple vendors

Chiplet Marketplace







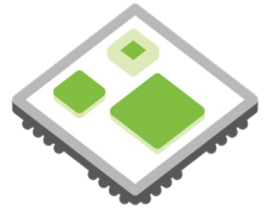
Open. Together.

OPEN Compute Project

[HIR Workshop & Symposium SEMI February, 2020 "Rise of Chiplets" Part 1]

Open Possibilities.

Chiplet Design Exchange (CDX)



OPEN DOMAIN SPECIFIC ARCHITECTURE

- Charter: Recommend standardized chiplet **models,** workflows and ecosystem
- Members: EDA, chiplet Providers, Assemblers & Integrators
- Recent Activities
  - Chiplet Design Kit Whitepaper (November 2021)
  - JEP30/CDXML chiplet part model (January 2023)
  - 3D IC Whitepaper (WIP)
  - 3DK Initiative (New)

Open Possibilities.

CDXML format (in collaboration with JEDEC JEP30)

CDXML is a format contribute to OCP by the CDX member
https://github.com/opencomputeproject/ODSA-CDXML

CDXML is filling the gaps in standardization

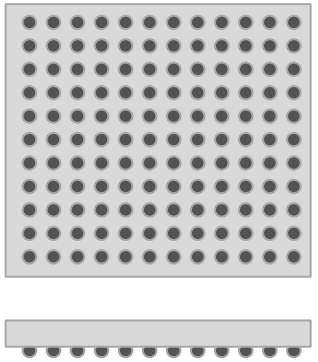
OCP and JEDEC have signed a collaboration agreement

- Enhance JEP30 (Part Model) with chiplet level data from CDXML
- Bring CDXML in line with JEP30 definitions

CDXML presentation from Global Summit 2022
https://www.youtube.com/watch?v=ed9BJDwZUtY

Open Possibilities.

CDXML format



CDXML contains the following information:

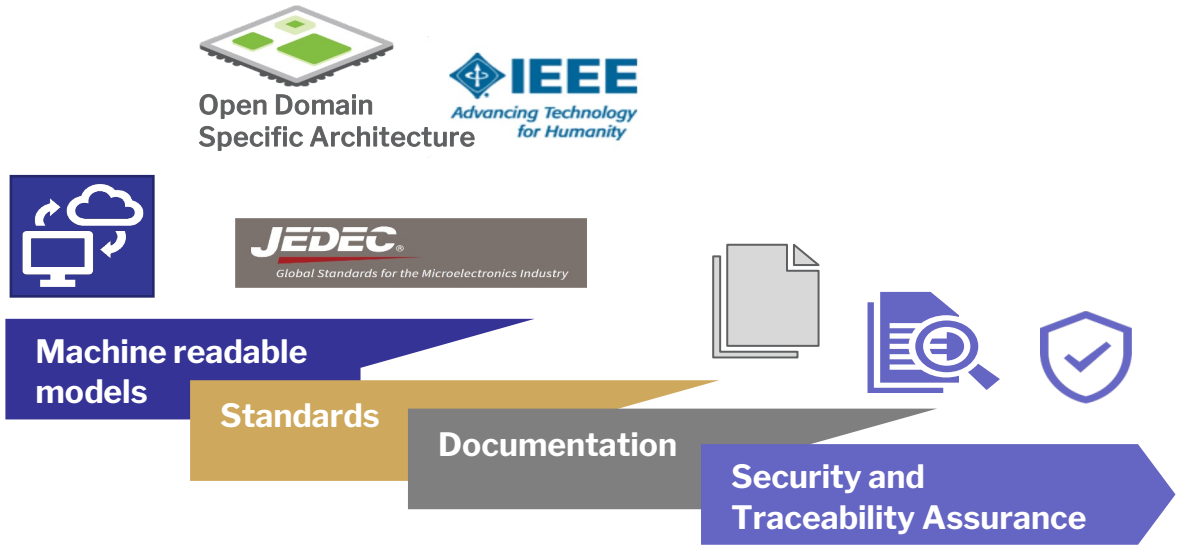
- Common data exchange format between the chiplets
- Standard data structure with XML schema
- D2D interfaces information
- Mechanical information
- IO information
- Electrical information
- Power and thermal information
- Chiplet integration

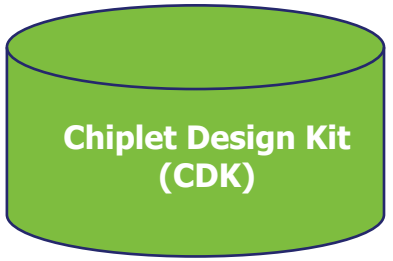
Being Developed at CDX Workstream of ODSA in Collaboration with JEDEC.

Chiplet Design Kit(CDK)

Recommended chiplet models to support 3DIC integration

- Leverage existing standards
- Drive new standards where required
- Machine readable models
- EDA tool/vendor neutral standards/formats
- Supported workflows
- Drive Ecosystem support
  - EDA Vendors
  - Fabs, substrate vendors, OSATs
  - Commercial and government 3D IC design community





Open Possibilities.

Chiplet Design Kits (CDKs)

Model	Description
Thermal	• ECXML – JEDEC JEP181
Physical & Mechanical	• Library Exchange Format (LEF) • GDSII or OASIS • JEDEC JEP30-P101/CDXML
Electrical/IO	• JEDEC JEP30-E101/CDXML
Behavioral	• SystemVerilog IEEE – 1800-2017 • Recommended: Verilog-AMS 2.4 • Optional: SystemC IEEE – 1666-2011 • Optional: Bus Functional Model (BFM)
Power	• Liberty (.LIB) • IEEE2416 Standard for Power Modeling • Optional: UPF – IEEE 1801-2018 or CPF • Optional: Verilog-AMS 2.4 • Optional: SystemC IEEE – 1666-2011
SI Analysis	• IBIS/IBIS AMI • Optional: Spice netlist (IO driver/receiver) • Optional: Channel model

Model	Description
PI Analysis	• Chip Power Model (CPM)
Static Timing Analysis	•Chiplet (.LIB)
Test	• BSDL – IEEE 1149.1/1149.6/1149.7 • ATPG model - Primitive/UDP based Verilog • Recommended: Internal JTAG (IJTAG) IEEE 1687 • Optional: IEEE-1500 Core Test Language (CTL) • Recommended: Gray-box level netlist • ATPG vectors - STIL (IEEE1450.1) or WGL • MBIST/repair vectors - STIL (IEEE1450.1) or WGL • Optional: UPF – IEEE 1801 or Chip Power Format • Optional: IP Firmware (if applicable)
Security	• Optional: Security Agent
Documentation and Guidelines	• General Chiplet Documentation • SiP Physical Integration guidelines • SiP Test guidelines • Optional: Firmware (if applicable) • Optional: Security

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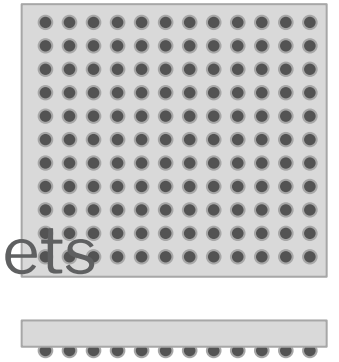

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Developed at CDX Workstream of ODSA in Collaboration with JEDEC

JEDEC JEP30 Part Model

JEDEC Publishes Major Update to JEP30 PartModel Guidelines

ARLINGTON, VA., USA – May 24, 2023 – JEDEC Solid State Technology Association, the global leader in the development of standards for the microelectronics industry, today announced significant updates to the JEP30 PartModel Guidelines, including all reference documents and related XML Schema files. JEP30 and its constituent documents are available for free download from the JEDEC website.

JEP30 establishes requirements for the frictionless digital exchange of part data between part manufacturers and their end customers responsible for electrical and electronic products creation. The JEP30 guidelines define a standardized format that can be efficiently consumed across different CAD tools and environments. By defining a common framework for part model creation and verification and helping to ensure different tools can accurately interpret and utilize the models created by the full spectrum of part manufacturers, JEP30 offers a transformative resource for both component manufacturers and designers.

The updated JEP30 part model guidelines can be used to define the digital twin of a part with the detail to enable significant process efficiencies throughout the part and product life cycles, including design, manufacturing, quality control, test, material declaration, and supply chain.

https://www.jedec.org/news/pressreleases/jedec-publishes-major-update-jep30-partmodel-guidelines

- Part Model extended to include chiplets
- Enables a chiplet marketplace
  - Chiplet providers publish part models
  - 3D IC integrators browse chiplet catalog
  - Delivery/procurement platform

Chiplet Providers

Chiplet Consumers

Open Possibilities.

3D IC Design Kits (3DK)

- CDKs include the design models for each chiplet in a 3D IC package
  - These can be generated by the chiplet design team for internal use
  - Or provided by third party chiplet vendors
- System on Chip (SoC) design enablement
  - SoC IP Libraries
  - Process Design Kits (PDKs)
- System in Package (SiP) design enablement requires a new set of design kits required to facilitate the design, verification, analysis and testing of 3D IC designs
- 3DK is a comprehensive set of proposed SiP design enablement kits

US Government Call for Standardized Assembly Design Kits (ADKs)

- Advanced Packaging for DoD Applications (AP4DA) RFQ Element10:

  “Standardized Computer Aided Design (CAD) Assembly Design Kits (ADKs) for 2.5/3-D Packaging growing the domestic packaging ecosystem with a distinct focus on security, advanced heterogeneous integration (HI) design capabilities and system-level supply chain assurance with trusted traceability. “

- DARPA Next Generation Microelectronics Manufacturing (NGMM) RFI

  “The process modules should describe the design support required including EDA tools and the approach for developing, maintaining, and distributing 3D assembly design kits (3D-ADKs).”

3D IC Design Kits (3DK)

- Chiplet Design Kits (CDK)
- System on Chip (SOC) IP Libraries
- Process Design Kits (PDK)
- Package Assembly Design Kits (PADK)
- Material Design Kits (MDK)
- Package IP design Kits (PIK)

Open Possibilities.

System on Chip (SOC) IP Libraries Required for 3D IC design

- Chip to Chip (C2C) & Die to Die (D2D) IP Models
  - Front End Models: LEF, .LIB, System Verilog (SV)
  - Verification IP
    - Generic Models (SV)
    - Connectivity creation/validation
    - Functional testbench/validation
    - Technology Mapping (generic to vendor/technology IP)
- Facilitate 3D IC Architectural Exploration/Analysis
  - Identify Key internal and external high-speed interfaces
    - External Chip-to-Chip (C2C) Interfaces
    - Internal Die-to-Die (D2D) Interfaces
  - Validate interface connectivity/functionality
  - Assess/map technology/vendor specific connectivity IP

Process Design Kits (PDKs)

- IC (Silicon/Type III-V Foundry)
  - Technology files:
    - DRC, LVS, DFM, PEX rules/decks
  - Circuit Design Kits:
    - Schematic Driven Layout macros to support Analog & Memory macro design
- Silicon Interposer (Silicon Foundry)
  - Interposer Technology files: DRC, LVS, DFM, PEX
- Organic Substrates (OSAT/Substrate Vendor)
  - Technology rules (PDF): Design Rule Manual (DRM), Material (see MDK)
  - Technology decks: DRC, LVS, DFM, PEX rules/decks

Package Assembly Design Kits (PADK)

- New open, collaborative format to support 3D IC:
  - Package planning
    - Chiplet bump rules
    - 3D IC stack-up
  - Package Design
    - Assembly Design rules
    - Package component placement rules
  - Wafer test support
    - Probe pad planning
- Support other formats through scripts/mapping tools
  - 3Dblox, CDXML/JEDEC, ….
- Open access during format development
- Controlled access after adoption of standard bodies

Open Possibilities.

Material Design Kits (MDK)

New open, collaborative format to define material properties to support 3D IC Design Analysis

- Package components
  - Substrates, interposers, PCB, heat sinks/TIM, …
- Electrical Properties
  - DK, DF, Dielectric, Surface Roughness
- Thermo-mechanical stress
  - Thermal conductivity
  - Thermal expansion coefficients
  - Young's Modulus
- Leverage CDXML materials format
- Open access during format development
- Controlled access after adoption of standard bodies

Open Possibilities.

Package IP design Kits (PIK)

Define reusable package connectivity components

- Connectivity cells:
  - bump/ubump, C4, TSV, HB, …
- Physical Models
  - LEF, GDS, CDXML, 3DBLOX
- Electrical Models
  - RLC PEX, ERC, ESD, …
- Schematic Symbols
- Parameterized macros
  - Power/Ground macros, High speed, high power, …

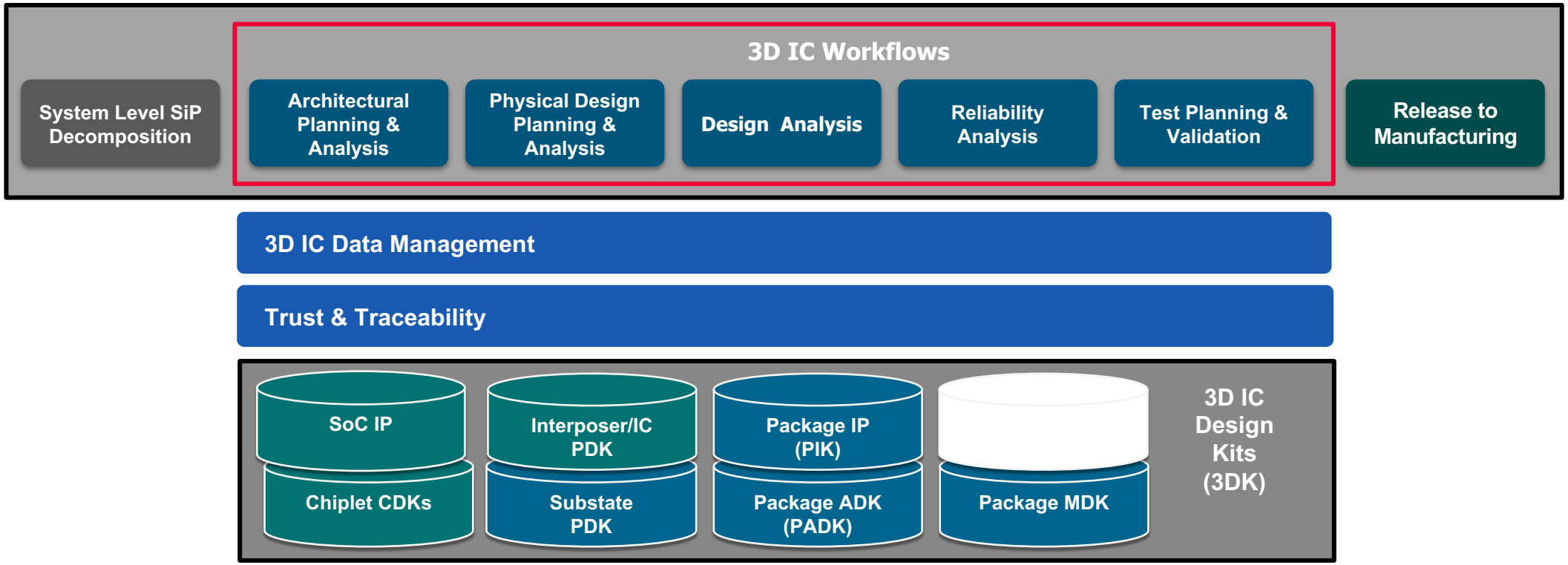
Open Possibilities.

3DK Status

Design Kit	Status	Proposed Action
SOC IP Libraries (Foundation/CTC)	Mature	Continue to adopt
SOC IP Libraries (DTD)	New, WIP	Adopt std SOC PDK model
Chiplet Design Kits (CDK)	Active JEDEC Adoption	Adopt
PDK: IC (Silicon/Type II-V)	Mature	Continue to adopt
PDK: Silicon Interposer	In production	Continue to adopt
PDK: Organic Substrate/interposer	New proposal	**Promote adoption of new PADK format**
PADK: Package Assembly Design Kit	New, WIP	**Active CDX working group**
ADK: Assembly rules decks	Mature custom	EDA adoption/support of ADK format
Package IP design Kits (PIK)	New proposal	**Promote, exemplar prototype**
Material Design Kits (MDK)	New proposal	**Active CDX working group**

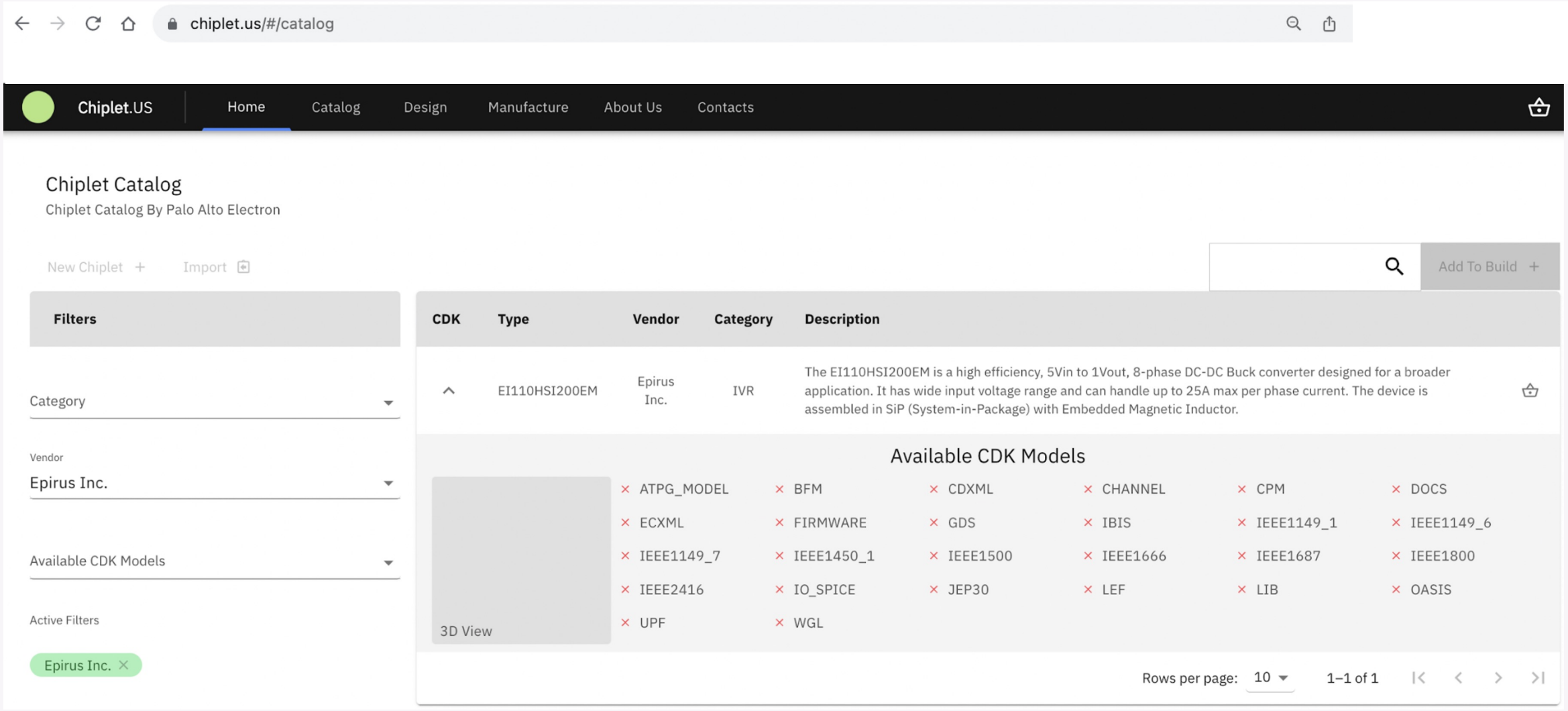
Summary

Broad adoption of chiplet based designs requires standardization of chiplet models, D2D Interface standards and 3D IC Design Kits (3DK)

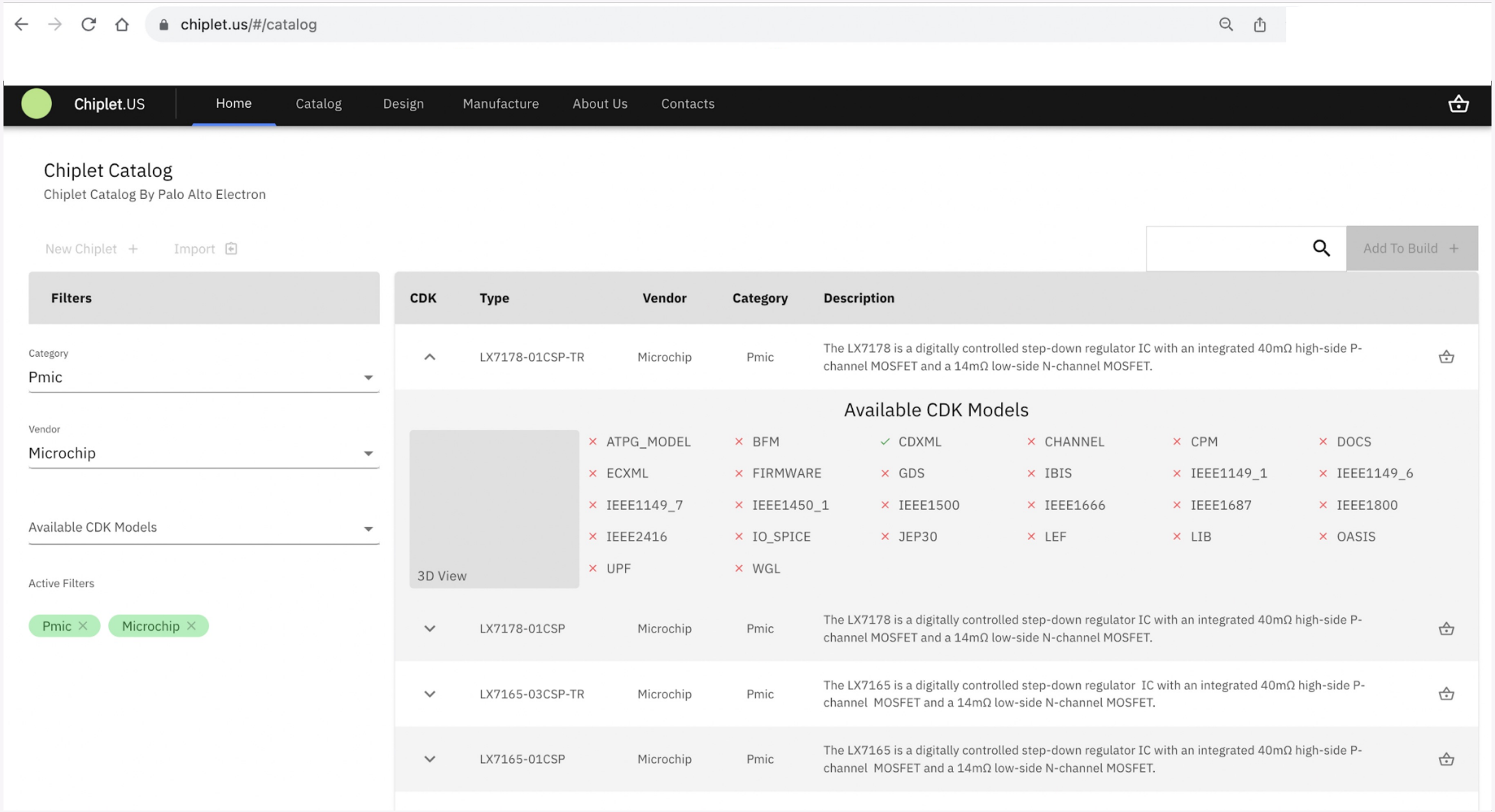


Open Possibilities.

Chiplet Catalog



Chiplet Catalog



Call to Action

Checkout our CDX whitepapers and CDXML formats

IEEE 3DIC 2021: November 15-18, 2021

https://ieeexplore.ieee.org/document/9687611

OCP: September 17, 2022

https://www.opencompute.org/documents/ocp-odsa-cdx-proposed-standardization-of-chiplet-models-for-heterogeneous-integration-2-pdf

OCP Global Summit: Oct 18-20, 2022

https://drive.google.com/file/d/1EEwYuEAECPM5Btu4_9Znder-RD4X_Dx-/view

Please join us:

- CDX weekly Meeting on on Thursday at 10:00 AM Pacific
- CDX biweekly 3DK Meeting on Thursday at noon Pacific
- CDX biweekly MDK meeting on Thursday at noon Pacific (alternate weeks)
- Contact David Ratchkov: david.ratchkov@thracesystems.com

Open Possibilities.

Thank You