Model-Based System Design for Chiplet-Based Architectures

Denis Dutoit – CEA List
Program Manager – Advanced Computing

cea list

Outline

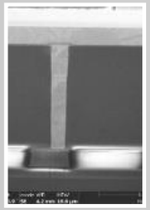
- Advanced packaging and demonstrators at CEA
- Chiplet platform for AI at Edge
- System-of-chiplets for Automotive
- Model-based system design

Advanced packaging and demonstrators at CEA

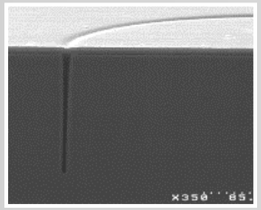
A complete tool box …

CEA tool box

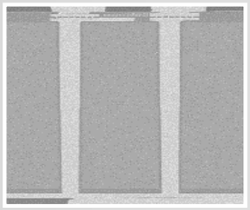
TSV
Through Silicon vias



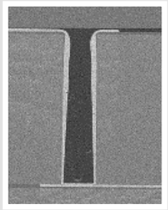
TSV HD Ø1x10µm



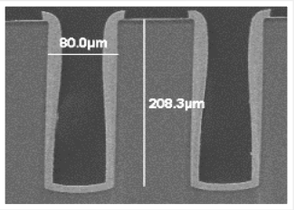
TSV / Trench first AR30



TSV mid AR10

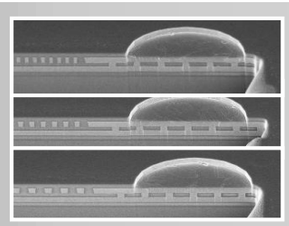


TSV last AR 0,5 → 5

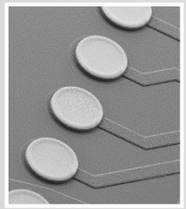


TSV last power (thick Cu-liner)

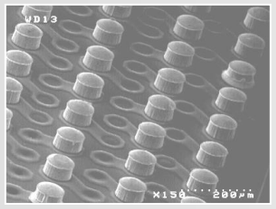
Routing

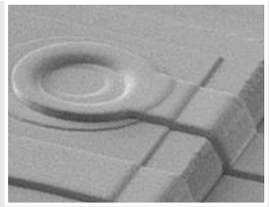


Front-side Cu damascene



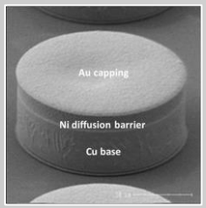
Back-side RDL co-integration (Pitch 20µm) with UBM & BUMP



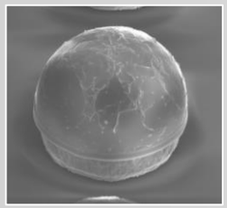


Cu conformal routing

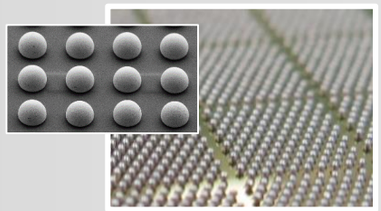
Connecting & Assembly



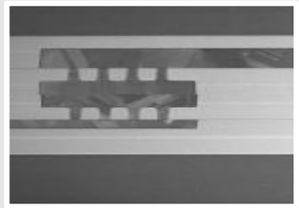
Copper pillars (Ø10µm)



Copper bumps (Ø10µm)

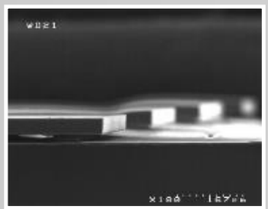


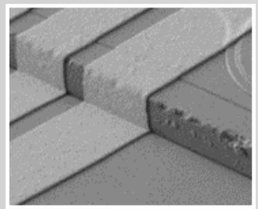
Bumping (Ø70µm) – Balling (Ø300µm)

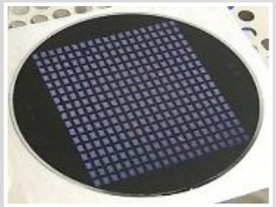


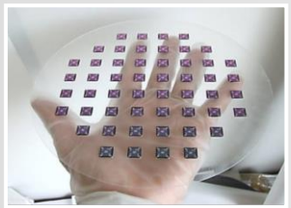
Hybrid bonding

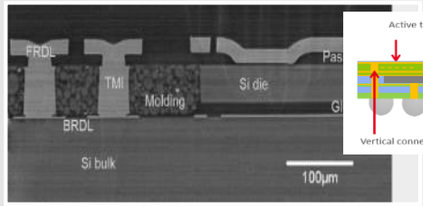
Rebuilt & thinning







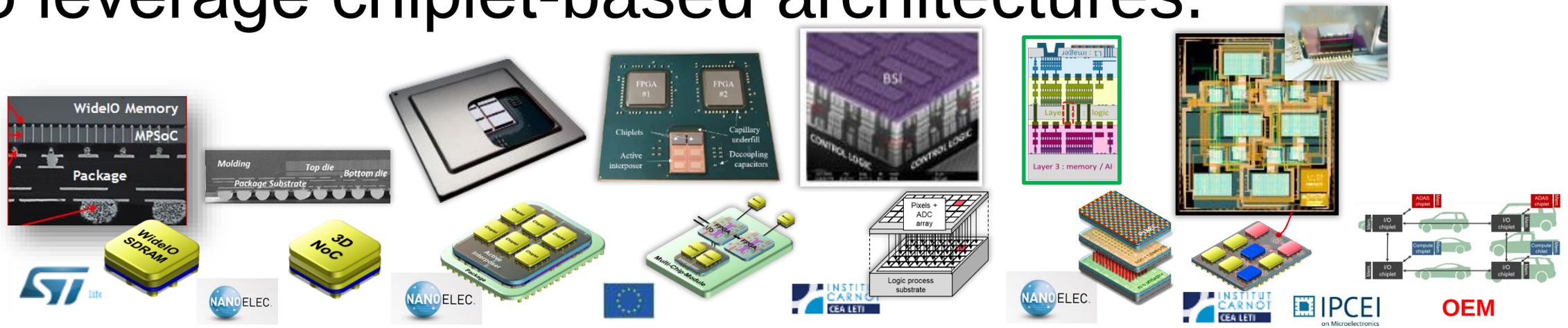




Si ultra thinning (20-30µm)

FO-WLP die first, RDL first, multi-strata, organic, silicon, glass substrates

… to leverage chiplet-based architectures.

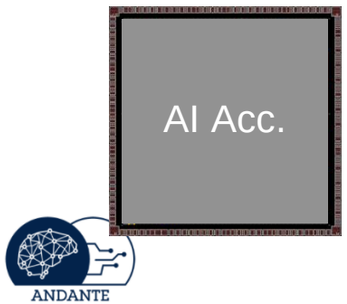


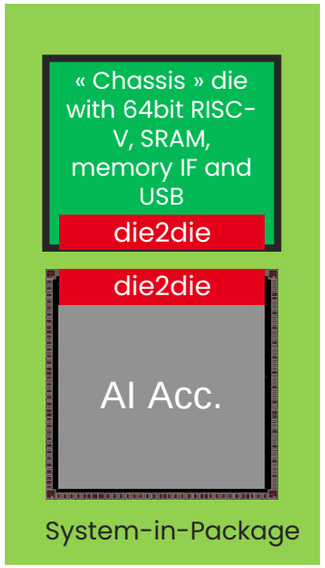
3D Circuit	WIOMING	3DNOC	INTACT	EXANODE	RETINE	SMART IMAGER	HUBEO-STARAC	THIS TALK
Application & Architecture	4G Telecom BB WIDEIO DRAM Memory-on-Logic	HPC 2 layer 3D NOC Logic-on-Logic	HPC: 96 Cores, 6 Chiplets on active interposer	HPC Heterogeneous chiplets, 2 chiplets, 1 active interposer, 2 FPGA	IMAGER 2 layer BSI, Distributed Pixel clusters on Logic	IMAGER 3 layer BSI, In Sensor AI engines	HPC: - 1Tb/s/mm2 link - 6 Chiplets on photonic NoC & interposer, E-O-E TX-RX chiplet	**AUTOMOTIVE: Model-based design, Heterogeneous chiplet, 1 I/O chiplet, 2 compute chiplets**
CMOS technology	DRAM + 65nm	65nm + 65 nm	FD28nm + 65nm	FD28nm + 65nm + FPGA	130nm	IMG + FD28 + FD28nm	100nm SOI SiPho, FDSOI28nm	**Heterogeneous**
3D Technology	TSV & Cu-pillar (40 µm pitch, F2B)	TSV & Cu-pillar (40 µm pitch, F2B)	TSV & Cu Pillar (20 µm pitch, F2F)	TSV & Cu Pillar (20 µm pitch, F2F) MCM	W2W, F2F, Hybrid Bonding	TSV 2 µm pitch, W2W2W, Hybrid Bonding	Cu-Pillar, TSV middle, Photonic + 3D integration	**System-In-Package, advanced substrate**
Status	Silicon [VLSI'2013]	Silicon [ISSCC'2016]	Silicon [ESSCIRC'2018] [ISSCC'2020]	Silicon [VLSI'2020]	Silicon [VLSI'2018]	On-going design [VLSI-TSA'2022]	Silicon [ISSCC'18] On-going fab' [DATE'2020]	**Concept [This Talk]**

Chiplet platform for AI at Edge

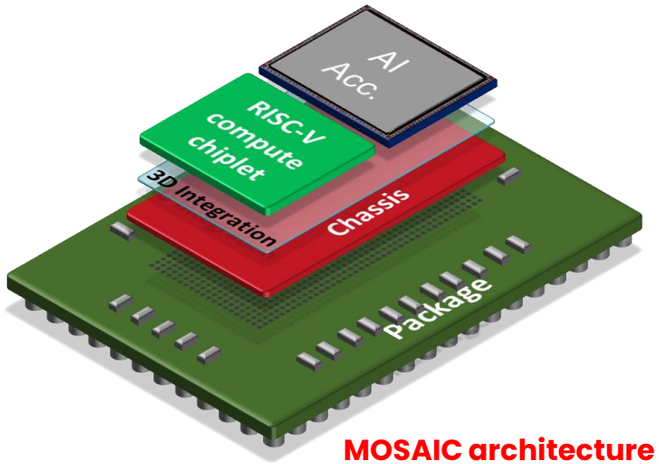
Chipletization roadmap at CEA for AI at Edge

Silicon validated | Design start | Under definition | *Status (beg. 2024)*





MOSAICS_LP



MOSAIC architecture

ASIC | SiP Chiplet | 3D Chiplet | *Integration scheme*

2023 | 2025 | > 2025 | *Chip availability*

MOSAICS-LP - A Scalable Chiplet Platform

Project & consortium

Visit us at booth 112

Edge computing chiplets platform requirements:

Chiplets re-use across products & customers

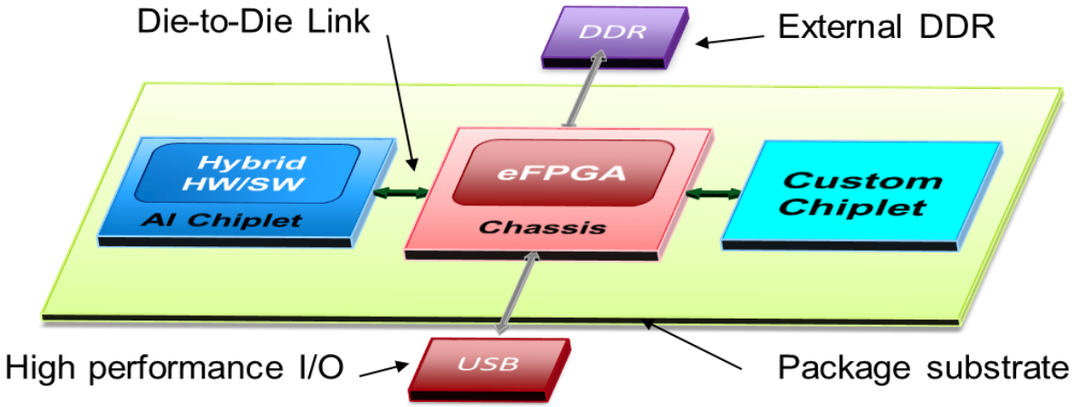
Low entry barrier to produce a chiplet

menta
Unlimited Power of Technology

- eFPGA IP technology
- Business model
- Ecosystem
- Sales & marketing
- Project lead

3 years project, with the support of **BPI France** and the **French government**.

Output: a ready to use **industrial platform** revolutionizing edge chips design (TRL 9)



cea list

- Heterogenous & modular architecture
- High performance digital circuits design
- AI chiplet demonstrator
- Experts in packaging & integration

A growing number of project Advisory Board members – Join us

Source: Anthony PHILIPPE & Yoan DUPRET

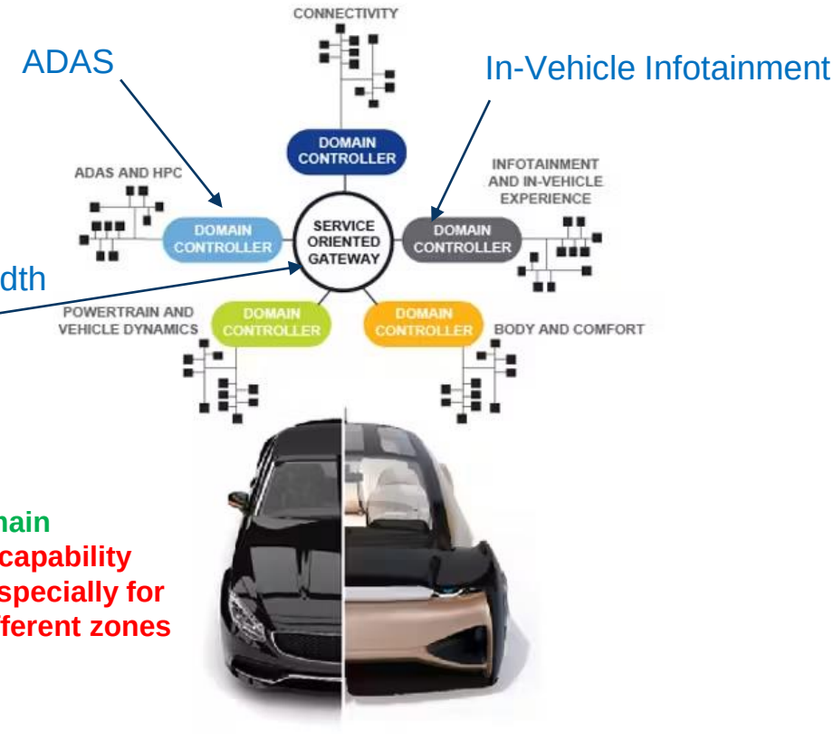
cea list

System-of-chiplets for Automotive

The auto architecture revolution: moving from domains to zones

Domain architecture

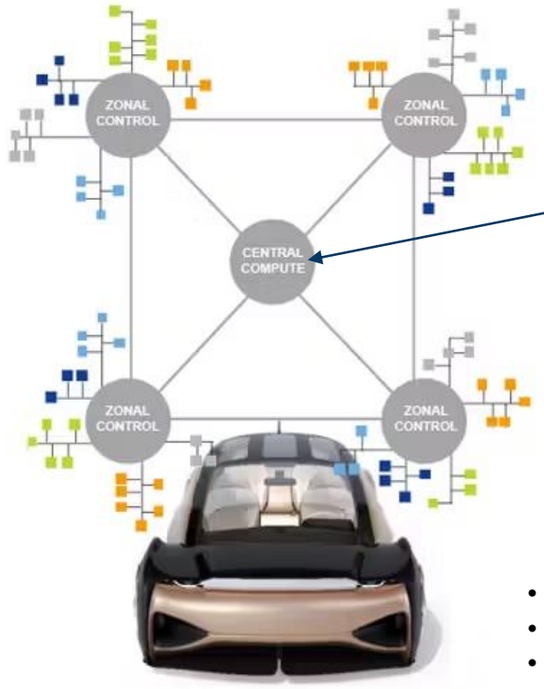
Systems are grouped by function



- **Scalable within domain**
- **Limited computing capability**
- **High cable length especially for data fusion from different zones**

Zonal architecture

Systems are grouped by physical location



ADAS
In-Vehicle Infotainment
High data bandwidth (for computing)

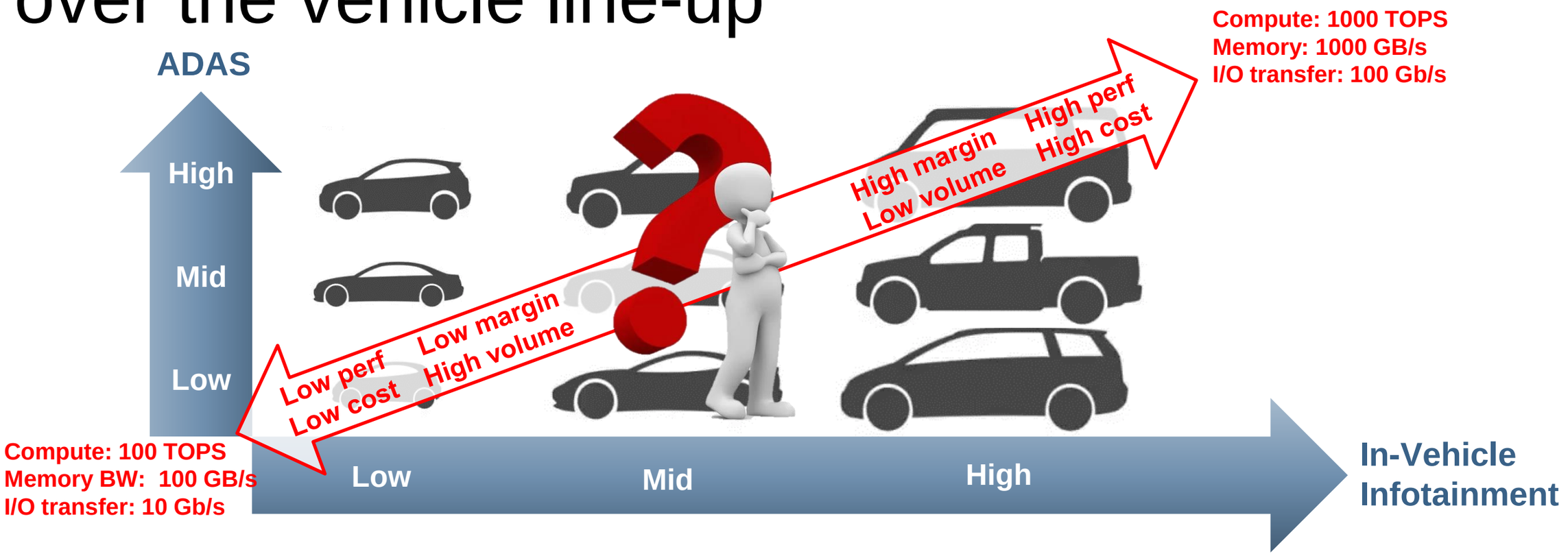
Server on wheels

- **Optimized for cable length reduction**
- **Optimized for advanced feature**
- **Optimized for data fusion from different zones**

Domain centralized computing → Domain level scalability → Vehicle level scalability → **Vehicle centralized computing**

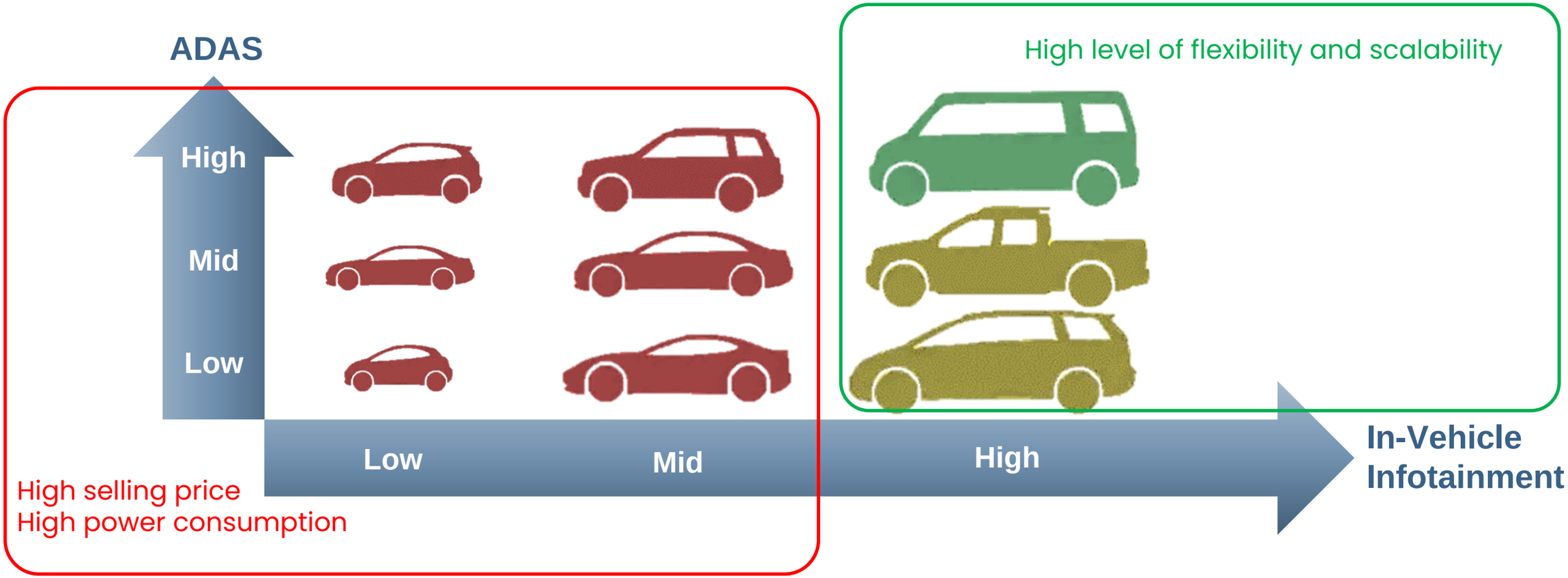
Pictures from: https://www.electronicdesign.com/markets/automotive/article/21242583/nxp-semiconductors-moving-from-domains-to-zones-the-auto-architecture-revolution

Vehicle level scalability: performance continuum over the vehicle line-up



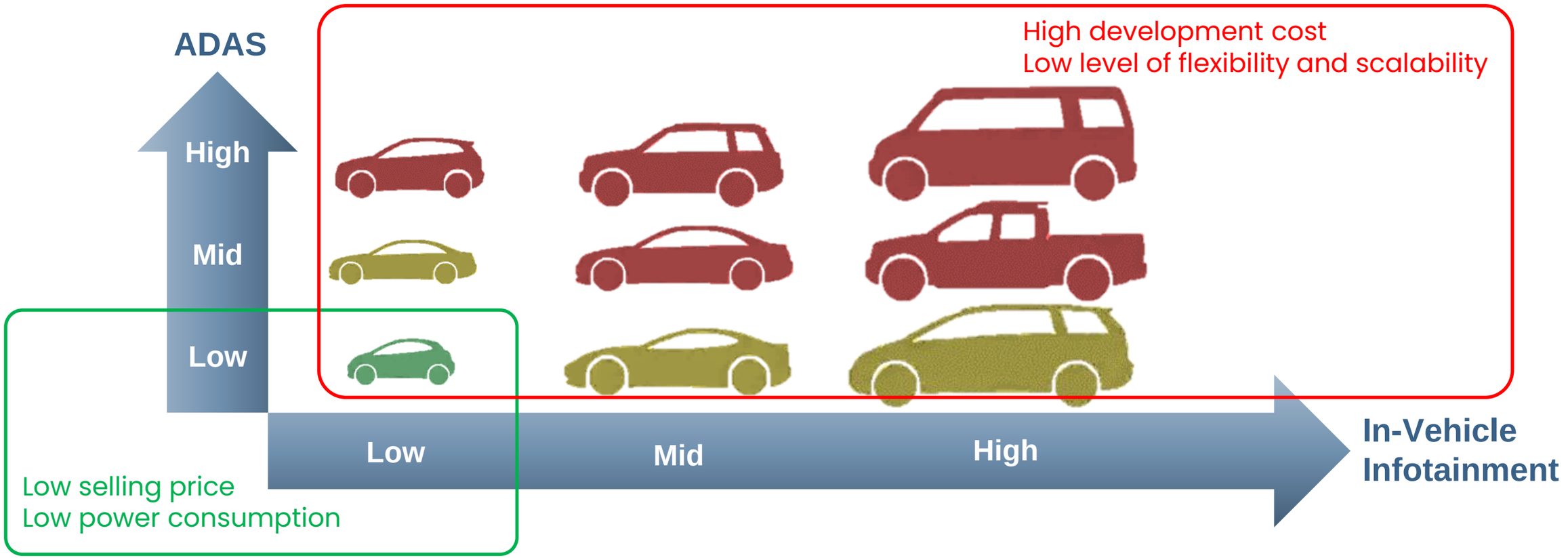
GPU solution

One chip covering all segments - software defined



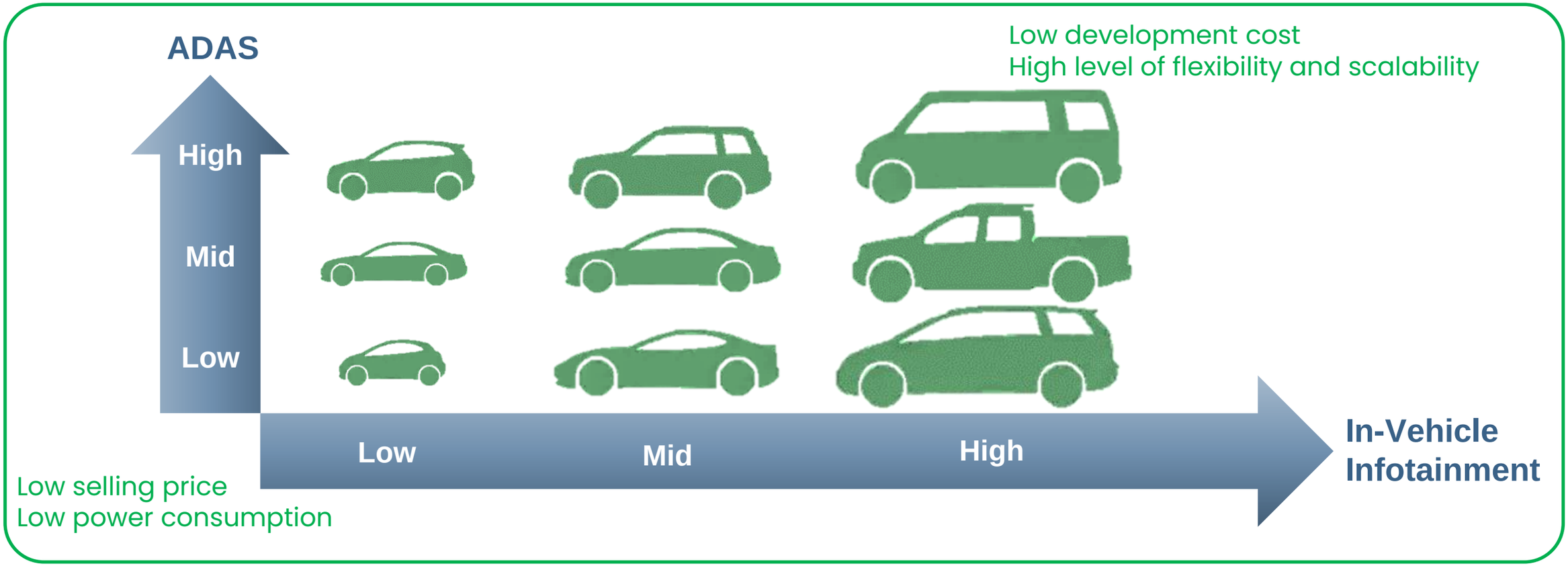
ASICs solution

One chip per segment - hardware defined



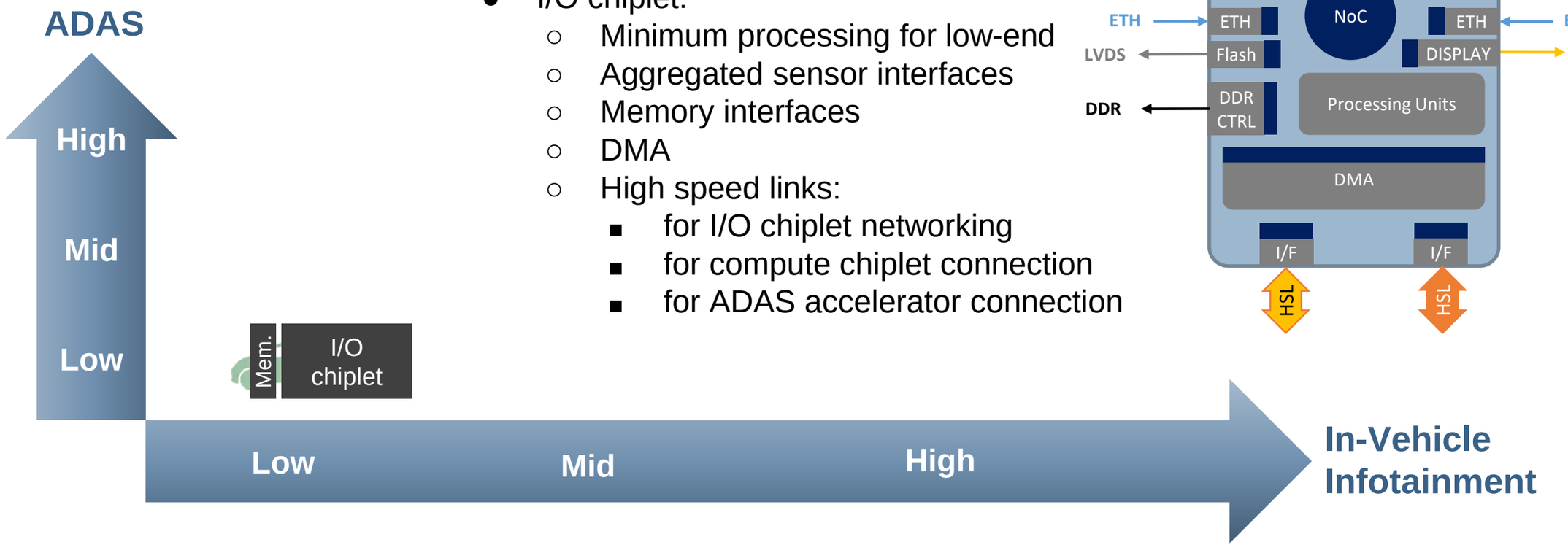
Chiplet solution

A few chiplets covering all segments – mix HW and SW defined



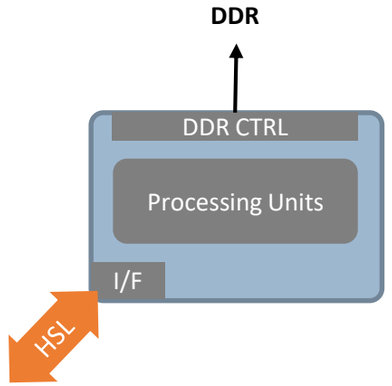
Chiplet Architecture: I/O chiplet

- I/O chiplet:
  - Minimum processing for low-end
  - Aggregated sensor interfaces
  - Memory interfaces
  - DMA
  - High speed links:
    - for I/O chiplet networking
    - for compute chiplet connection
    - for ADAS accelerator connection

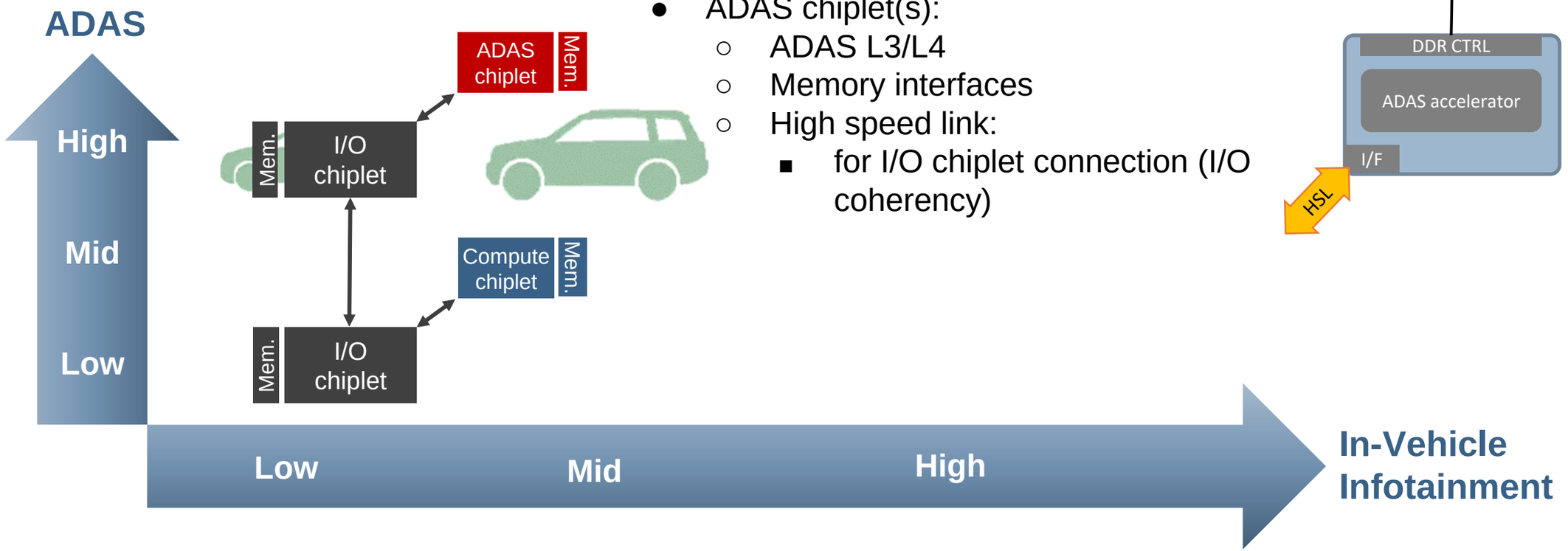


Chiplet Architecture: compute chiplet

- Compute chiplet:
  - Additional processing for mid-end
  - Memory interfaces
  - High speed link:
    - for I/O chiplet connection (full coherency)

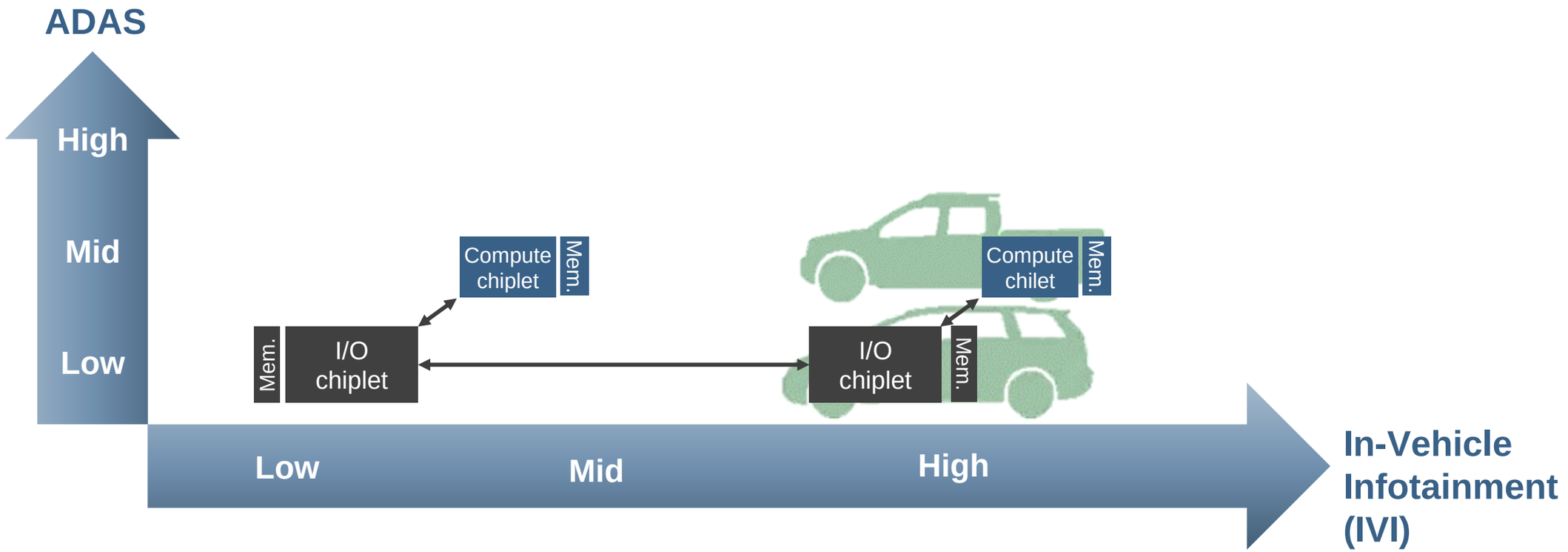


Chiplet Architecture: ADAS chiplet(s)

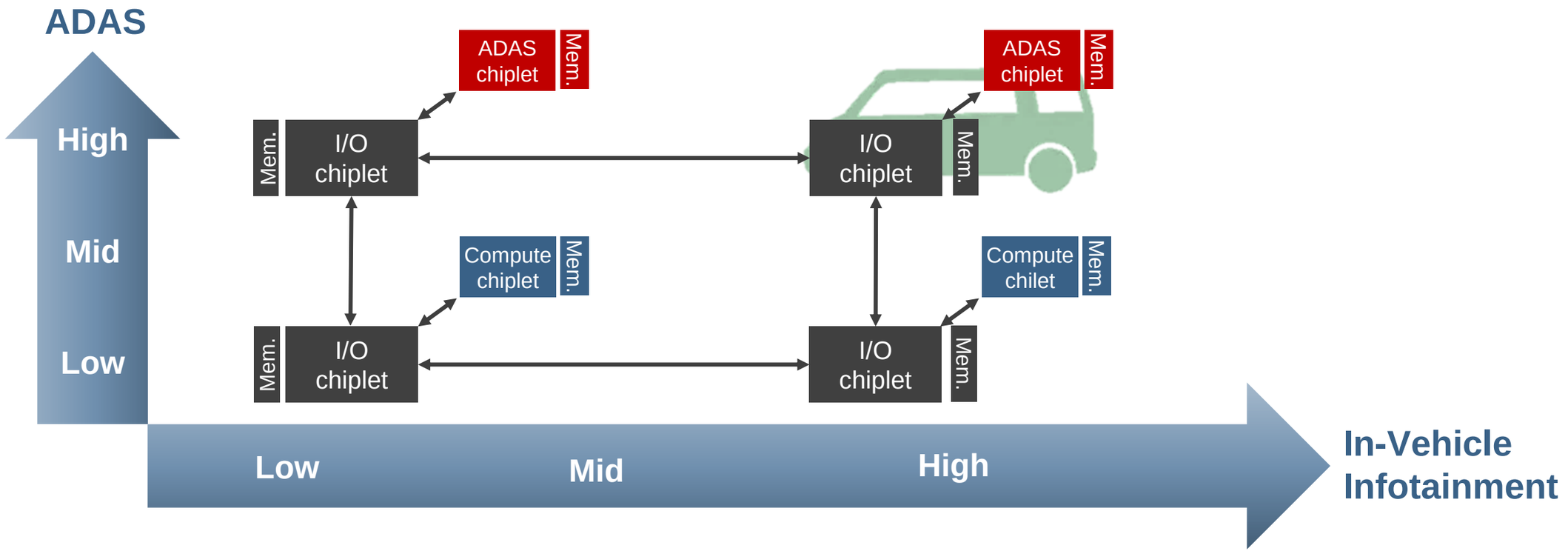


- ADAS chiplet(s):
  - ADAS L3/L4
  - Memory interfaces
  - High speed link:
    - for I/O chiplet connection (I/O coherency)

Chiplet Architecture: scalability towards IVI

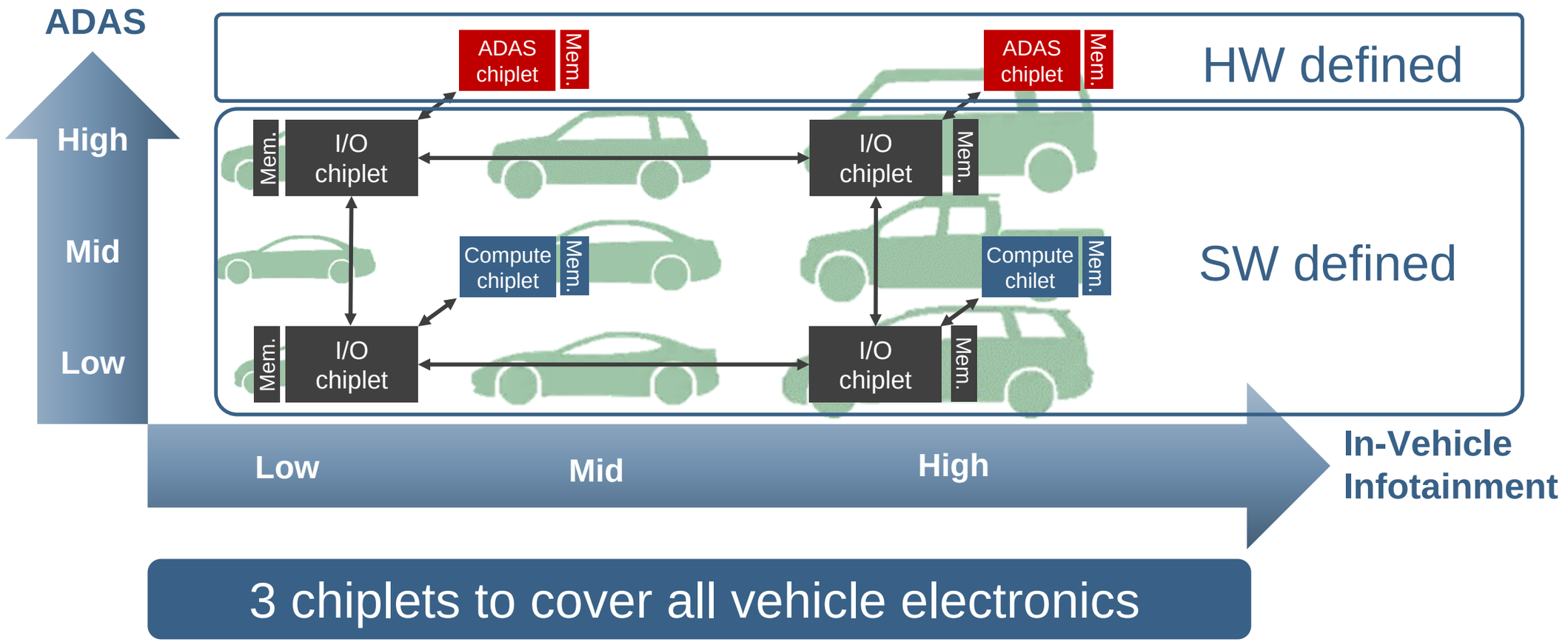


Chiplet Architecture: scalability towards ADAS



Chiplet Architecture

A few chiplets covering all segments – mix HW and SW defined



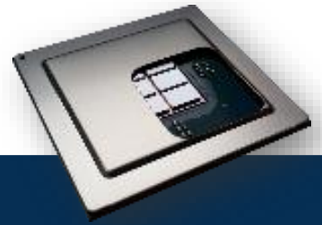
3 chiplets to cover all vehicle electronics

Model-Based System Design

CEA assets in system design

INTACT

3D technologies & design capability

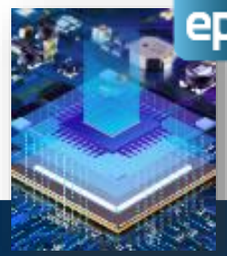


Processor Architecture
Chiplet design

- **World's first 3D System-on-Chip with an active silicon interposer.**
- Mary-core architecture (96 cores)
- 3D integrated circuit:
  - 6x chiplets in 28nm FDSOI
  - 1x active interposer in 65nm

EPI

SW/HW co-design of complex computing architecture



Digital twin

- Full **methodology** of SW/HW **co-design** for general purpose processor specifications
- Delivery to partners of a **Virtual Platform** of the architecture based on the CEA **VPSim tool:**
  - **Performance evaluation** of architectural components
  - Best compromise accuracy & simulation time

FACE

SW application deployment using service-oriented architecture

CES'2019

Model Based SW Engineering

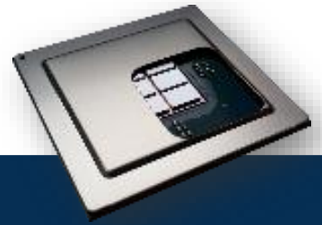
- **Formal model of computation and communication**
- **Model-based software engineering** for timing analysis, software deployment on heterogeneous HW, runtime monitoring (safety-critical system)

One of the lead projects

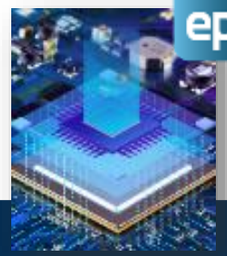
EPI

INTACT

3D technologies & design capability



SW/HW co-design of complex computing architecture



FACE

SW application deployment using service-oriented architecture

CES'2019

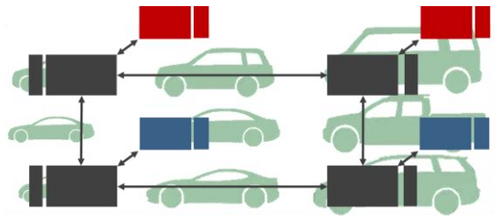
Processor Architecture
Chiplet design

Co-optimization

Digital twin

Co-design

Model Based SW Engineering

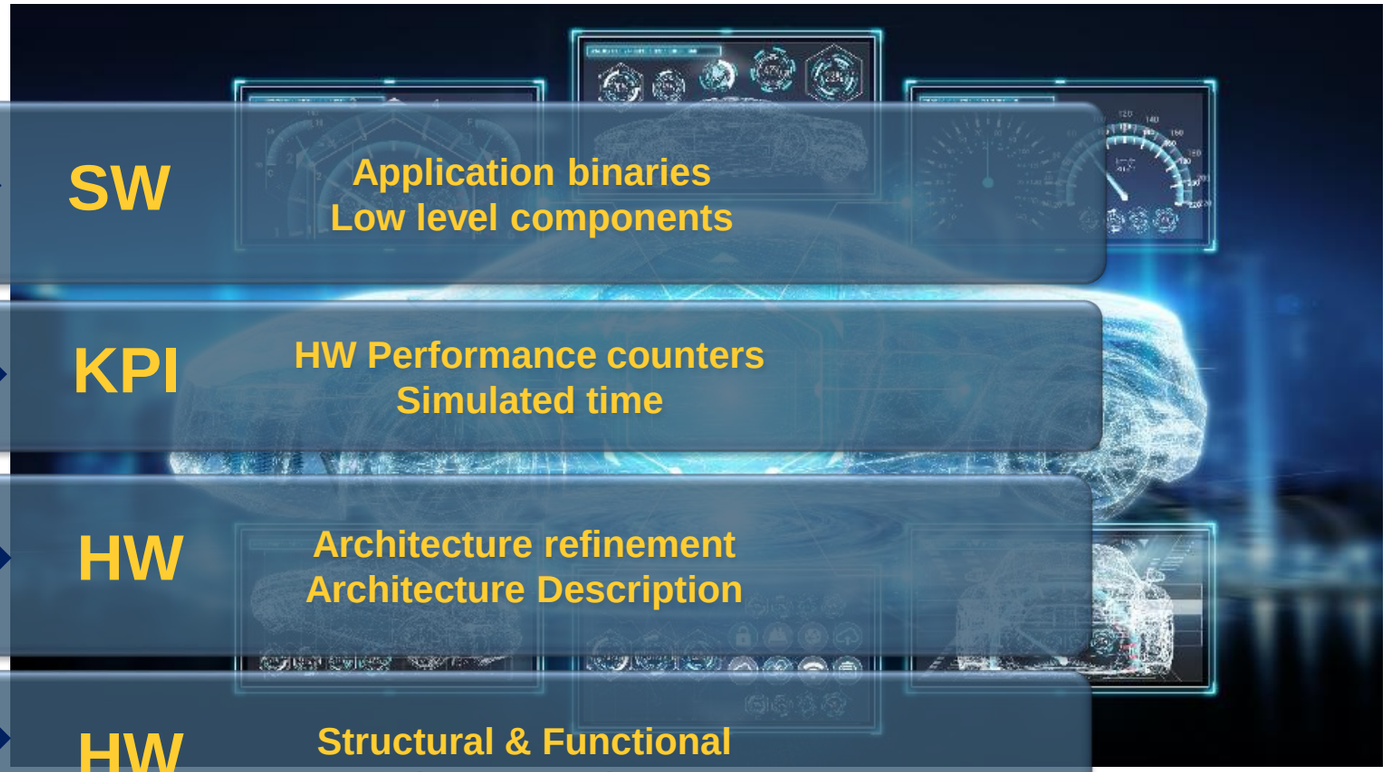


OEM A

Model-based system design enabling adequacy between applications SW and electronics architectures

- Model based SW deployment and validation
- Virtual prototyping HW models
- Automated Design Space exploration

Model-based system design



Model based SW deployment and validation → SW: Application binaries, Low level components

Virtual prototyping HW models → KPI: HW Performance counters, Simulated time

Automated Design Space exploration → HW: Architecture refinement, Architecture Description

Chiplet architecture baseline → HW: Structural & Functional Disaggregation

Tools | Inputs/Outputs

cea list

Conclusion

- The automotive E/E architecture in moving towards “server on wheels”.

- Chiplets are an attractive value proposition for “server on wheels” :
  - best trade-off between software-based and hardware-based architecture,
  - a few chiplets cover all the needs (in terms of Performance, Power, Area, Cost and Time to market).

- Chiplet-based architectures require system-level design automation based on models:
  - virtual prototyping,
  - automated design space exploration,
  - SW deployment.

Thank you for your attention

Acknowledgements:

- 3D architecture, design & virtual prototype CEA-List teams
- 3D technology CEA-Leti teams

Industrial partners

Denis Dutoit – CEA List

Program Manager

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References

Slide 5:

[VLSI'2013] D. Dutoit et al., "A 0.9 pJ/bit, 12.8 GByte/s WideIO memory interface in a 3D-IC NoC-based MPSoC," 2013 Symposium on VLSI Technology, Kyoto, Japan, 2013, pp. C22-C23.

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