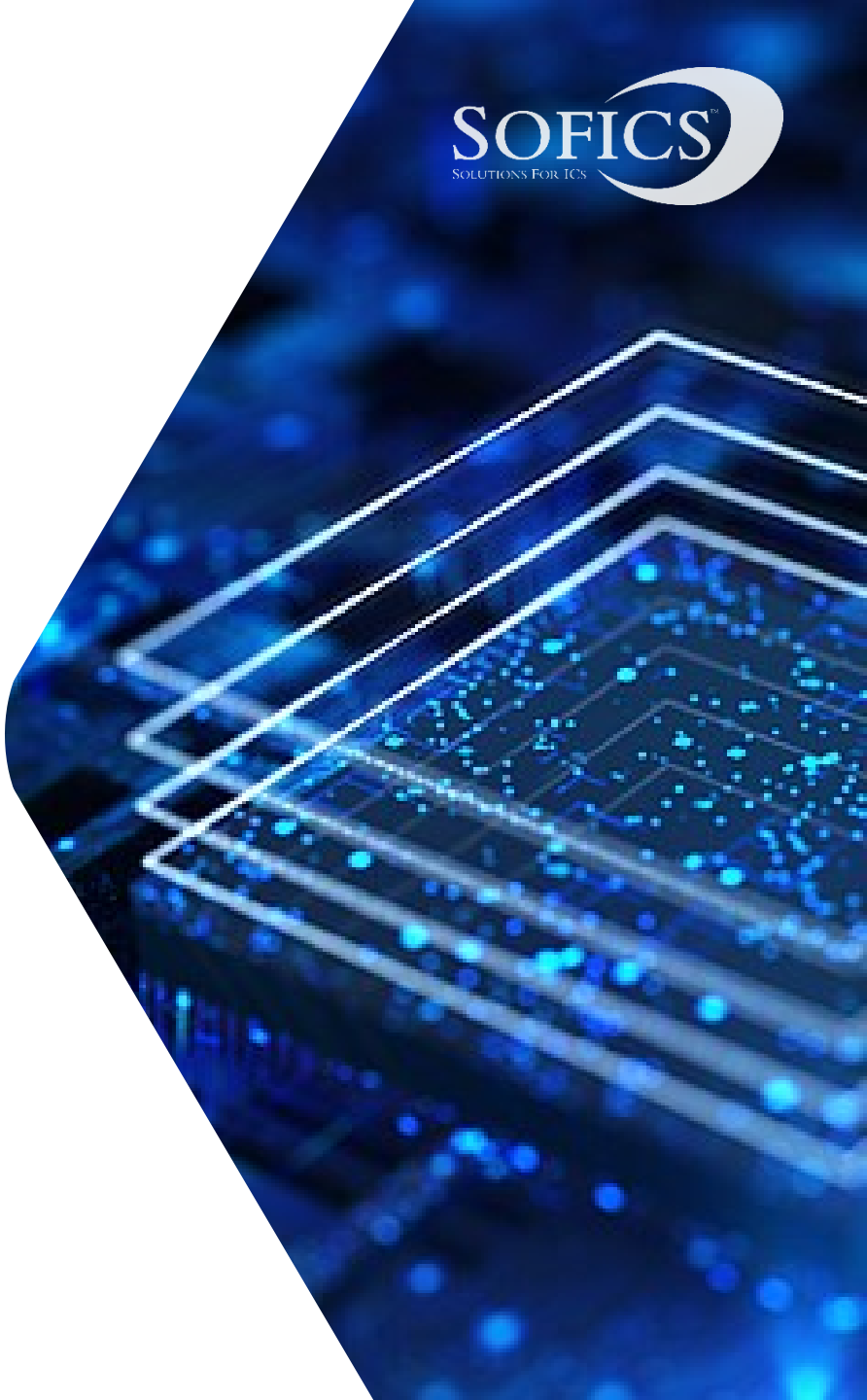
CHIPLET SUMMIT

2024

PROTECTING AGAINST ESD IN DIE-TO-DIE INTERFACES



SOFICS – 2024

Outline

- **ESD for die-2-die interfaces**
  - **Requirements**
- ESD protection for I/Os
- Examples
- Select the right ESD robustness level

ESD requirements for die-2-die interfaces / chiplets

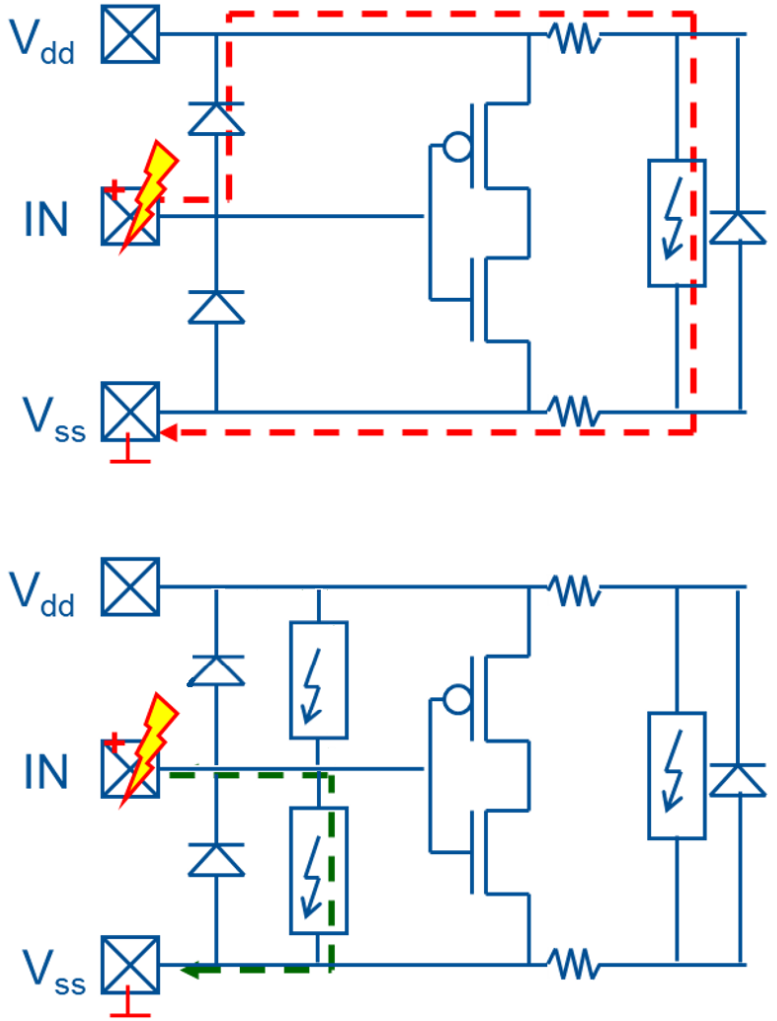
- Die-2-die interfaces need specialty ESD protection
  - Much smaller **area** than GPIO
  - **Flexibility** related to power grid
  - **Signal voltage** below the GPIO voltage range
  - Lower **drive current** compared to regular I/Os
  - ESD protecting for **thin oxide** transistors
  - (Very) low **parasitic capacitance**
  - Lower **ESD robustness** can be tolerated.

Outline

- ESD for die-2-die interfaces
- **ESD protection for I/Os**
  - **Conventional approach**
  - **Local clamp approach used by Sofics**
- Examples
- Select the right ESD robustness level

Local ESD clamp in I/O area

- **Conventional** ESD protection
  - Dual diode approach
  - Not optimal for die-2-die
- **Solution**: Local clamp
  - Strongly **reduced voltage drop** during ESD
  - Reduced **dependence on power clamp**
  - Reduced parasitic **capacitance**
  - Reduced **leakage**
  - Easy **optimization**
  - **Flexibility** for die-2-die and I/O segments

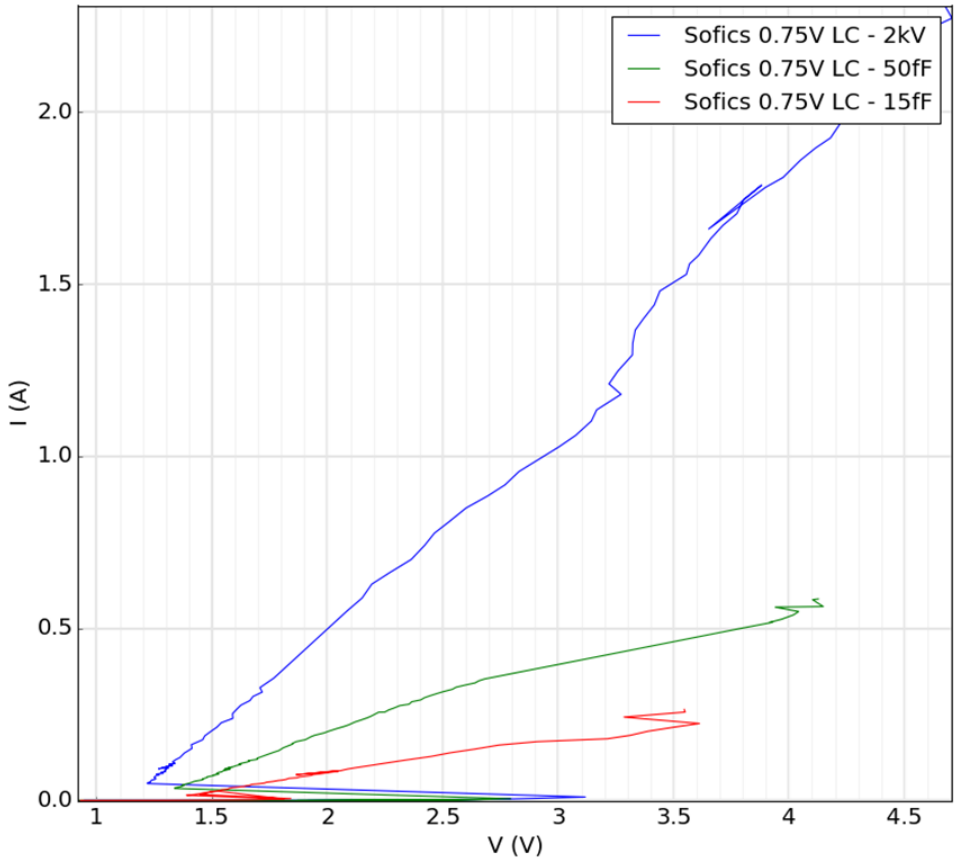


Outline

- ESD for die-2-die interfaces
- ESD protection for I/Os
- **Examples**
  - TSMC 7nm
  - TSMC 6nm
  - TSMC 5nm
- Select the right ESD robustness level

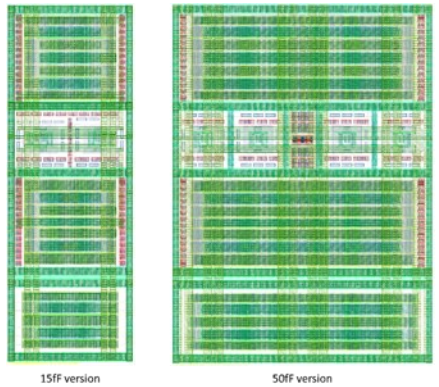
Local ESD protection in 7nm FinFET

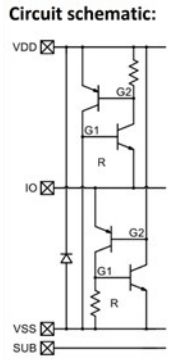
- Silicon proven
  - Sensitive circuit
    - Uses thin oxide transistors
  - Different versions
    - 2kV HBM for regular IO circuits
    - 400V HBM for die-2-die interface
    - 150V HBM for die-2-die interface
  - Lower HBM rating
    - Smaller size
    - Lower parasitic capacitance
    - For high-bandwidth interconnect



Local ESD protection in 7nm FinFET

- Silicon proven
  - Full-local ESD protection
    - ESD-on-SCR
  - Different versions
    - 2kV HBM for regular IOs
    - 400V HBM for die-2-die interface
    - 150V HBM for die-2-die interface

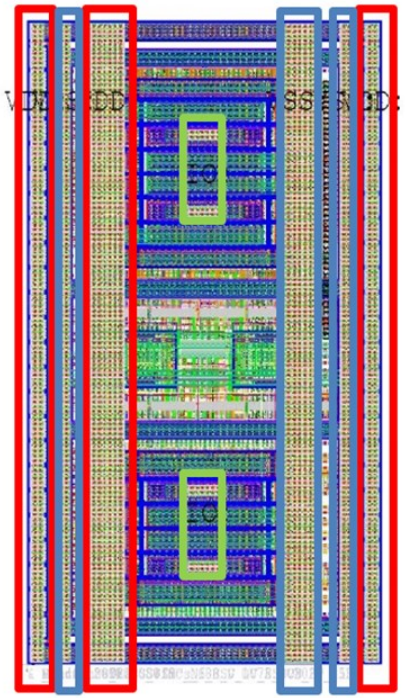


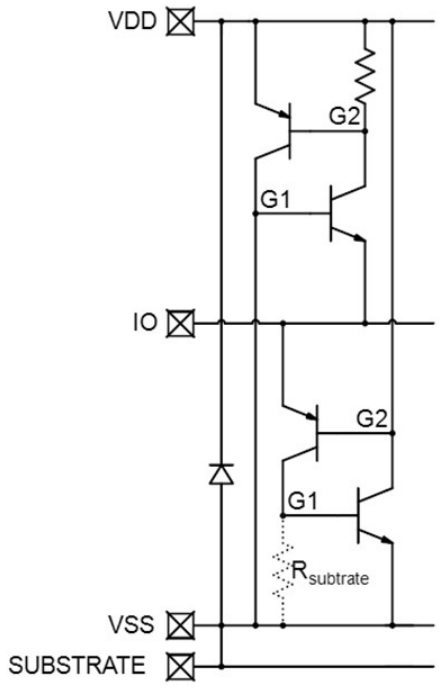


HBM [V]	Capacitance [fF]	Width [um]	Height [um]	Area [um²]	SCR width [um]
150V	15fF	7.43	21.1	<160	2x 3.5
400V	50fF	15.4	21.1	<330	2x 11.5
2kV	Not optimized	24.3	30	<750	4x 20.8

Local ESD protection in 6nm FinFET

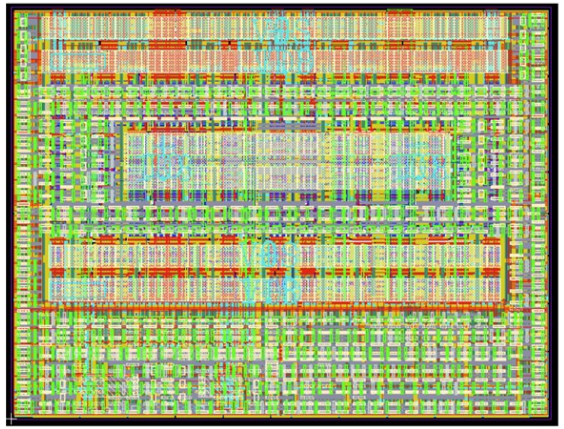
- ESD protection for SerDes Tx
  - 0.75V SerDes interface
  - Total parasitic capacitance:
    - <13 fF
  - ESD protection:
    - 100V HBM
  - Leakage at 0.75V DC
    - 10pA at 25°C
    - 100pA at 125°C
  - Area: 7.5um x 22um

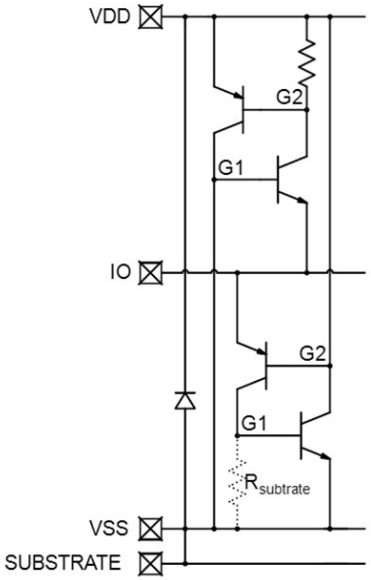




Local ESD protection in 5nm FinFET

- ESD protection for SerDes Tx
  - 0.9V SerDes interface
  - Total parasitic capacitance:
    - <14 fF
  - ESD protection:
    - 100V HBM
  - Leakage at 0.9V DC
    - <100nA
  - Area: 10um x 13um



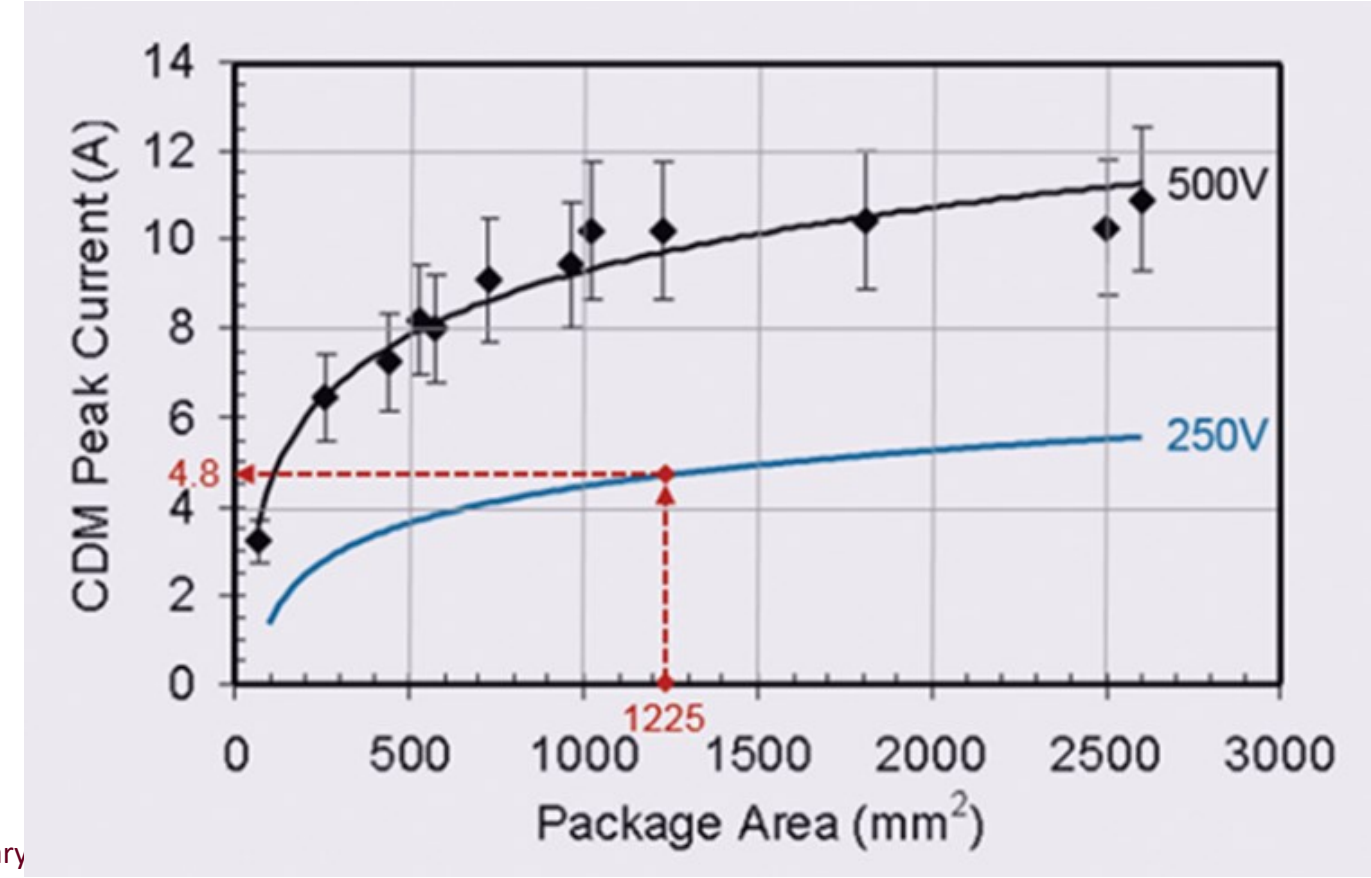


Outline

- ESD for die-2-die interfaces
- ESD protection for I/Os
- Examples
- **Select the right ESD robustness level**

CDM peak current depends on package size

- CDM peak current (vertical)
  - Depends on CDM voltage
  - Depends on package area (horiz.)
- Example: 250V CDM
  - Small package: < 2A peak current
  - Larger package: ~5A peak current



Industry discussion to reduce CDM for SerDes

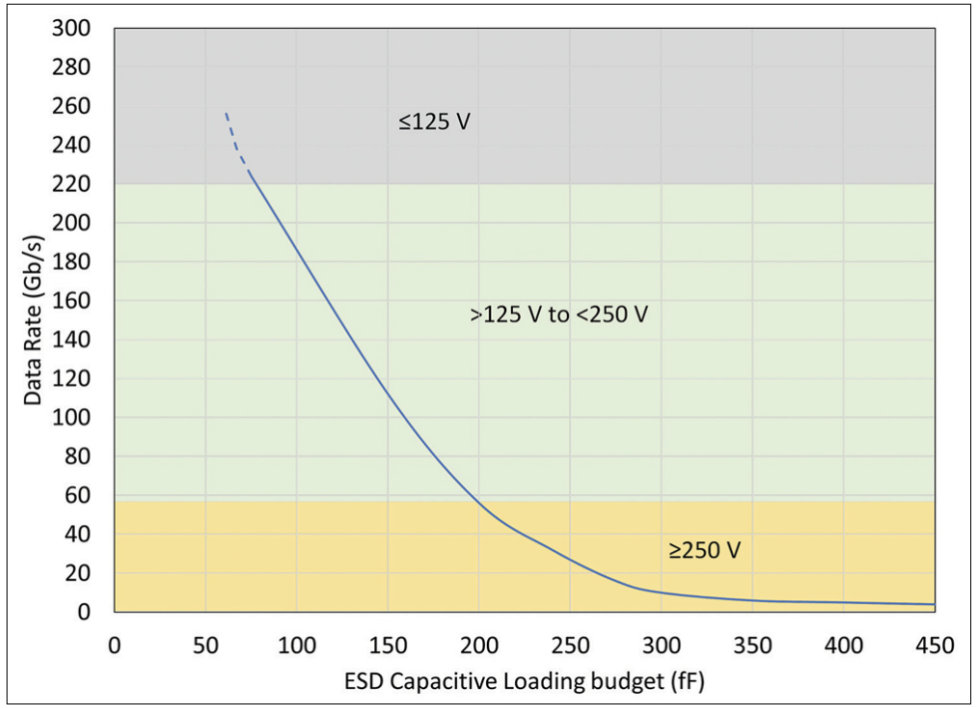


Figure 2: Data Rates of single lane SERDES vs. Allowed ESD Capacitive Loading Budget of high-speed IO circuits using non return to zero signaling. From [3]

- CDM related to cap. budget
  - Below 75fF
    - CDM of 125V
    - 220 Gbps and faster
  - 75fF to 200fF
    - CDM between 125V to 250V
    - 56 to 220 Gbps
  - 200fF loading capacitance
    - CDM of 250V
    - 56 Gbps or slower

Further reduced CDM level for die-2-die interfaces

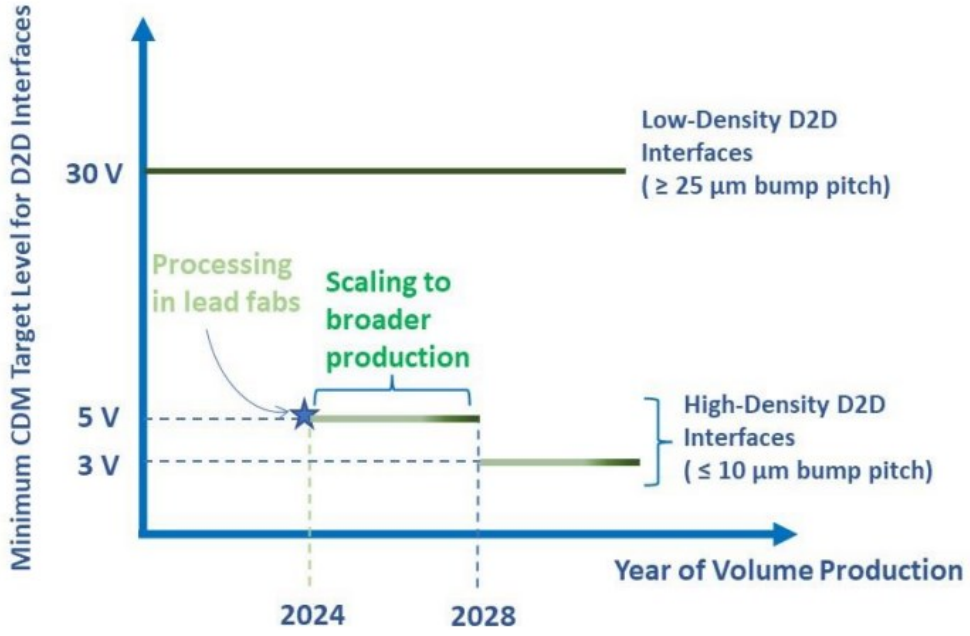


Figure 1: Roadmap of CDM Targets of Die-to-Die Interfaces

Table 1: Conversion Table of V_{CDM} to I_{peak} in a CDM Test Set-up According to ANSI/ESDA/JEDEC JS-002.
Note: The peak current depends on the die size. The average peak currents for the small and large calibration targets are presented.

V_{CDM}	I_{peak} for C (die) = 7.2 pF (corresponds to a typical die area of ~ 62 mm^2)	I_{peak} for C (die) = 55 pF (corresponds to a typical die area of ~ 500 mm^2)
125 V	1.9 A	3.0 A
30 V	455 mA	720 mA
5 V	76 mA	120 mA
3 V	46 mA	72 mA

- Industry discussions
  - Lower CDM specifications
  - 125V to 250V for regular pads
- Chiplets, further reduced
  - CDM of 30V for low density D2D
  - Further reduction to 5V and 3V
    - High density D2D
    - Leading fabs (ESD control!)

https://esdindustrycouncil.org/ic/en/shared/industry-council-white-paper-2-pii-rev-1.0-final.pdf

Outline

- ESD for die-2-die interfaces
- ESD protection for I/Os
- Examples
- Select the right ESD robustness level
- **Why Sofics?**

Sofics IP: Solutions for ICs

20+
years in business

5000+
IC designs use Sofics IP

All kinds
of applications

70+
patents

5M+
wafers with Sofics IP

10+ years
TSMC partner

100+
customers

2B+
ICs rely on Sofics IP

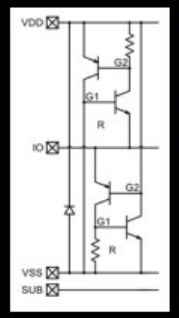
50+
processes
0.5um – 3nm

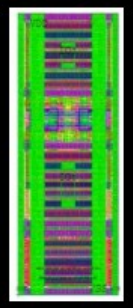
Chiplet partnership – DECA / Sofics

ESD protection has large impact on efficiency

Capacitance from ESD protection is a significant factor for energy efficiency

ESD capacitance on both die can be larger than wire capacitance

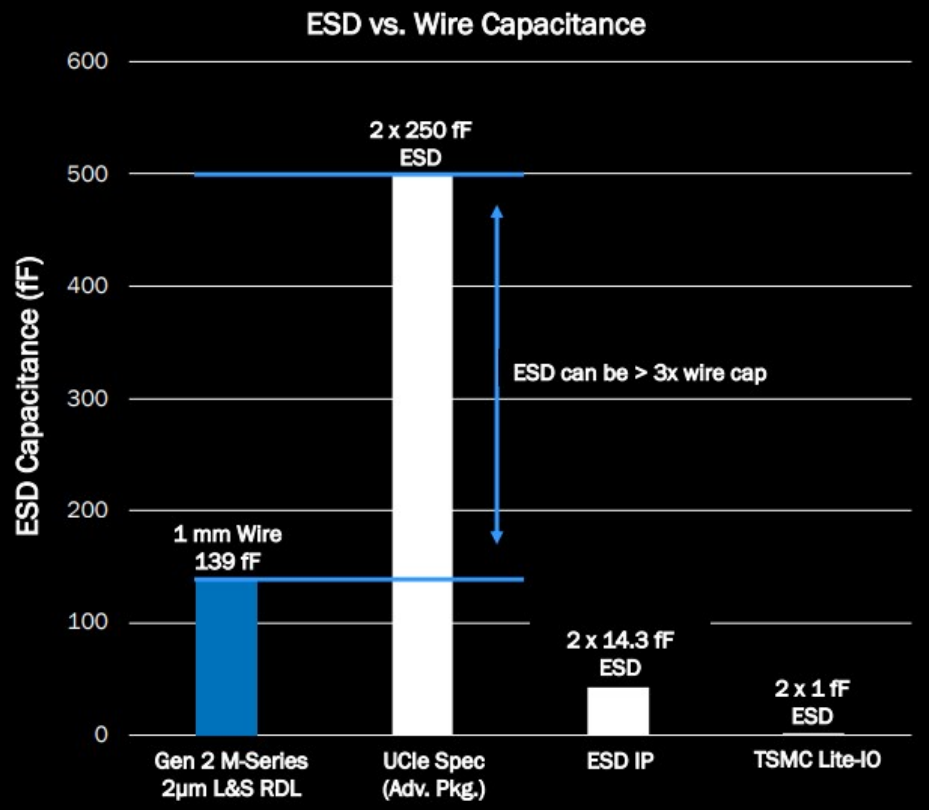




SOFICS

Process: TSMC N7 FF – GOX2 = 1.8V
Used Metals: 7 metals
Special Layer required: Deep Nwell
Area: 156.62µm² (7.426µm x 21.09µm)

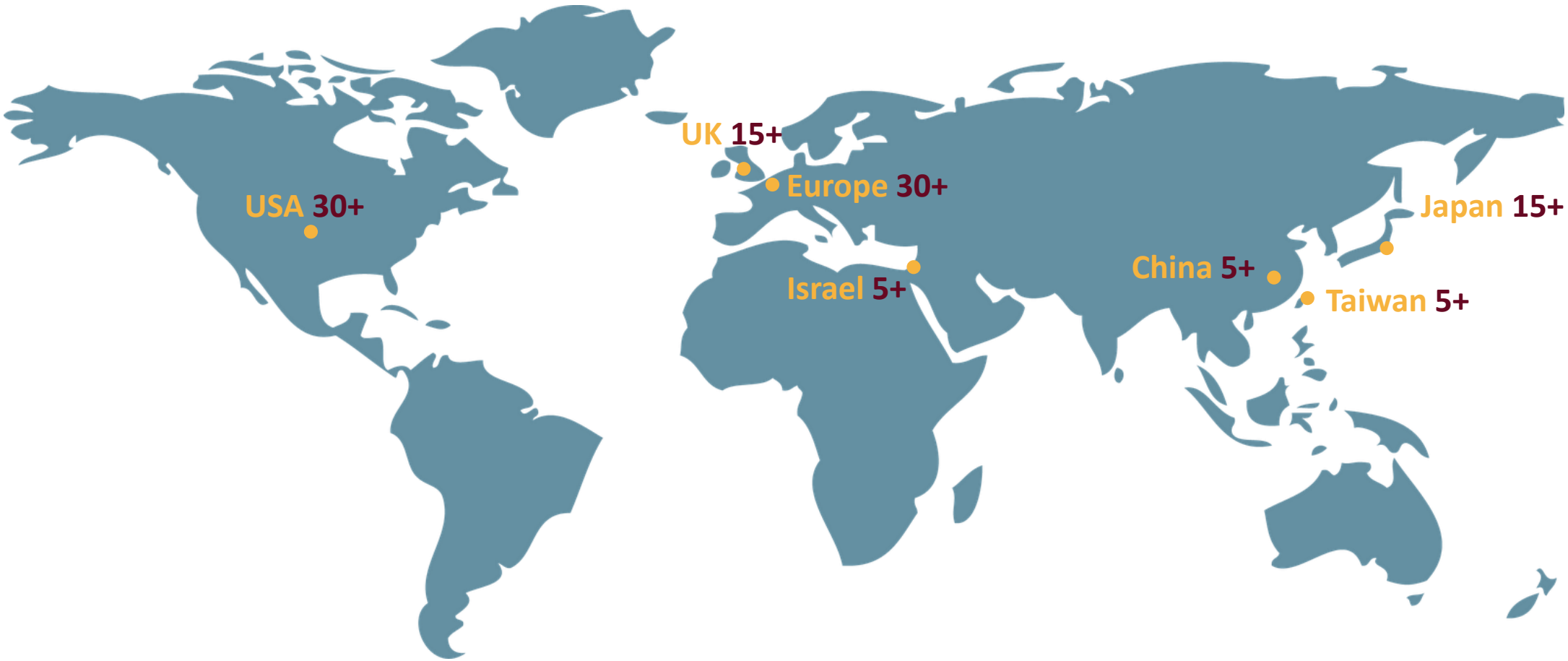
Example ESD IP for TSMC N7 from Sofics



DECA

Deca released for Chiplet Summit 2023

100+ customers globally



Customer success example

Graphcore Colossus

AI accelerator on TSMC 16nm FinFET

23.5B transistors

800mm²

Phil Horsfield, VP Silicon

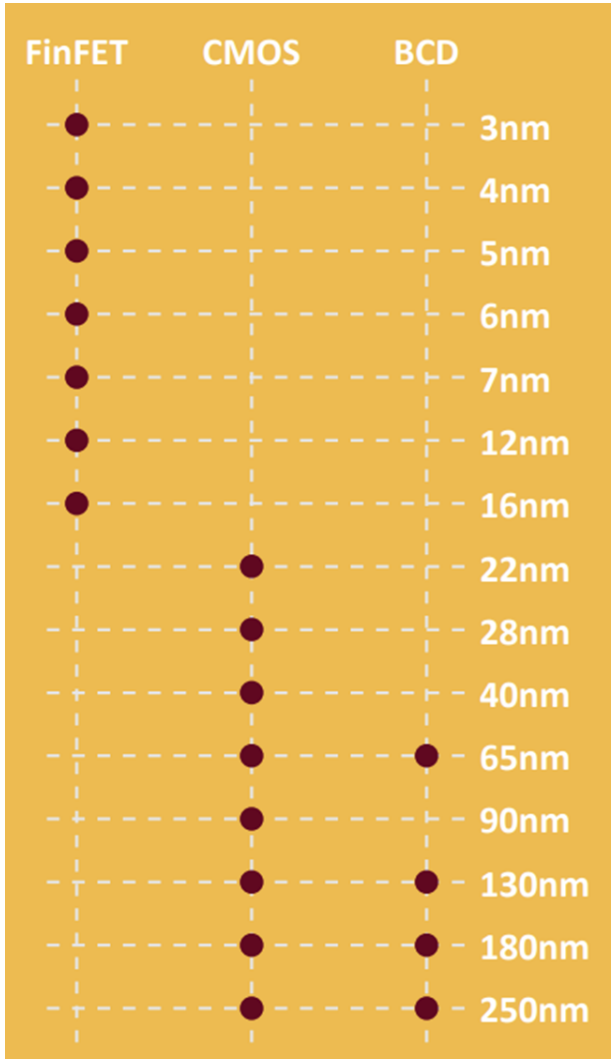
"Sofics offered us flexibility with customization, a proven silicon ESD portfolio and fast time to market. Within just a few weeks we went from first contact to contract to solution delivery."

Sofics' strategic partnership with TSMC

TSMC relationship

- Sofics supports **60+ TSMC customers**
  - USA, Europe, Israel, Japan, China,…
- Close **cooperation 10+ years**
  - DCA alliance member since 2008
  - IP alliance member since 2010
- **TSMC9000** assessment
  - Frequent MPW shuttles
  - BCD, CMOS, FinFET
- TSMC audited **secure vault**
  - FinFET designs in office in Belgium

Sofics' IP is proven on 50+ processes



CMOS

- Mature: 0.5um to 180nm
- Mainstream: 130nm to 65nm
- Advanced: 40nm to 22nm

FinFET technology

- 16nm to 3nm

SOI technology

- 130nm to 22nm

BCD technology

- 250nm to 55nm

BiCMOS technology

Sofics IP is used in many applications

Internet of Things, wearables

15+ customers

Focus: Low power

Artificial Intelligence

5+ customers

Focus: High performance

Space applications

5+ customers

Focus: Radiation hard solutions

Sofics IP is used in many applications

Automotive

15+ customers

Focus: Higher reliability

Medical

5+ customers

Focus: Higher reliability

Datacenter and wireless

40+ customers

Focus: Low parasitic capacitance

Meet our team in Belgium

Next steps

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Sofics website: www.sofics.com

Articles: https://monthly-pulse.com/

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