Chiplet Integration and Production Test Simplification

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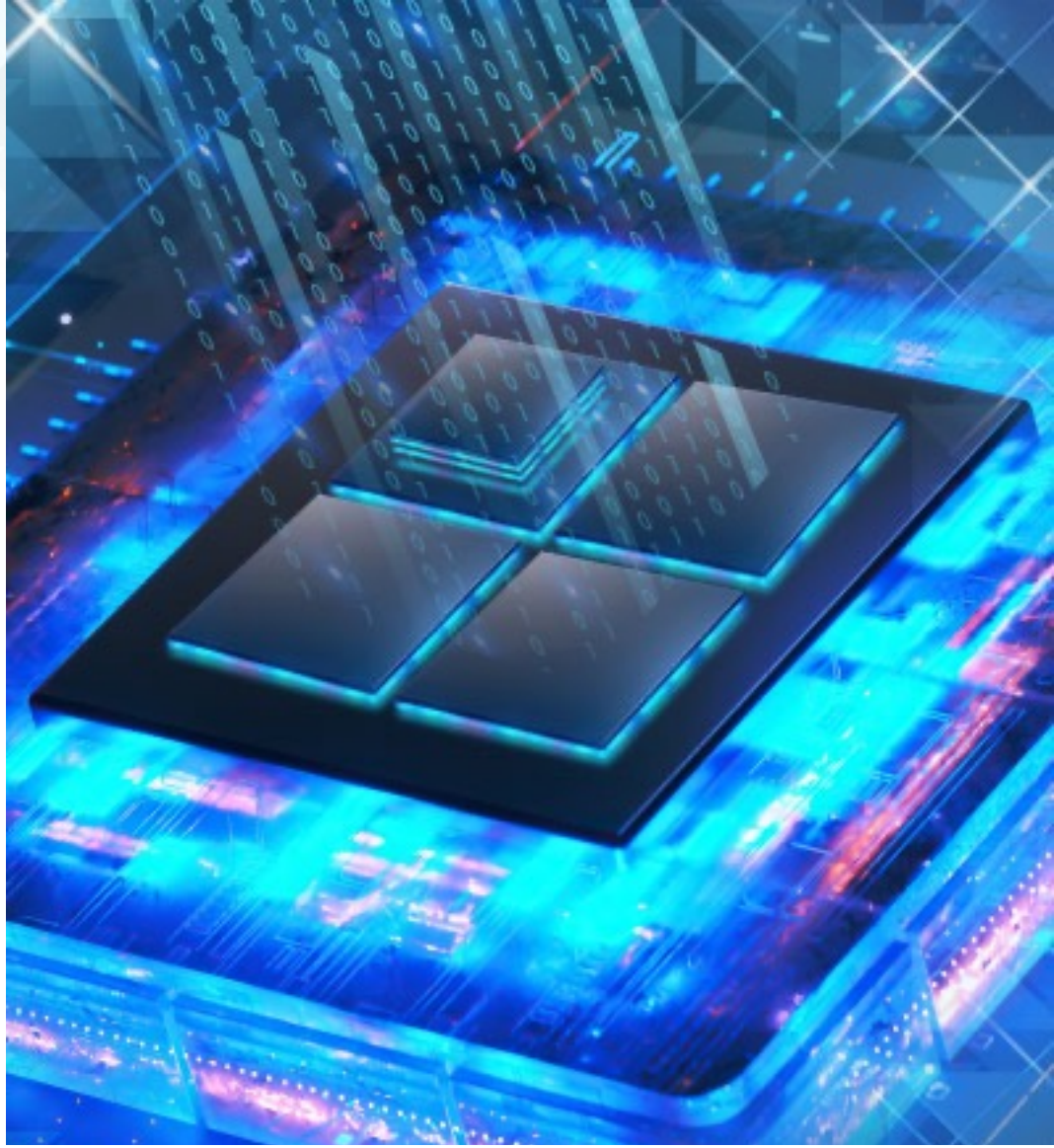


Agenda

1. Integration End Markets
2. Assembly Package Integration Technologies
3. Amkor Examples
4. New UCIe™ standard
5. Production Test Simplification & Ecosystems

Amkor Integration Market Applications

Automotive, Health, Industrial

ADAS, SiP/IVI
MEMS, sensors
Performance, safety

Communications

5G, RF & mixed signal
Handheld devices
Mobile/Smartphones
Tablets, IoT, satellite

Artificial Intelligence, Networking, Computing

Networking
Data center, infrastructure
PC/Laptop, storage

Consumer

Connected home
Set-top box, televisions
Visual imaging, wearables

Multi-die Packages Are Ubiquitous!

Why Stuff Packages with Multiple Die?

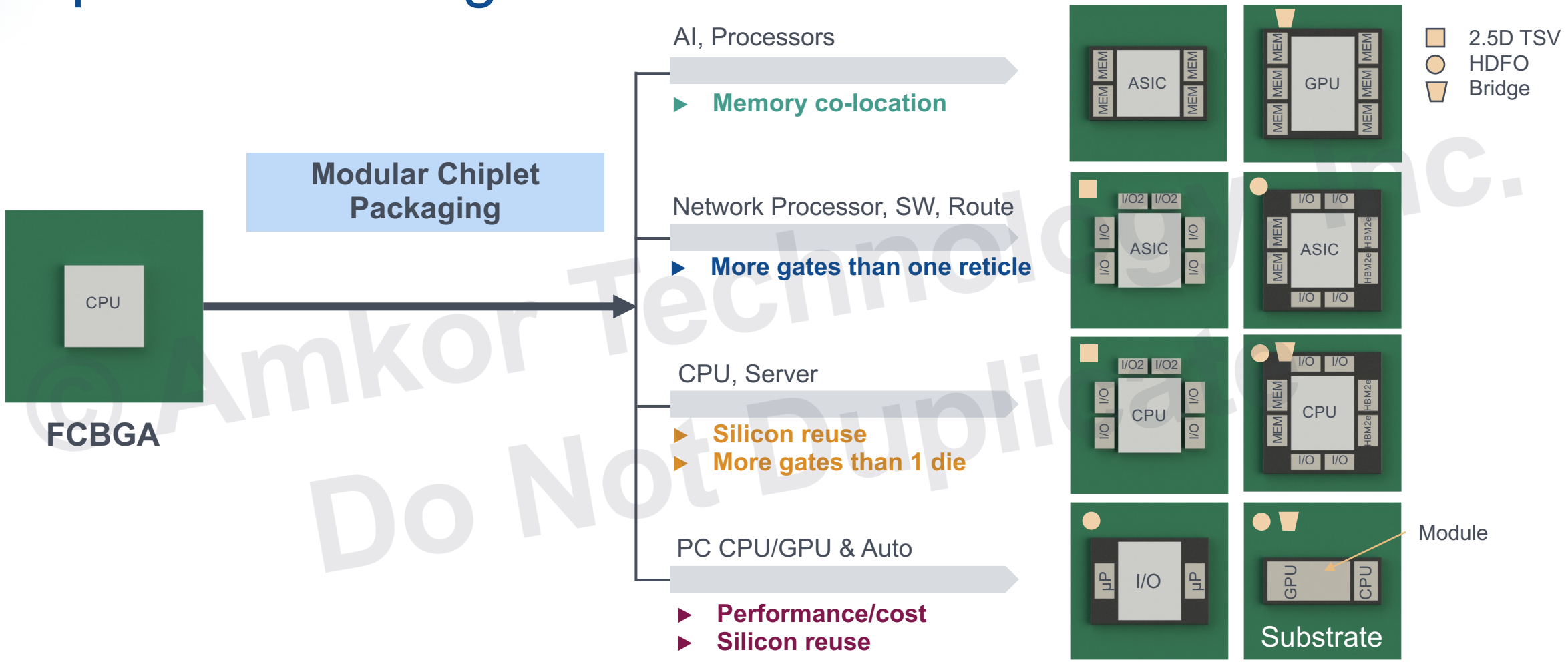
Enhanced Levels of Integration
Chiplets from different fab technologies; Unequal shrinks for specific technologies

Modular Design
Lego block design; Instantiate custom block count

Silicon to Package Footprint
Linear aggregate Si area for monolithic die

Cost
Per functional block

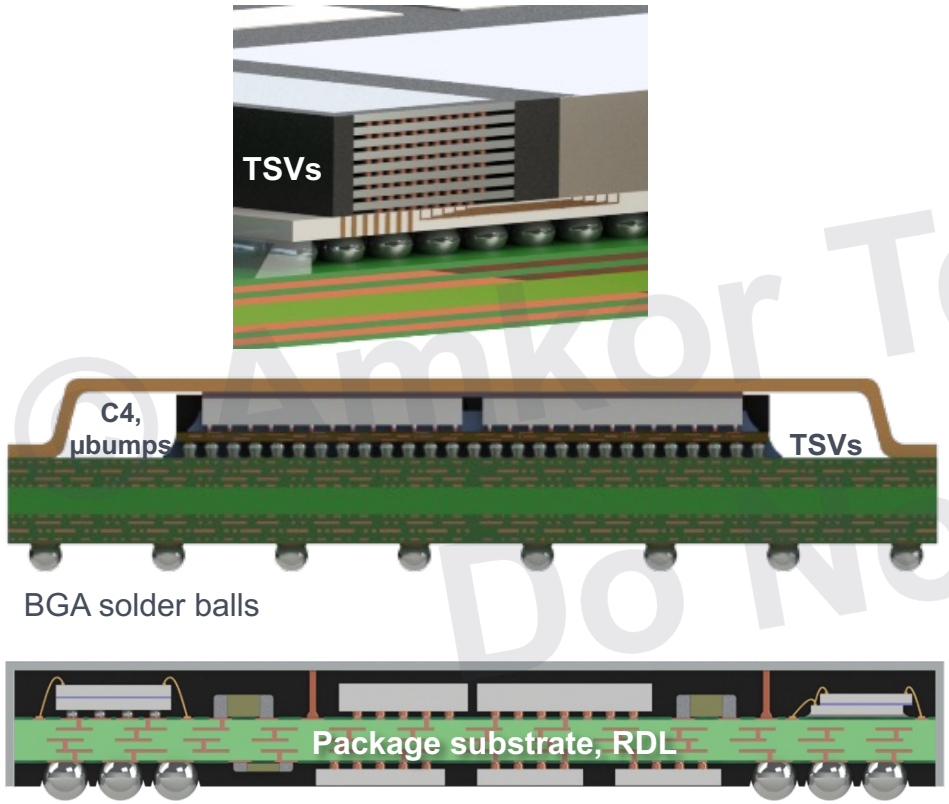
Chiplets & Packages



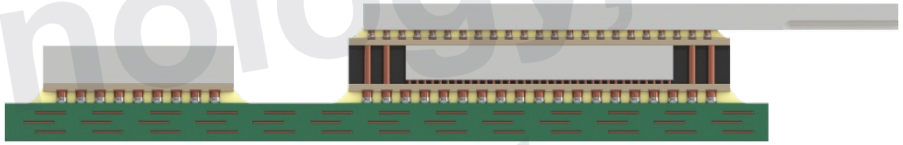
Die Disaggregation, to Allow Higher Levels of Integration!

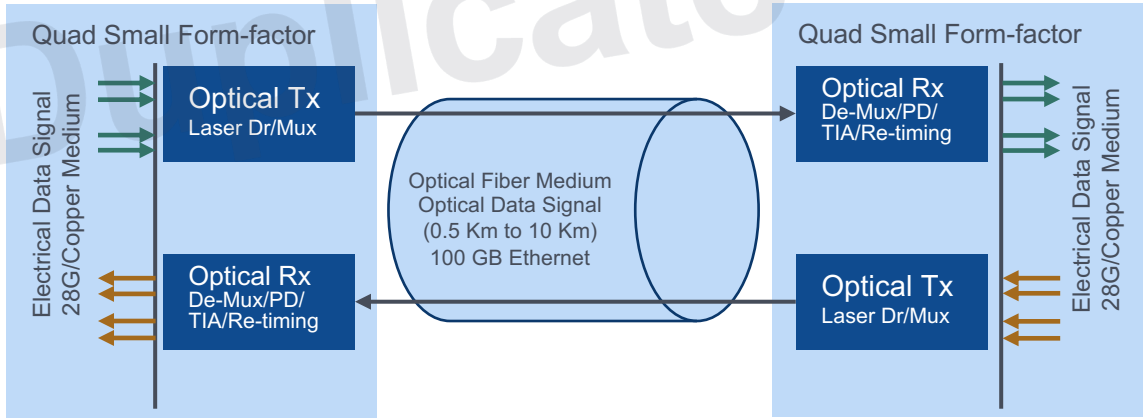
Example of Amkor Package Assembly Topologies

ASIC/CPU/GPU/FPGA, HBM



Si Ph Enabling 100 to >400 Gbps Data Rates

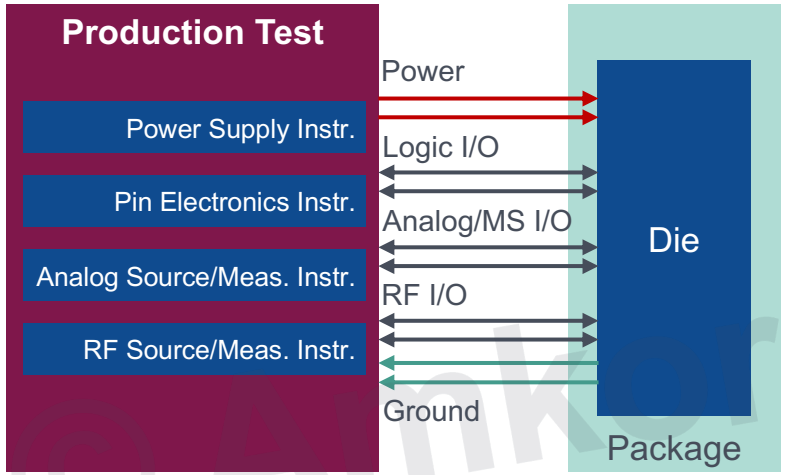




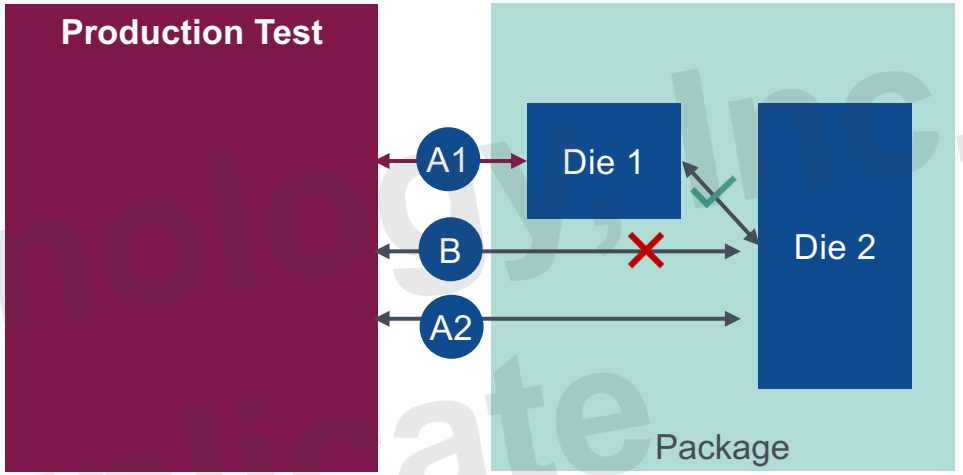
As Packaging Complexities Increase, New Matching Test Methodologies Must Be Architected

Production Test Challenges

Direct Test Access



Indirect Test Access



- Functional & structural test content
  - BIST, SBFT, scan – IEEE 1149.x, 1500, 1687, 1838
- Digital test instrumentation features
- Concurrent testing

Die 2 interface physically

- A Pinned out
- B Not pinned out

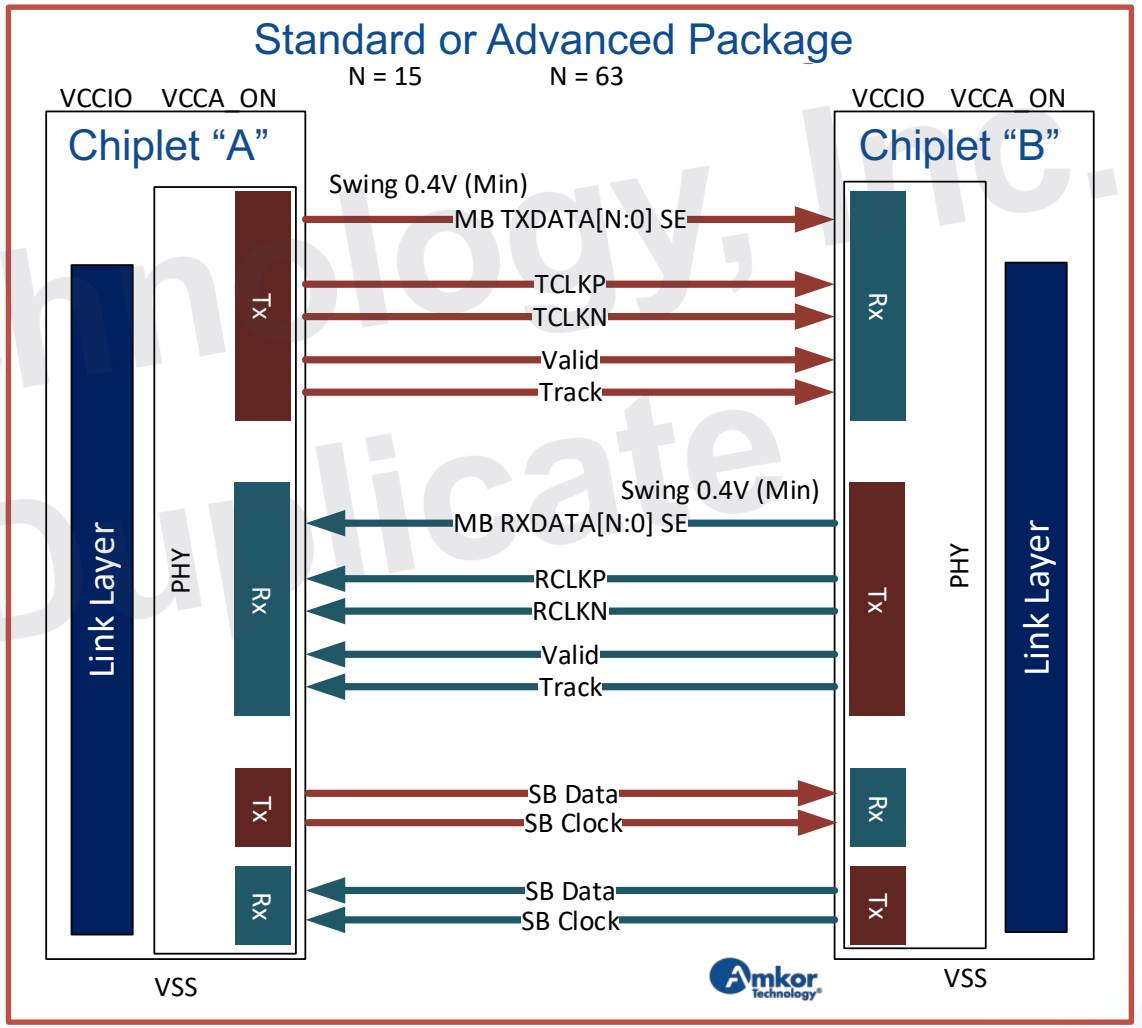
Limited Ability to Stimulate, Test and Measure Individual Dies and Interconnect in Adv. Pkgs

UCIe Standard Attempts to Address the "Standardization" Needs

Universal Chiplet Interconnect Express (UCIe v1.1)

Standard & Advanced 2.xD Package

- Latency: <2nS
- Data width: 16...64 module, unidirectional NRZ
- Data rate: 4...8...12...16...24…32 Gb/s; fwd clk: 8 GHz (Ref: 2 GHz)
- Bit error rate, channel reach, power efficiency, data lane swing, clock skew, impedance, total jitter, lane-to-lane skew, rise time, fall time, crosstalk
- Sideband – high data rate



Source: UCIexprss.org. UCIe is trademark Universal Chiplet Interconnect Express

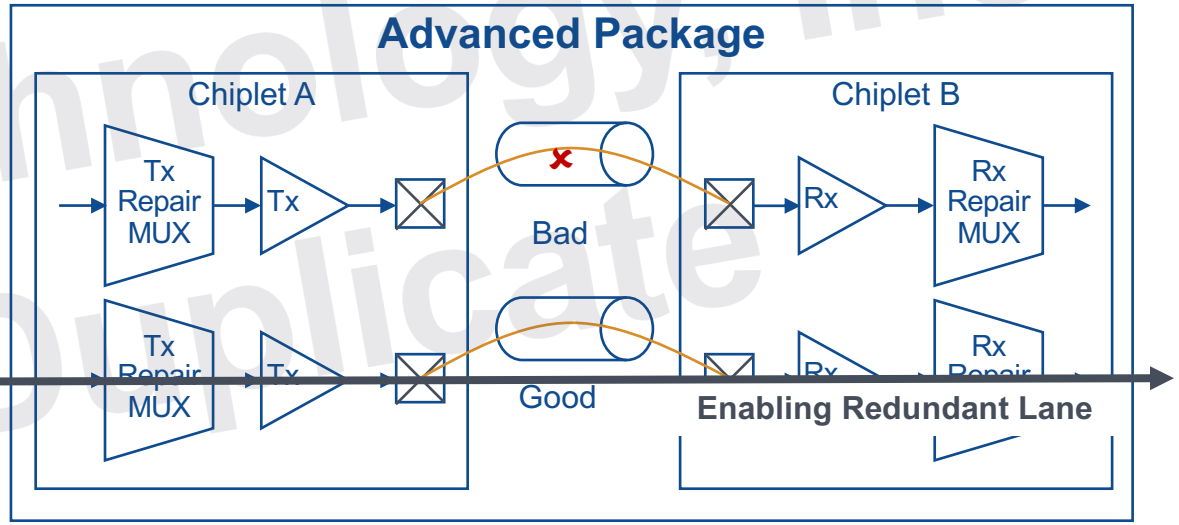
UCIe Test Methods – Production Test Simplification

Fixed Shoreline to Enable Chiplet Place & Route Simplification & Interoperability

Source: UCIexpress.org. UCIe is trademark Universal Chiplet Interconnect Express

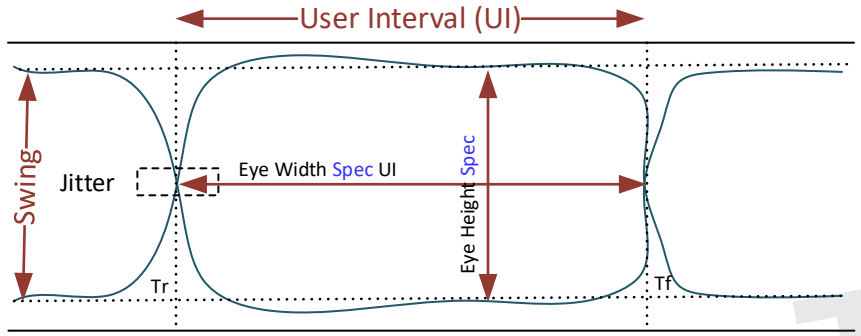
UCIe Test Methods – Production Test Simplification

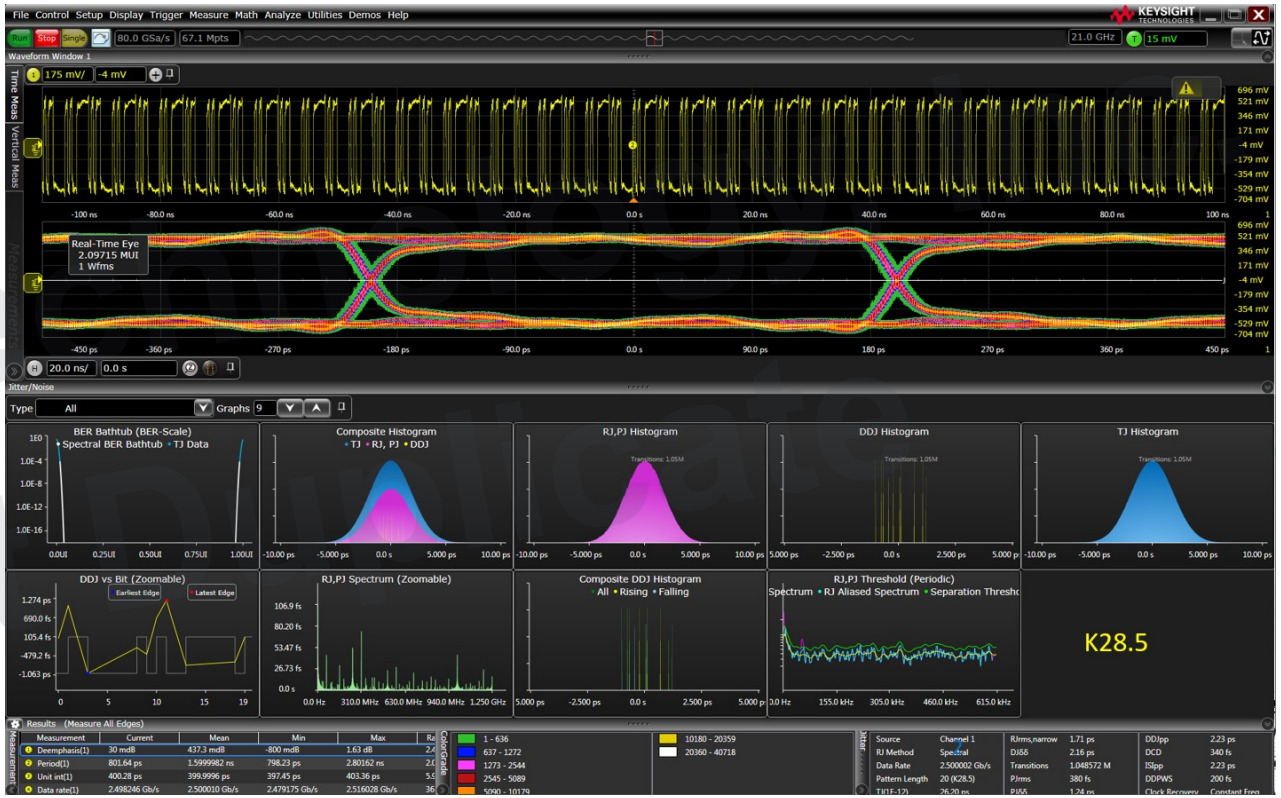
- Redundancy repair
  - Data, valid, diff clock, track, sideband
- Width degrade
- Lane reversal



The Standard Allows For Recovery During the Manufacturing Test Workflow

UCIe Test Methods – Production Test Simplification



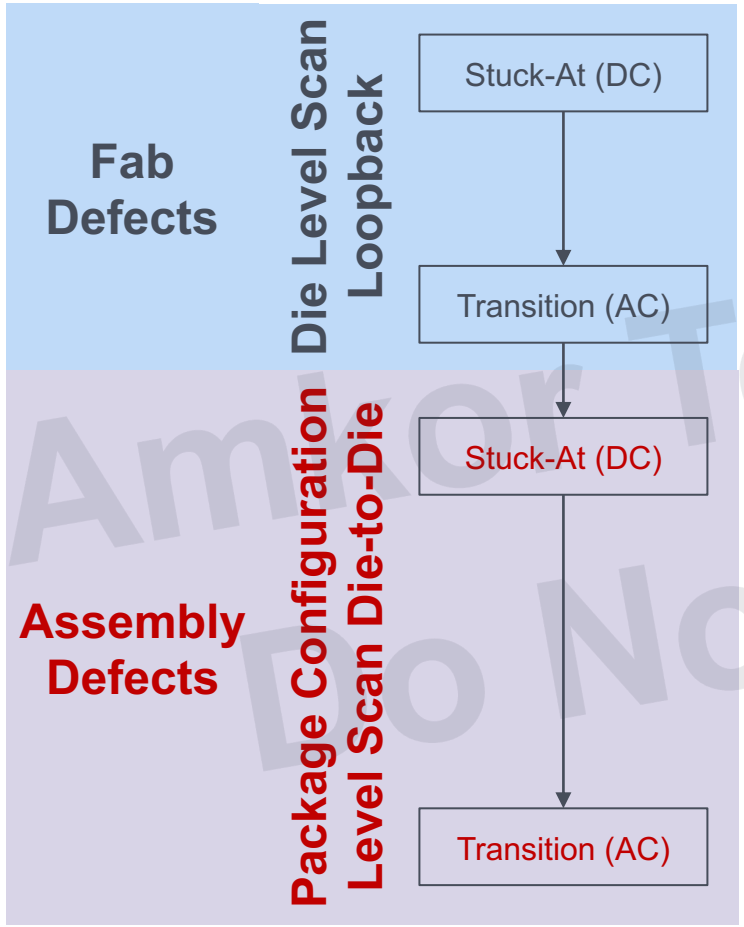


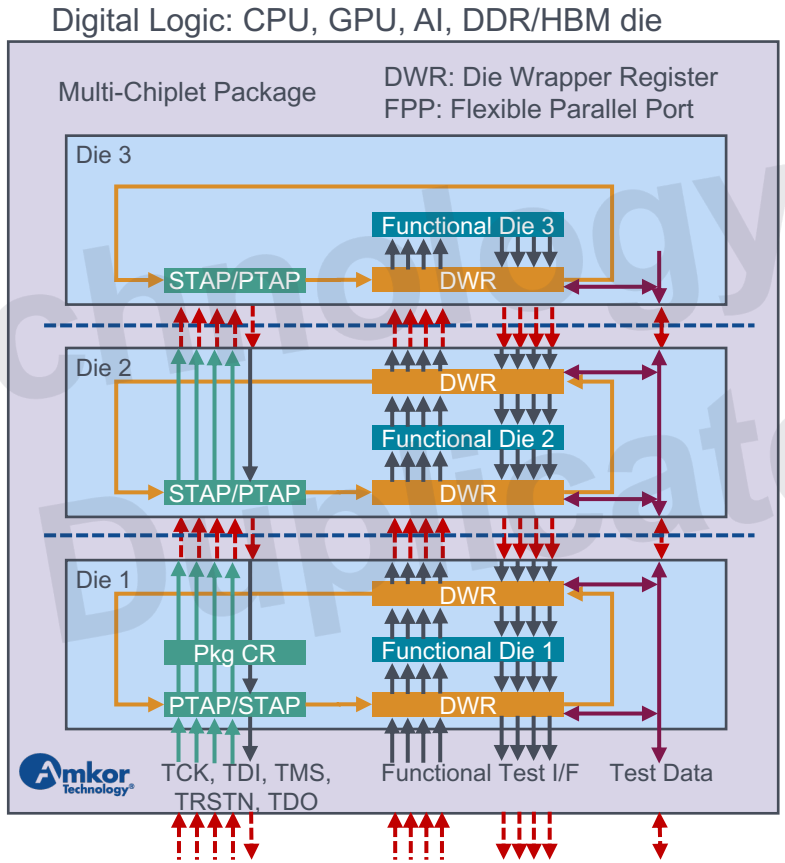
- Mission mode Tx, Rx eye
  - Margining
  - Characterization
  - Hardware & software
  - Calibration
- On-die sensors

The Standard Allows Package Process Health Indicator (PHI) Monitoring

Source: UCIexpress.org. UCIe is trademark Universal Chiplet Interconnect Express

Advanced Package: Design For Test (DFT)



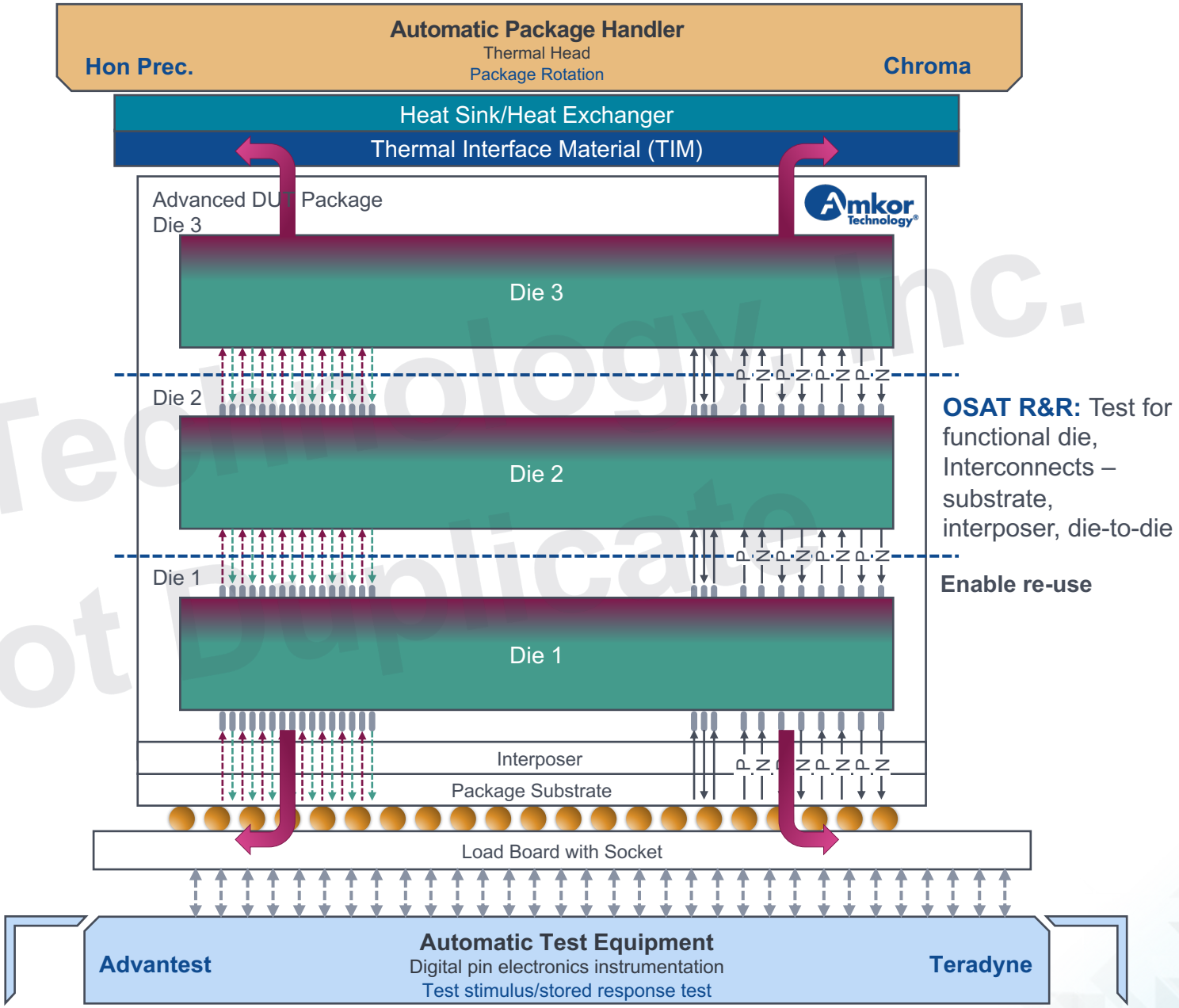


Scan Test Content to Screen Assembly Defects

Reference: "IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits," IEEE Std 1838-2019 , vol., no., pp.1-73, 13 March 2020, DOI: 10.1109/IEEESTD.2020.9036129.

Adv. Pkg. Test Challenge

- Power
  - Cu pillar & µbump – contact resistance
- Signal
  - Capacitive loading for signal & ground
  - Crosstalk & increased noise in Si substrate
  - Insertion loss & return loss – via/bump interface
- Thermal
  - Interconnect/underfill layers
  - End-of-the-line layers
  - Bulk silicon
  - µbump
  - Heat sink



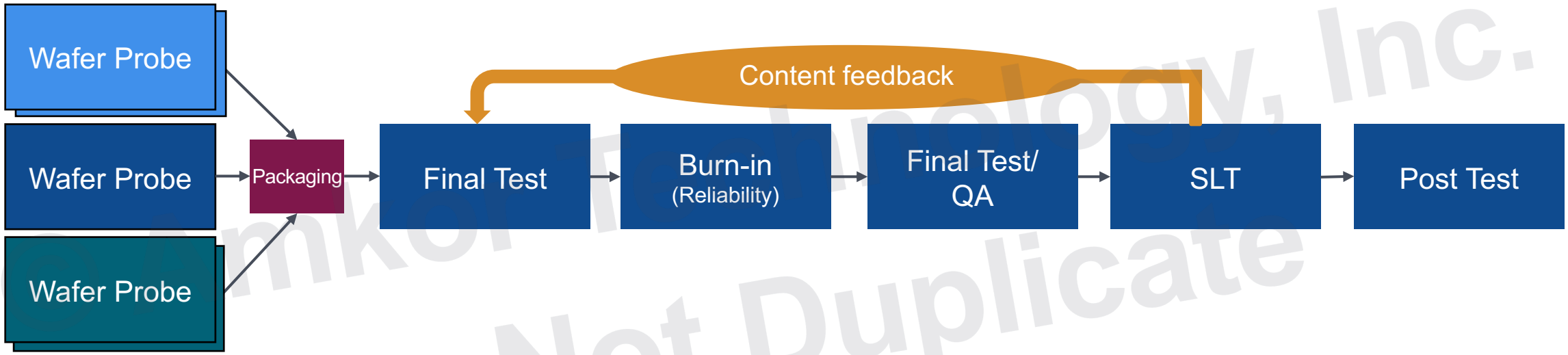
UCIe Test Methods – Automotive Scaling

- Latency
- Data width
- Data rate
- BER
- Channel reach
- Bump pitches
- Power efficiency
- Bandwidth density
- Data lane swing
- Clock skew
- Impedance
- Total jitter
- Lane-to-lane skew
- Rise time, fall time, crosstalk
- Reliability

3D Chiplet Stack Topologies Continue to Impact the Test Ecosystems

Source: UCIexpress.org. UCIe is trademark Universal Chiplet Interconnect Express

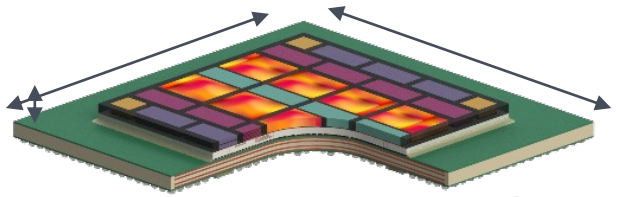
Advanced Packaging Production Test Flow

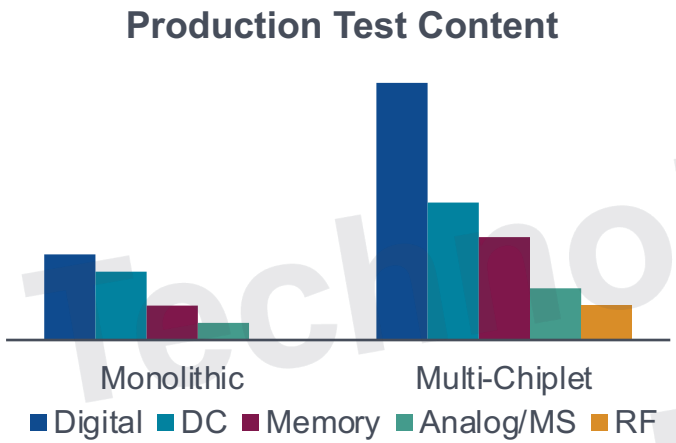


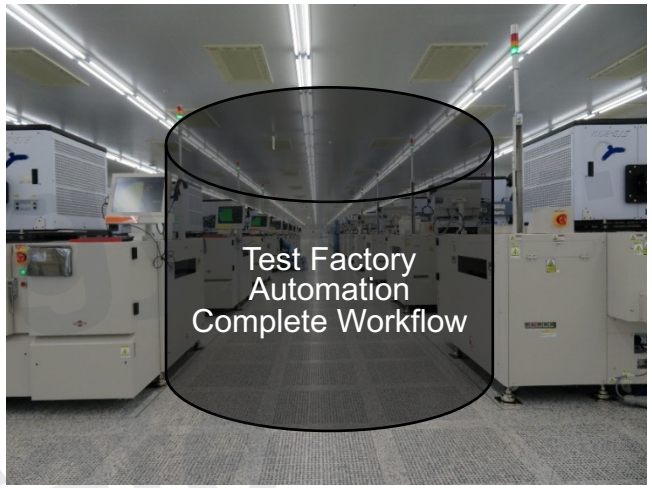
Alter Test Flow **Test Content Re-distribution** **Platform Level Test Quality**

Advanced Packaging Production Test Ecosystem

Architecture, Design, Development & Deployment







Package Handler

- Physical characteristics
- Thermal designs
- Production economics

Post-Pkg Test Equip Req's

- Increased content
- Enhanced performance
- Enhanced test scope due to multi-functional DUT blocks for each test insertion

Enhanced Data Automation

- Unit Level Traceability (ULT)
- Data feed forward
- Retest
- Design feedback

Test Equipment Suppliers May Need to Help With Coverage & Mfg Simplification

Summary

- Multi-die packages allow for denser integration
- Multi-die packages with 2D & 3D variations results in performance benefits, while adding complexities
- Business continues to have economic and performance challenges
- Amkor is the industry leader in advanced packaging and production test solutions

Amkor Test Services

24/7

Operation of fully networked test floors

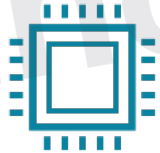
Test Development

Software & hardware for probe, strip, final and system level test

Full End-of-Line Processing

Bake, scan, pack, ship and finished good services

Tested Annually



>9 Billion units
>1.8 Million wafers

Accurate and Thorough Test Services

Wafer probe, final test, strip test, film frame test, system level test, opens/shorts test, burn-in and complete end-of-line

Testing For Commercial, Industrial & Automotive Devices

Discrete, power, mixed-signal, memory, RF, MEMS and SiP devices

>3600 Testers in 7 Locations

3000+ Amkor,
600+ consigned

ENABLING the FUTURE

Thank You

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