Heterogeneous Wafer Level Technologies for Chiplet Integration

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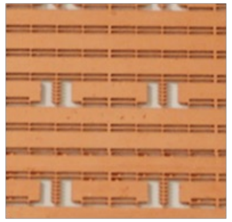
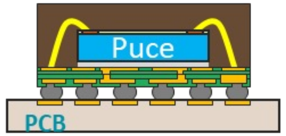
From classical to “advanced” packaging

• <2010
Packaging considered a menial task
Die → package → board → system

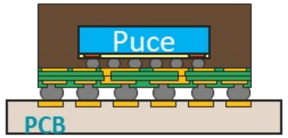


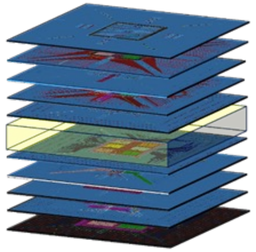
Cu Leadframe

Wire bonding

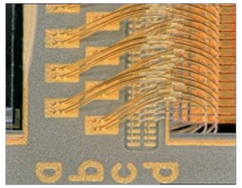


« Flip-chip »

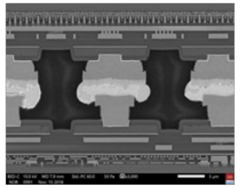




Laminated substrate

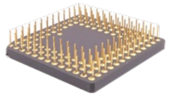


Wire bonds

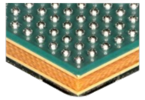


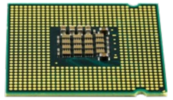
Micro-pillars

DIP, PGA

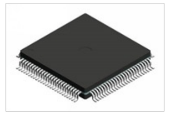


BGA/LGA

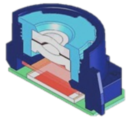




QFP/QFN

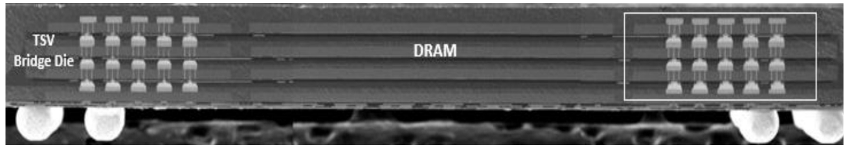


Specific

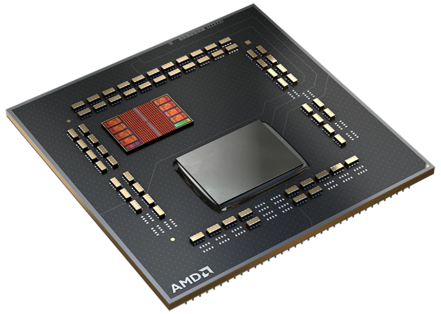


• >2010
Packaging as a driver for innovation
System in package (SiP) technologies

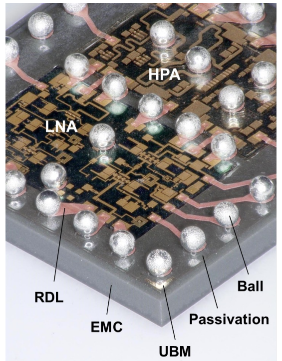
SiP Apple Watch 1

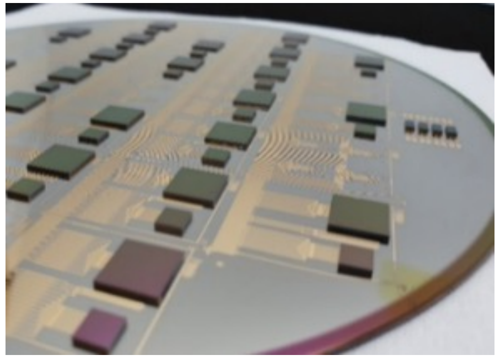


Hynix Integrated Fan-out Memory (HIFOM)



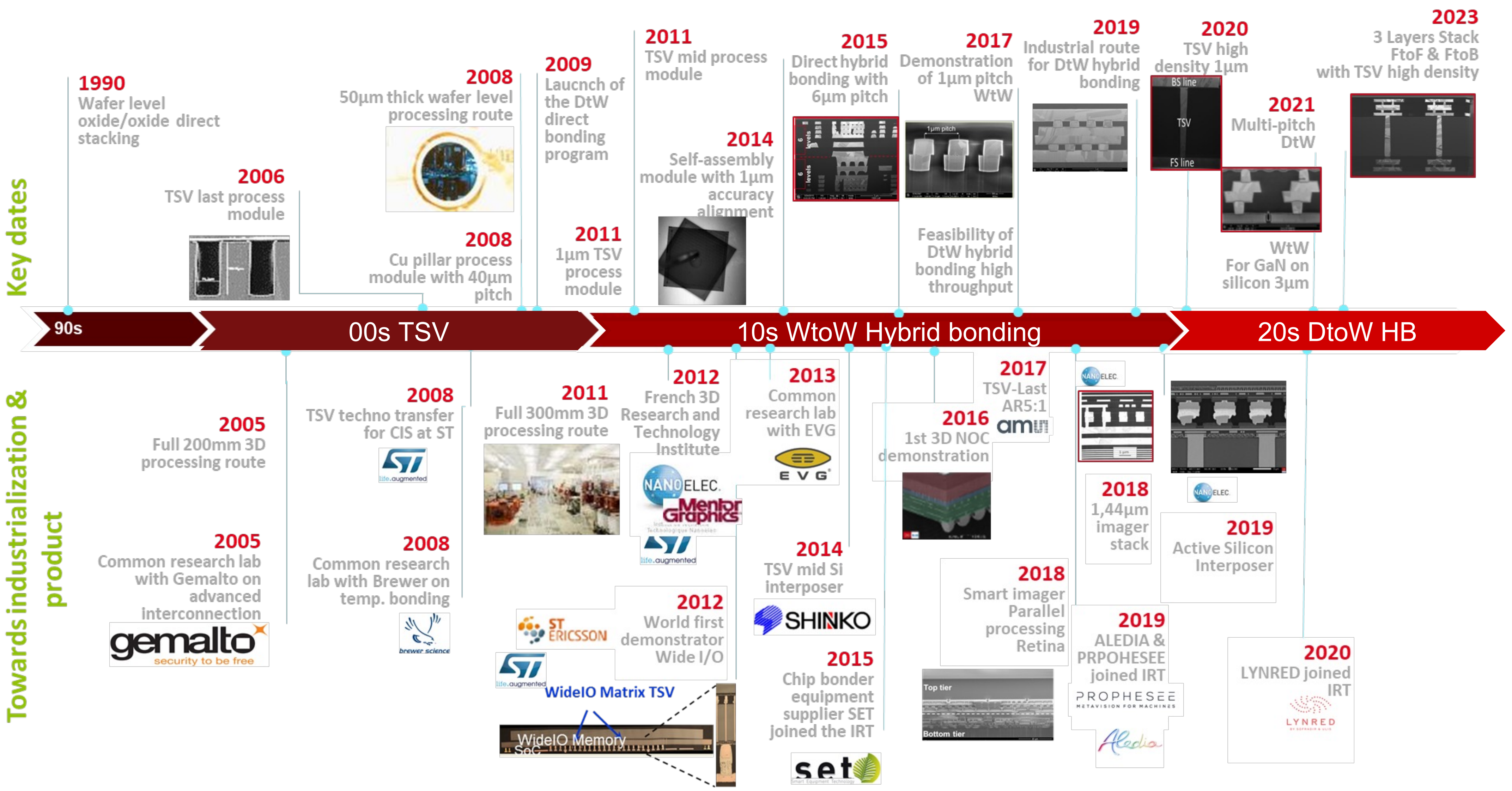
AMD 3D V-cache





« Wafer-level » packaging

3D @ LETI: KEY MILESTONES



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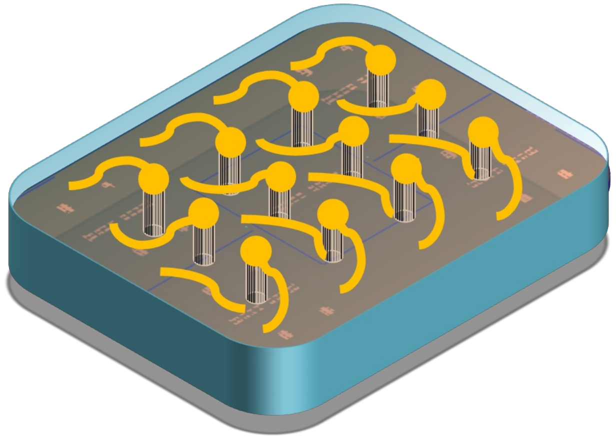
MORPHOLOGY OF A 3D CIRCUIT

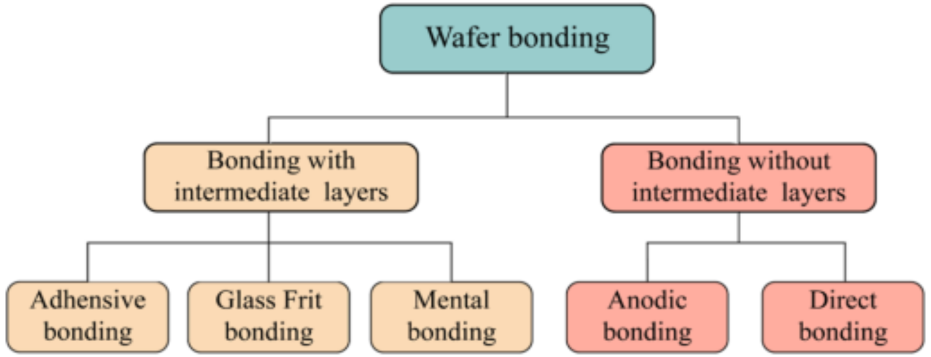
- **Thin stacked layers**
  Layer 1 (# bottom die) / (…) / Layer N (# top die)
  Can be as thin as a few µm or less
- **Layer-to-layer vertical interconnects**
  Heart of 3D density

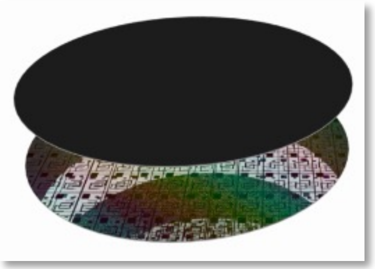
- **Intra-layer vertical interconnects**
  Communication between frontside and backside of each layers
  Through silicon Vias (TSV), through glass vias (TGV), …
- **Intra-layer in-plane interconnects (2D)**
  ReDistribution Layers (RDL)

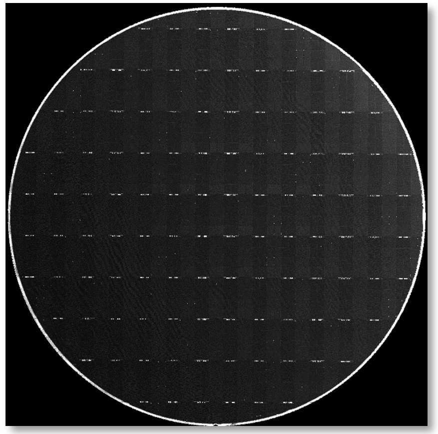


WAFER-TO-WAFER BONDING TECHNIQUES

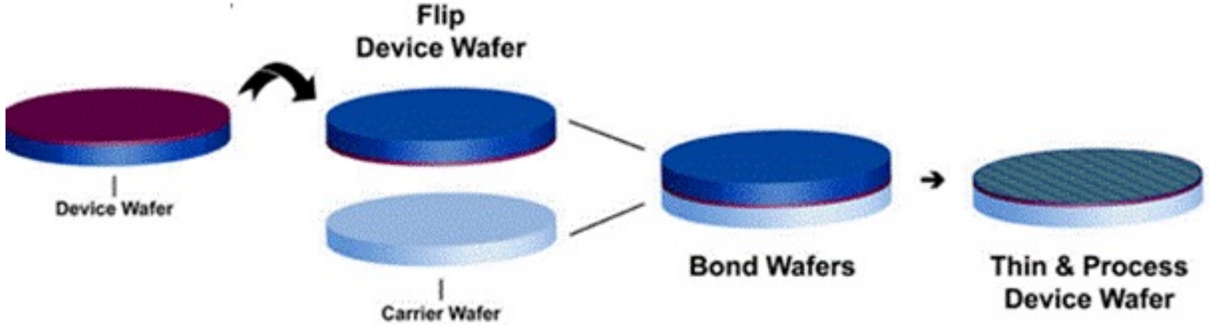
- **Thin wafer processing (<50µm)**
  Thinning and subsequent process of thin wafers requires prior bonding to a mechanical carrier
- **Temporary bonding**
  Can be achieved by polymer bonding, or direct bonding with weak adhesion forces on purpose
  May include a non-sticky part on the surface
- **Debonding**
  Chemical dissolution, Thermal release, UV laser degradation

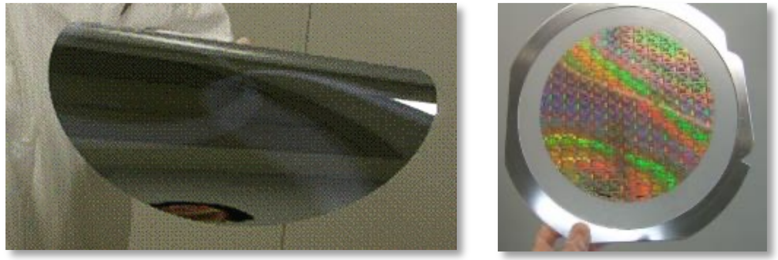






Scanning acoustic microscopy



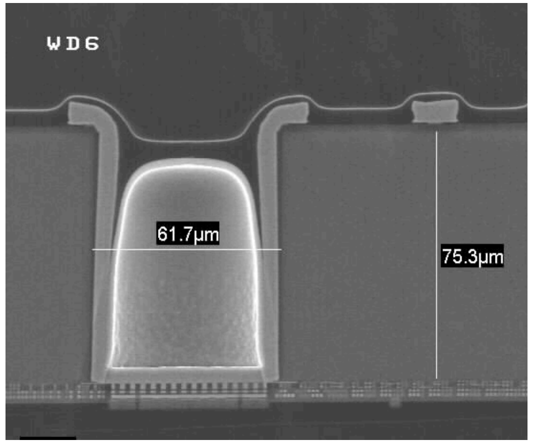


50 µm thin silicon wafers

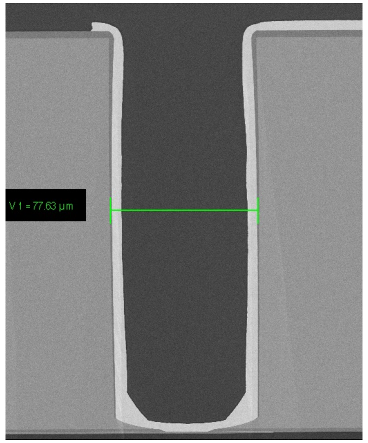
THROUGH SILICON VIA (TSV) TECHNOLOGIES

- **Through silicon via realized <u>after</u> circuit processing***

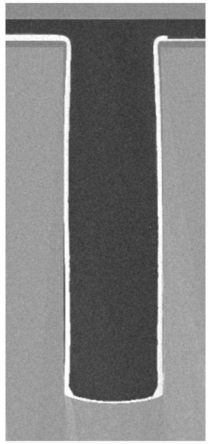
Industrially mature since 2008



AR 1,2 after passivation



AR 2,5 after RDL



AR 3,7

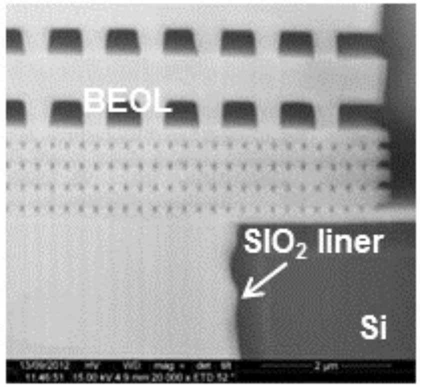
AR = Aspect Ratio = height/diameter

*D. Henry et al., ECTC 2008

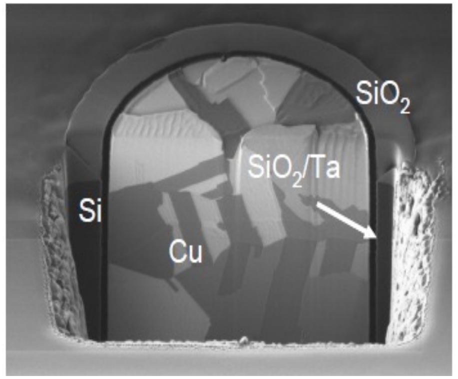
**P. Coudrain et al., EPTC 2012

- **Through silicon via is realized during circuit processing****

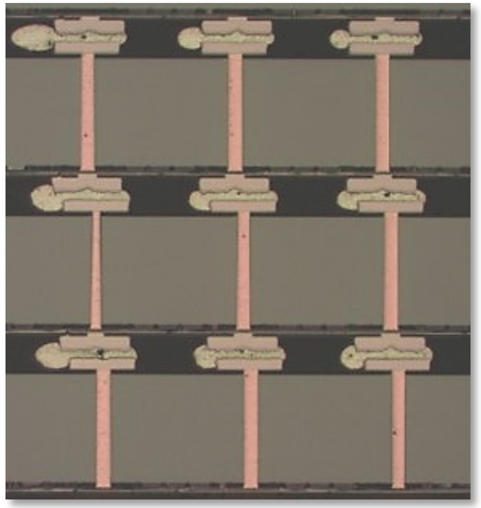
Industrially mature since 2013



TSV & CMOS back end of line

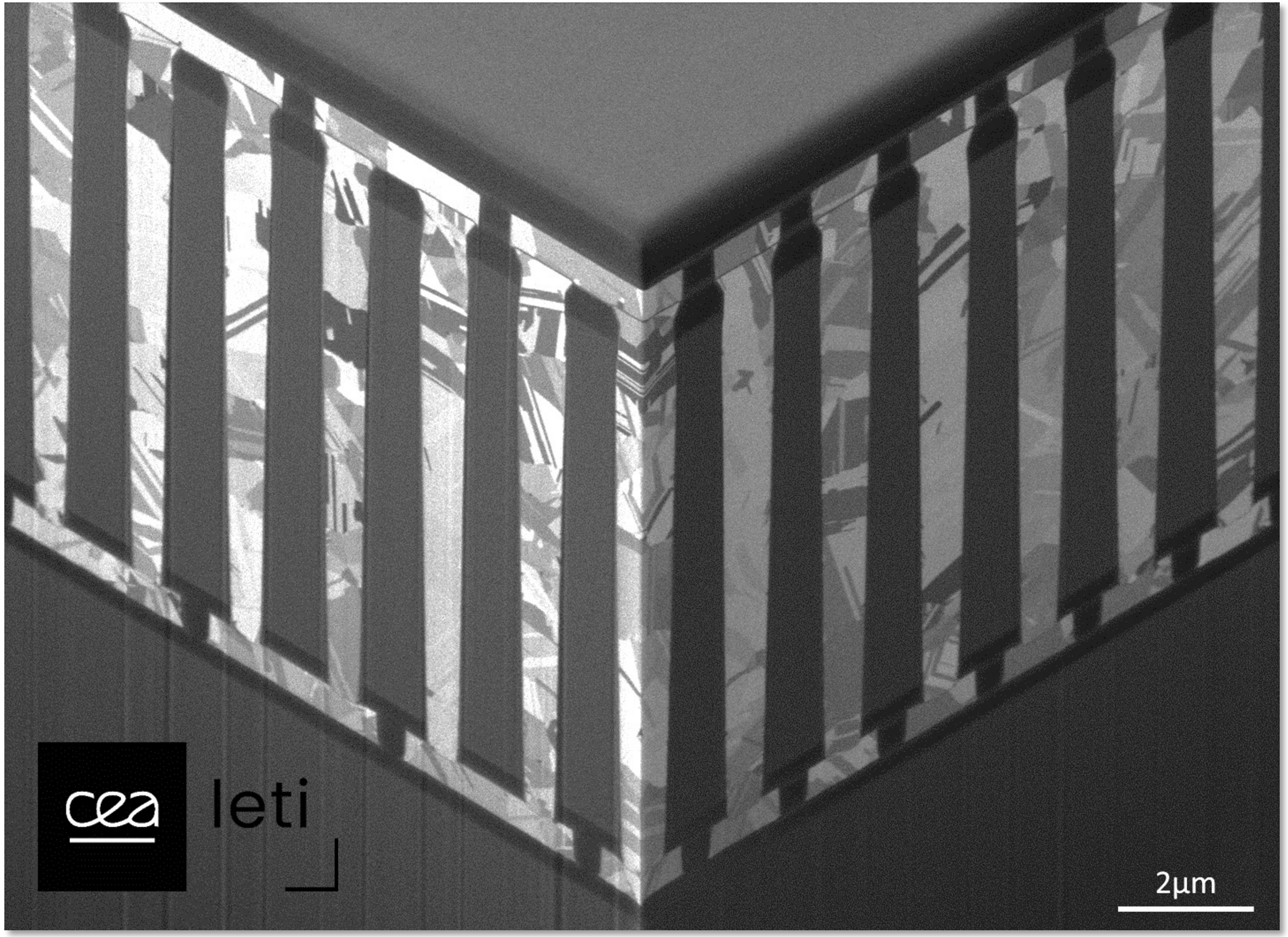


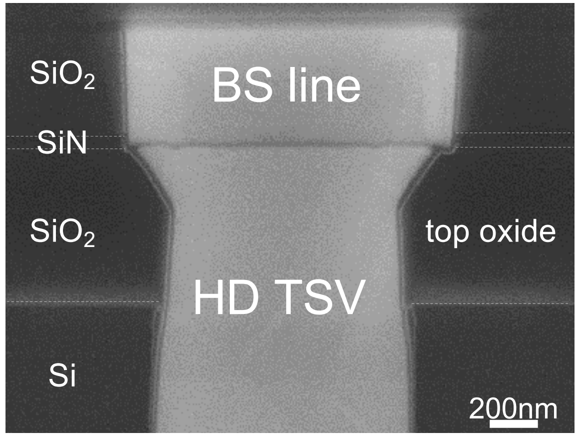
TSV structure

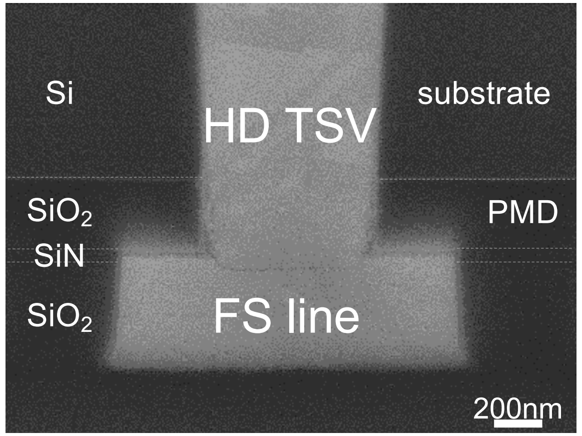


64Gb DDR4 DRAM 3D,
Samsung (2015)

High density TSV – in progress

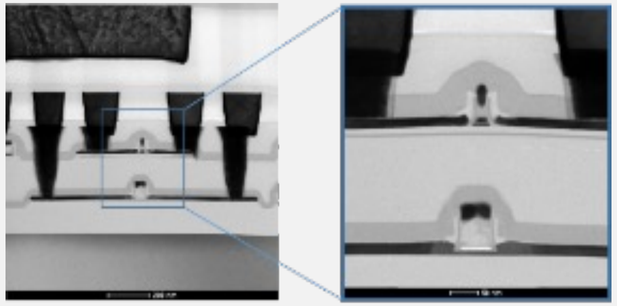
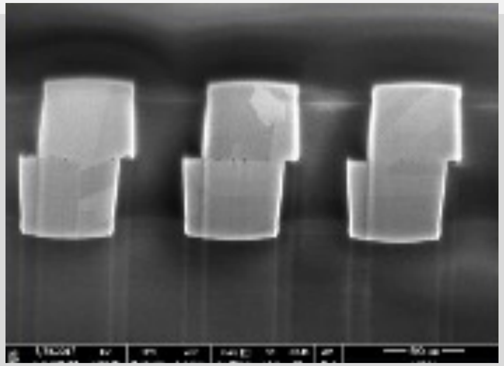
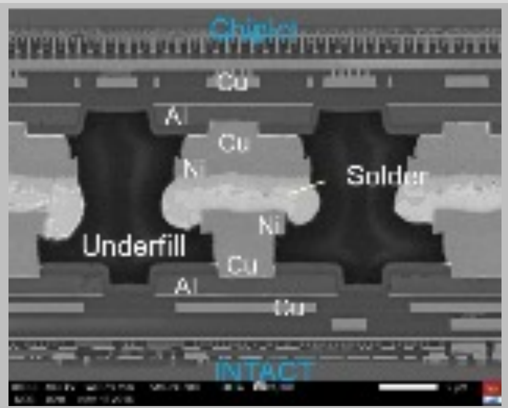






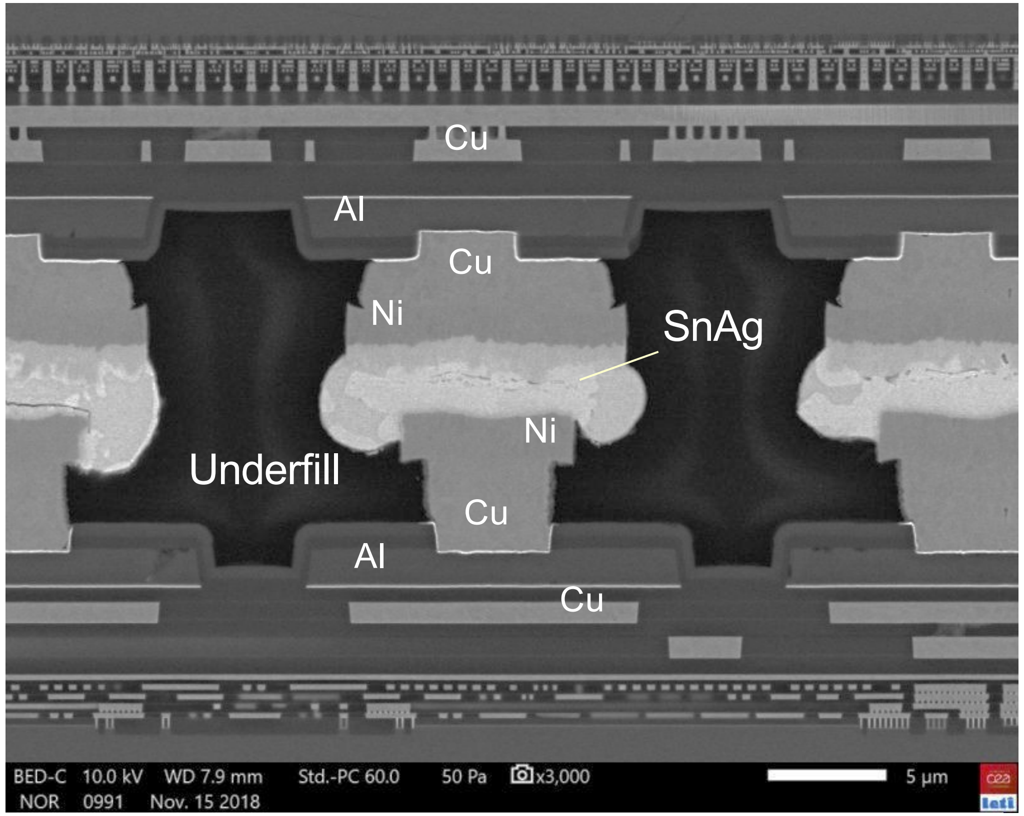
S. Borel et al., Electronic Components and Technology Conference, 2023

TECHNOLOGIES FOR 3D INTERCONNECTS

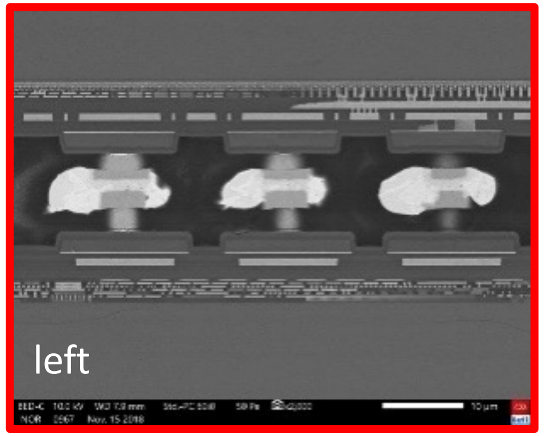
Interconnect pitch				
<100nm	Sequential 3D		10^8 cont./mm^2 Transistor level	**Wafer to Wafer**
100nm-10µm	Hybrid bonding		10^6 cont./mm^2 Logic-block level	**Die to Wafer** **Wafer to Wafer**
> 10µm	Metal & adhesive bonding		10^3 cont./mm^2 Circuit level	**Die to Die** **Die to Wafer** **Wafer to Wafer**

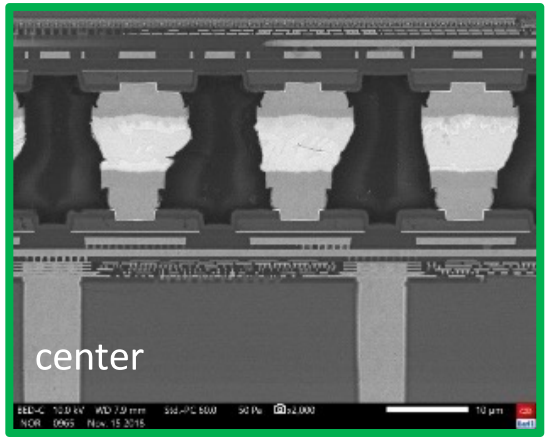
MICROBUMPS / PILLARS ASSEMBLY

- **Industrial state of the art: 20µm pitch**
- **Thermo-compression with parallelism optimization**



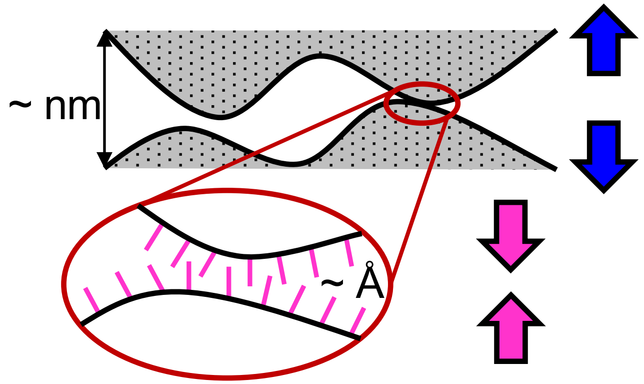
P. Coudrain et al., Electronic Components & Technology Conference, 2019





Assembly without proper parallelism tuning: non-homogeneous soldering along the die

DIRECT BONDING PRINCIPLE

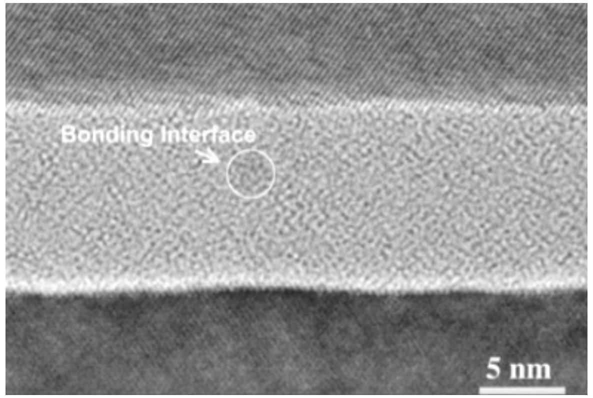


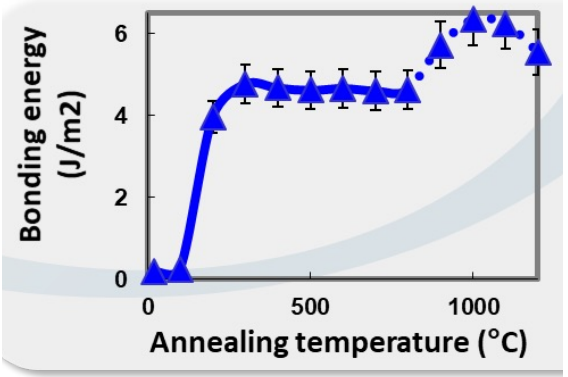
- **Bonding without adding material**
  Based on the attraction of very smooth surfaces
  CMP is the key process for this process

- **SiO_2/SiO_2 bonding**
  Required roughness < 0,65nm rms [1,2]
  Van der Waals interaction after bonding at T_{amb}
  Siloxane covalent bonds formed after annealing

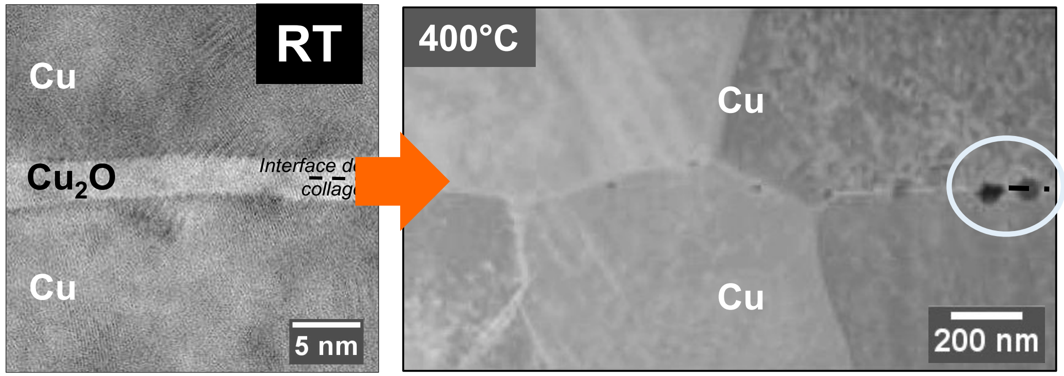
- **Cu/Cu bonding**
  Required roughness < 0,5nm rms [1,2]
  Cu recrystallization during annealing > 200°C [3,4,5]

[1] F. Rieutord, et al. *ECS Trans.,* vol. 3, no. 6, pp. 205–215, 2006
[2] H. Moriceau, *Microelectronics Reliability*, vol. 52, no. 2, pp. 331–341, 2012
[3] L. Di Cioccio, et al., *J. Electrochem. Soc.,* vol. 158, no. 6, pp. P81–P86, 2011





SiO_2/SiO_2 interface after anneal

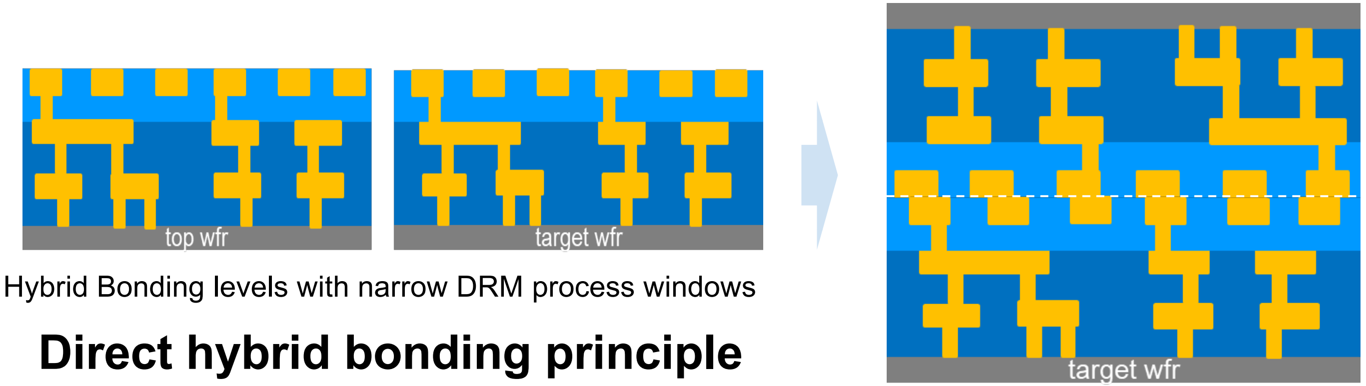


[4] P. Gonchardon et al., *ECS Trans.*, pp. 357-367, 2014
[5] S. Moreau et al., Proc. of ECTC, pp. 1940-1945, 2016

DIRECT HYBRID BONDING PROCESS: A HOT TOPIC !

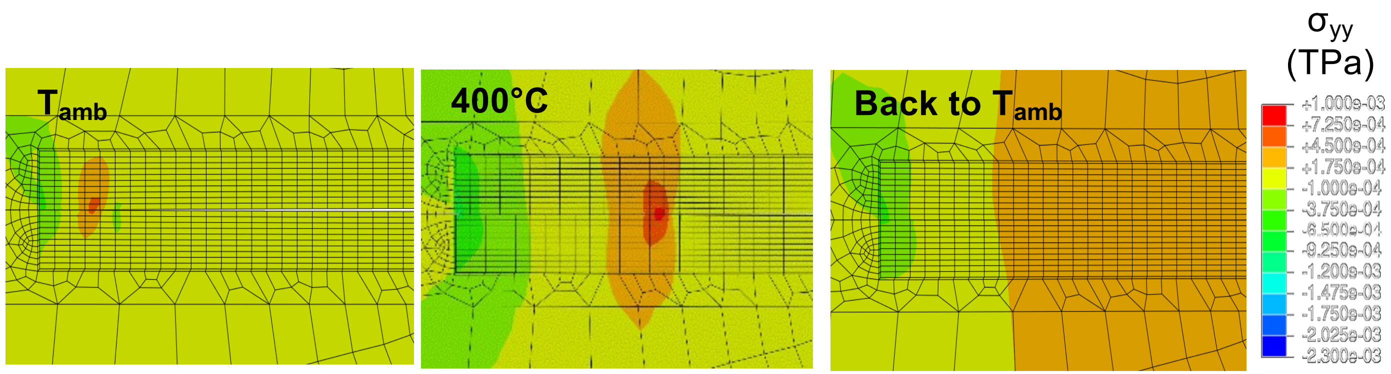
- **Mix of SiO_2/SiO_2 & Cu/Cu bonding**

- **Precautious CMP process**
  Cu etch rate > SiO_2 → dishing in Cu pads
  Cu interface closes during annealing
  Proper design rule manual

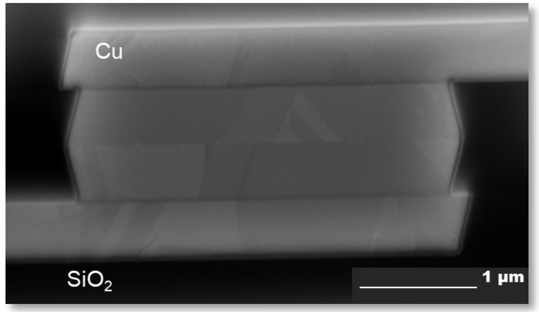


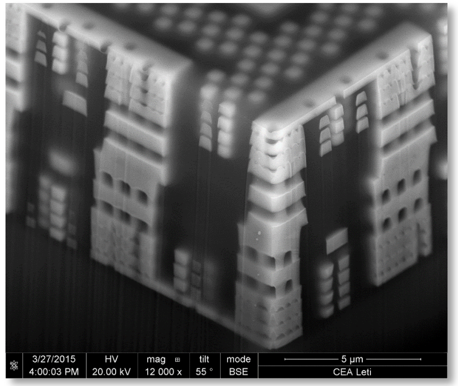
Hybrid Bonding levels with narrow DRM process windows

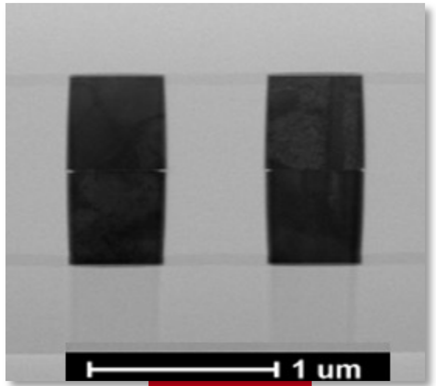
Direct hybrid bonding principle



Thermomechanical simulation of the bonding process

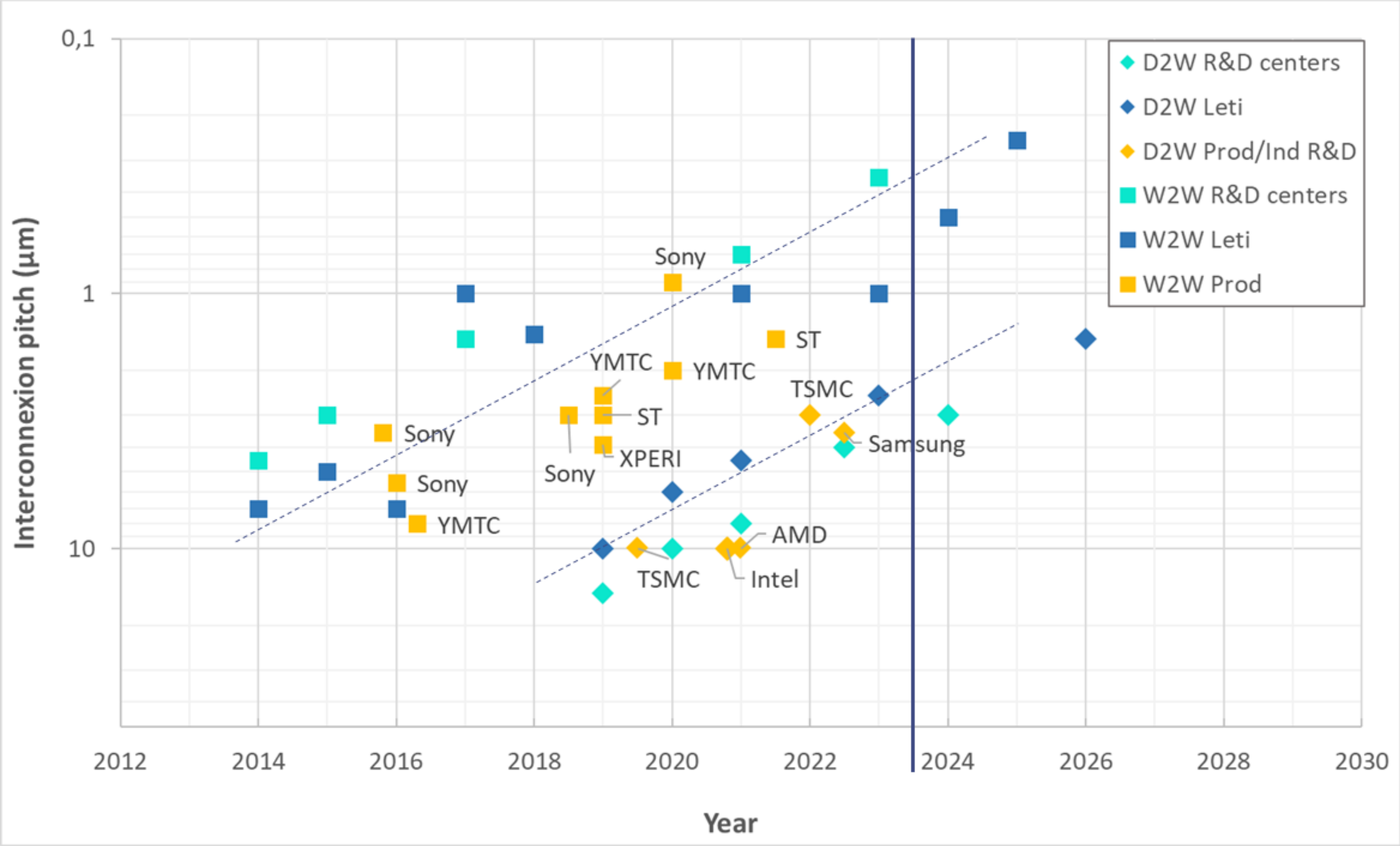




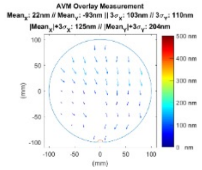


Y. Beilliard, PhD Thesis, Université Grenoble Alpes, 2015
Y. Beilliard et al., International Journal of Solids and Structures, Vol. 117, June 2017, pp. 208-220
S. Losthis et al., Proc. of ECTC, pp. 869-876, 2016
L. Millet et al., VLSI'2018 , JSSC'2019
J. Jourdon et al., IEDM 2018

HYBRID BONDING ROAD-MAP @ LETI

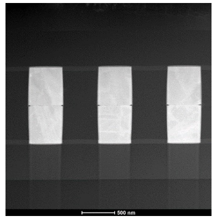
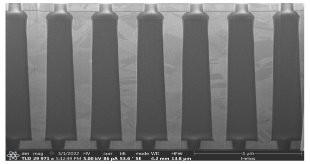
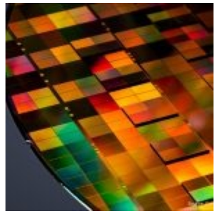


Placement accuracy from tool suppliers ≠ Alignment accuracy ≠ Pitch validated with full functional wafers connexion

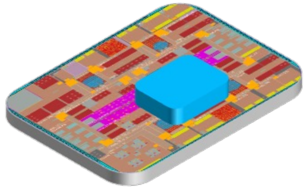


Our main developments drivers :

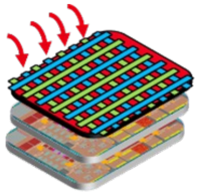
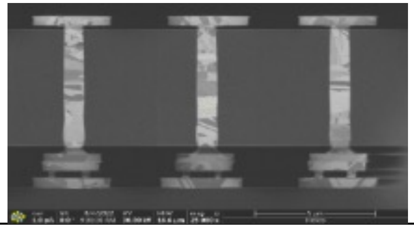
Performance : Innovative bonding process, Interconnection density increase, KGD strategy, High density TSV

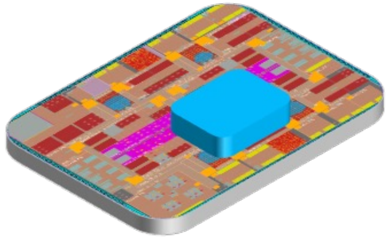





- **Heterogeneous 3D** : Adaptation to non-CMOS technologies, exotic material integration, Low temperature processes (200°C and below)

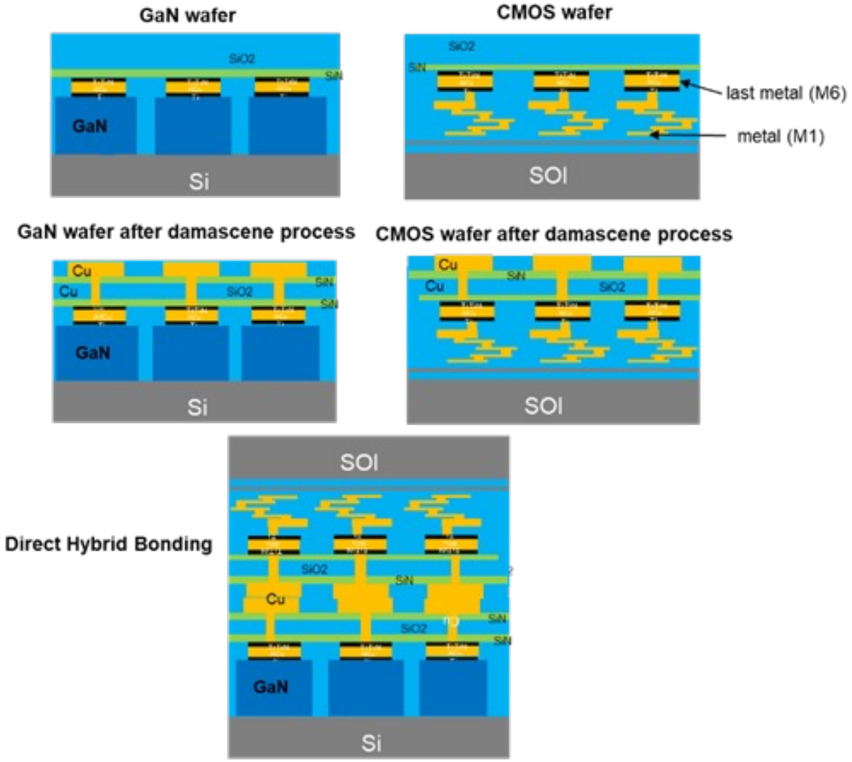


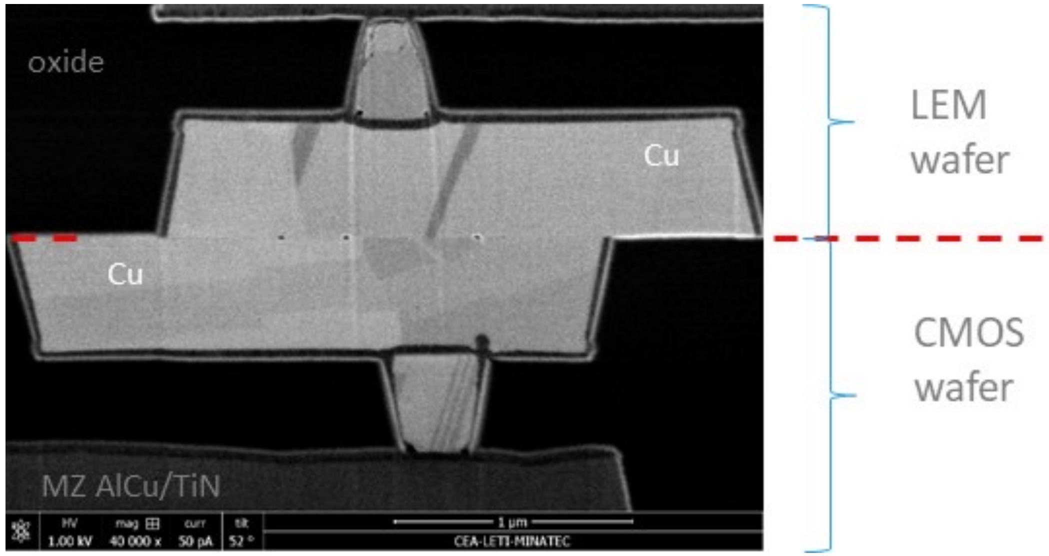

- **Architecture** : Multi-stacking layers , Chiplets on bottom die, Co-integration with Si interposer

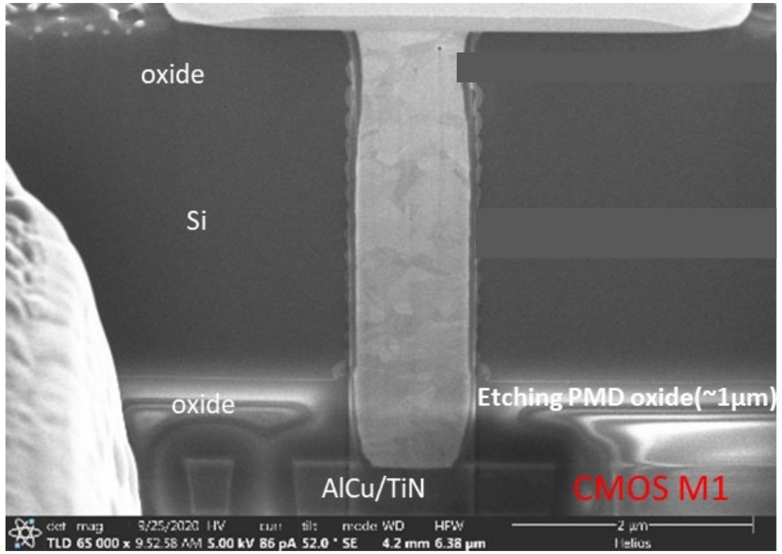






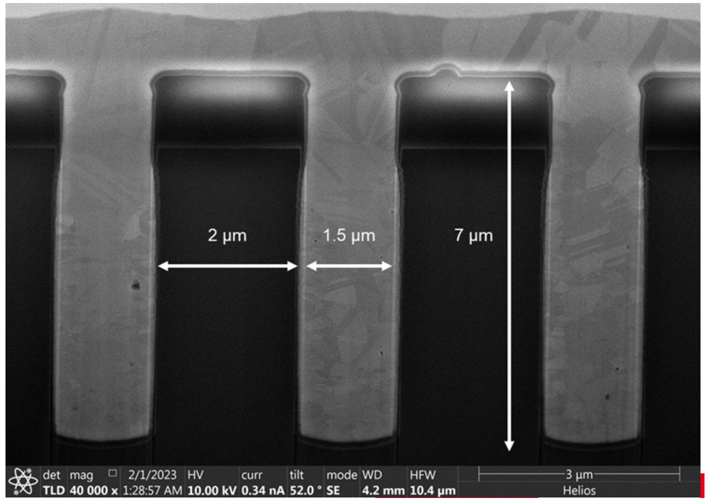
HETEROGENEOUS WAFER TO WAFER BONDING FOR DISPLAYS





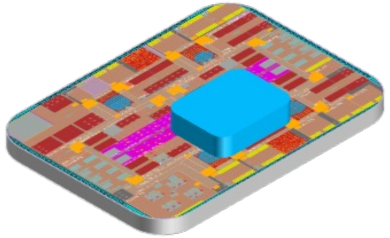


W2W process
HB 3 μm LED / CMOS
Interconnect TSV 1μm



@ 180°C : under development with dedicated damascene process or an redistribution layer (RDL) process for routing

200mm integration of TSV HD Ø1.5 μm / H 7 μm



HYBRID BONDING FOR FUTURE RF APPLICATIONS

Finest pitch and shortest length for interconnections

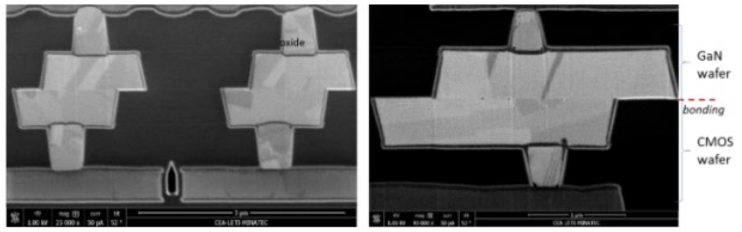


Fig. 3. FIB-SEM X-section of Copper /silicon oxide hybrid bonding area for 3 and 5 µm pitch

C. Dubarry et al., 3DIC 2021

- Few tens of IOs to connect
- Better signal propagation @ very high frequencies (> 100GHz, mmW, sub-THz)
- Interface with tiny and high performance devices (III-V/II-VI active devices)

RF chiplet Enabler

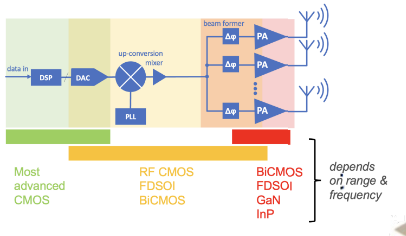
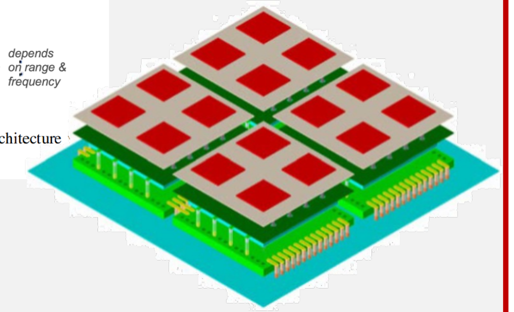


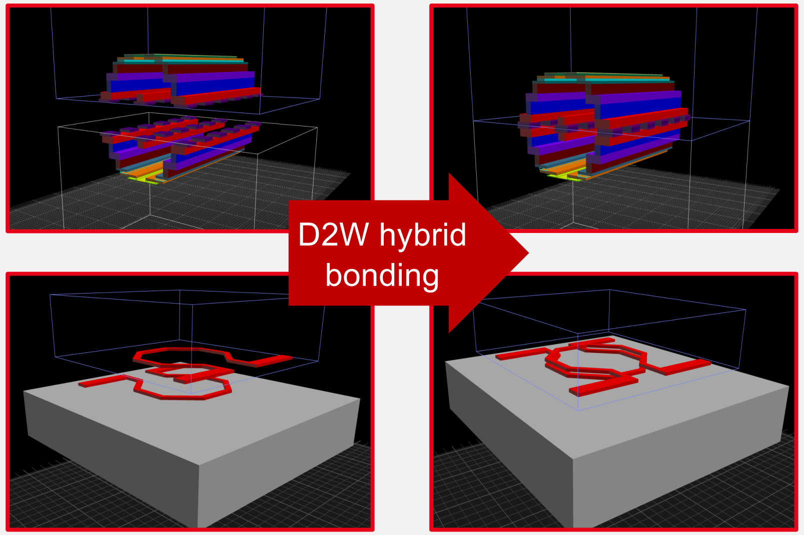
Fig. 3: Typical mmwave beamforming transmitter architecture technology partitioning.



D. Belot et al., EuCNC 2022

- Array based Front End Modules and antennas for beam forming (6G)
- Better thermal dissipation possibilities
- Reduced BOM and costs (III-V / II-VI materials)

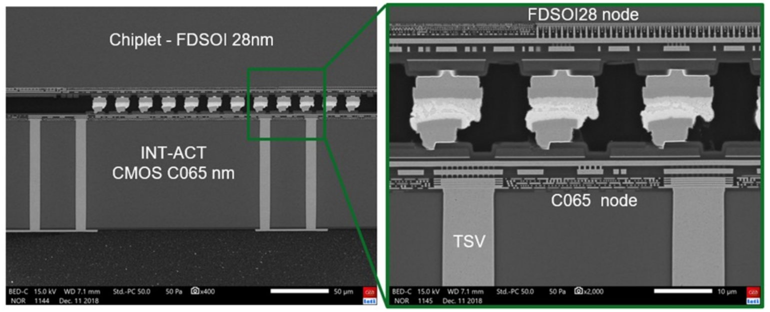
Expected results



- Die to wafer hybrid bonding with 3 x 3 mm² top chip
- 3D transmission lines & passives devices to be measured up to 325GHz

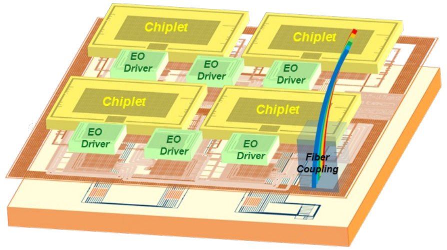
ADVANCED 3D INTEGRATION

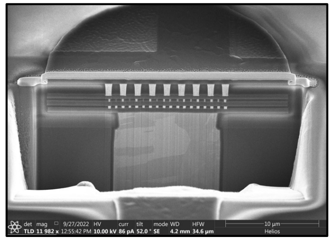
INTACT
HPC chiplet enabler

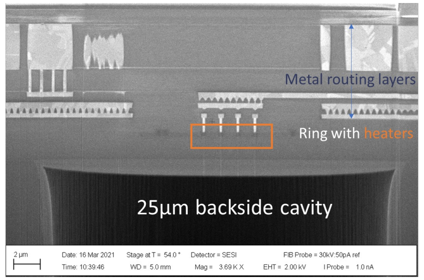


6 chiplets (FDSOI 28nm) 3D-stacked on an **active interposer** (CMOS 65nm)

POPSTAR
Photonic chiplet enabler

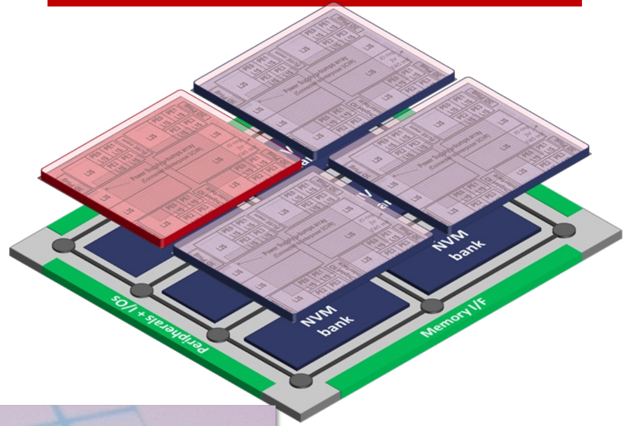


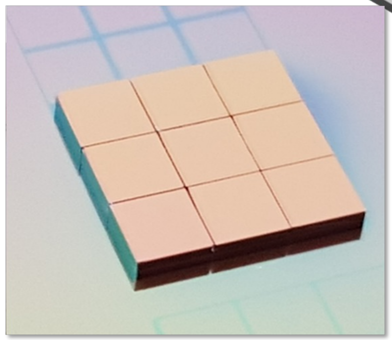


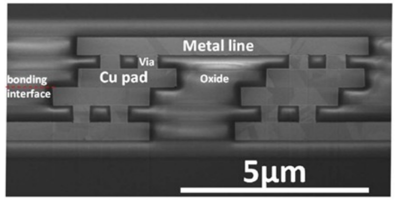


4 chiplets (FDSOI 28nm) & E/O chiplets 3D-stacked on a **photonic interposer** (ONoC)

Generative AI at edge chiplet enabler







Hybrid bonding die to wafer key enabling technology for **high I/O density**

LETI'S ECO-SYSTEM FOR 3D INTEGRATION

Industrial partners

Aledia Innovative displays, LYNRED, amu, Radiall, PROPHESEE METAVISION FOR MACHINES, SteerLight, intel, ST life.augmented, Valeo, MBDA MISSILE SYSTEMS, aryballe, muRata INNOVATOR IN ELECTRONICS, soitec

Service

CERN, tronics microsystems, Direct Conversion Empowered X-RAY Imaging, THALES

R&D partnership

C2MI Réinventer l'innovation, SIEMENS

CEA Labs (architecture, design)

cea leti

Technological Platform : Equipments & process

Equipment suppliers

KLA, unity SC, APPLIED MATERIALS, Lam RESEARCH, EVG, PROFACTOR, set Smart Equipment Technology, Besi

- **Growing eco-system** with applications calling for Advanced packaging & Die-to-Wafer hybrid bonding such as **embedded systems** for autonomous vehicle.
- **New partnerships** to get an highly accurate full **mature processes**
- CEA-Leti has a strong 3D integration & packaging background, working on all challenges in **collaboration with users & equipment providers**