CHIPLET SUMMIT
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ChipletSummit.com

Known Good Die Enables Advanced Packaging & Chiplet Manufacturing

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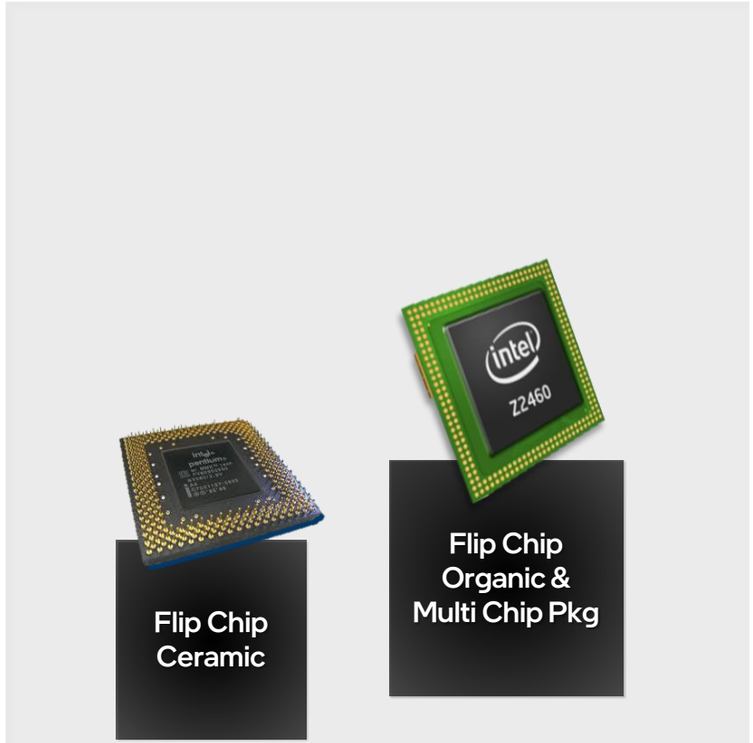
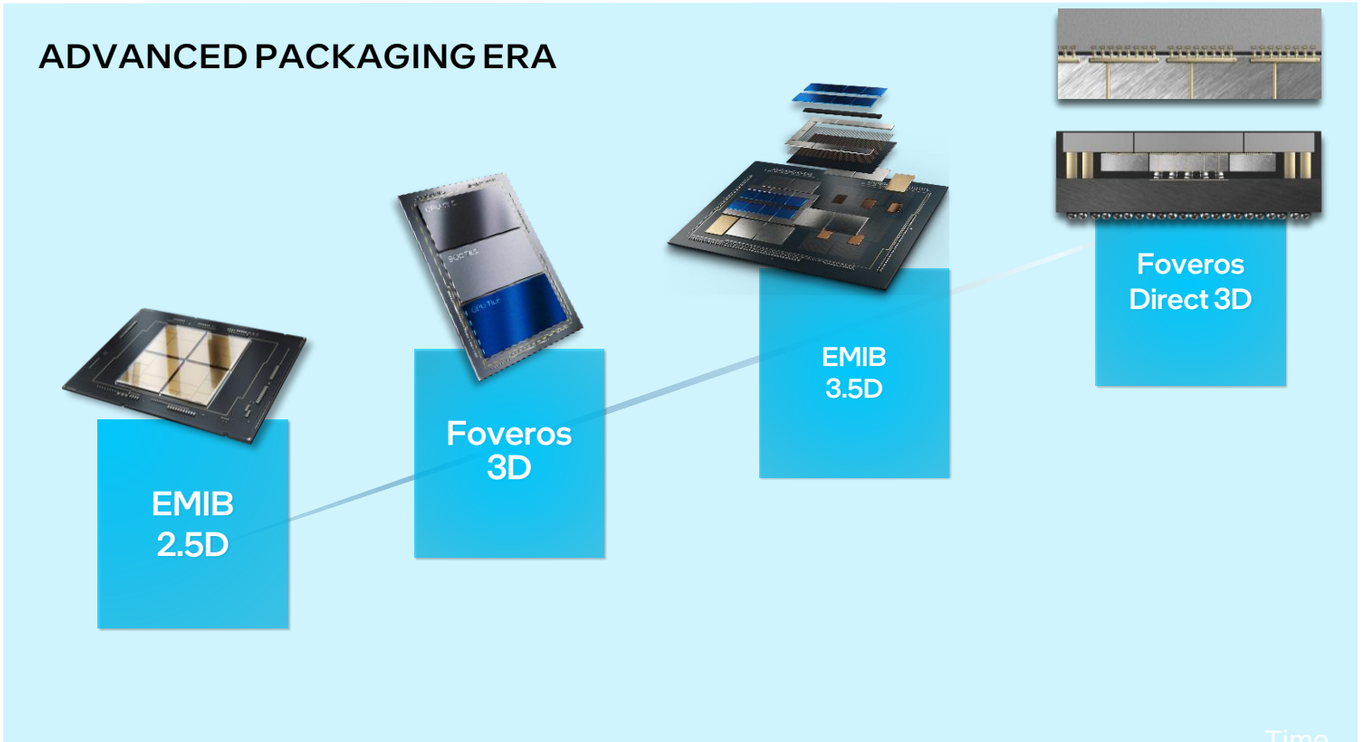
TD Foundry, Intel Foundry

Agenda

- Advanced Packaging Trend
- Known Good Die in chiplet era
- Die Sort capability at Intel Foundry
- Summary

Intel Foundry Package Technology – Expansive Ecosystem





Package main function:
provide power and signaling from motherboard to die

Added package value:
high density interconnects that enable larger die complexes from multiple process nodes

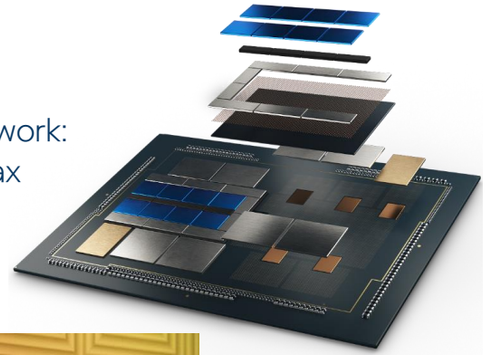
Chiplet Advantages & Challenges

Advantages

Moving from
System on Chip

To
System on Package

Modular Manufacturing at work:
Intel® Data Center GPU Max

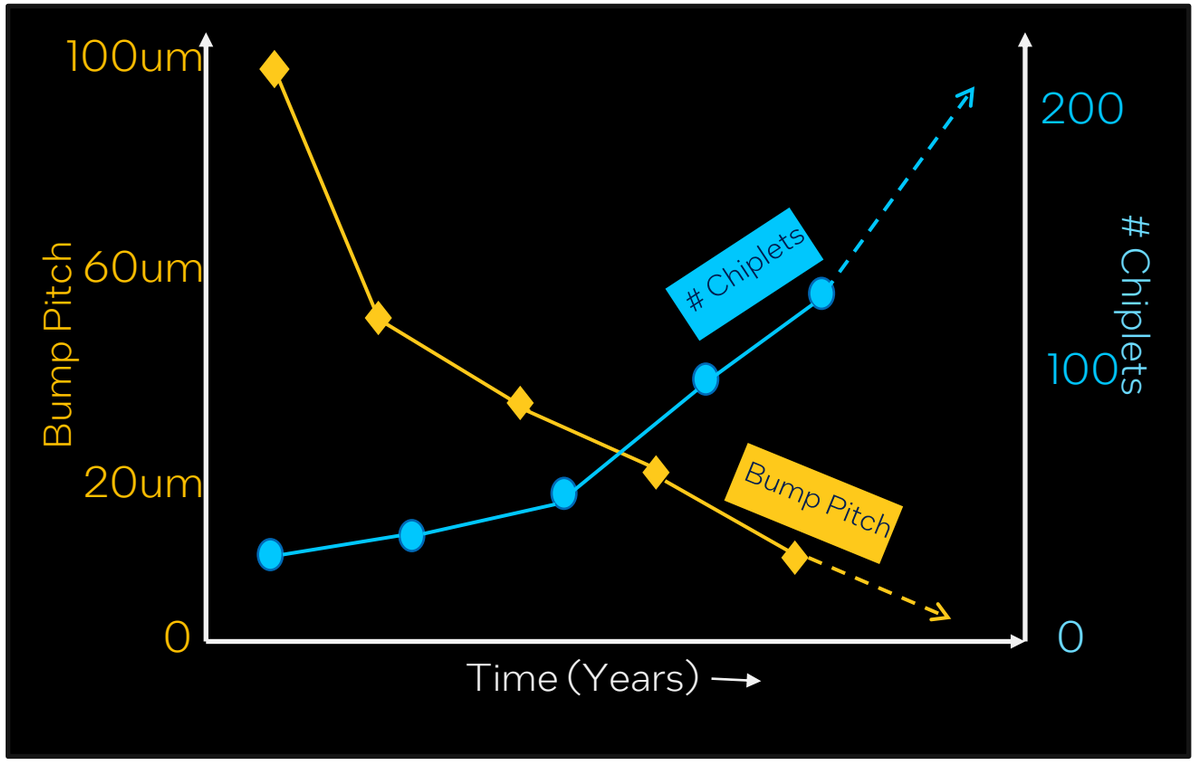


Manufacturing Challenges

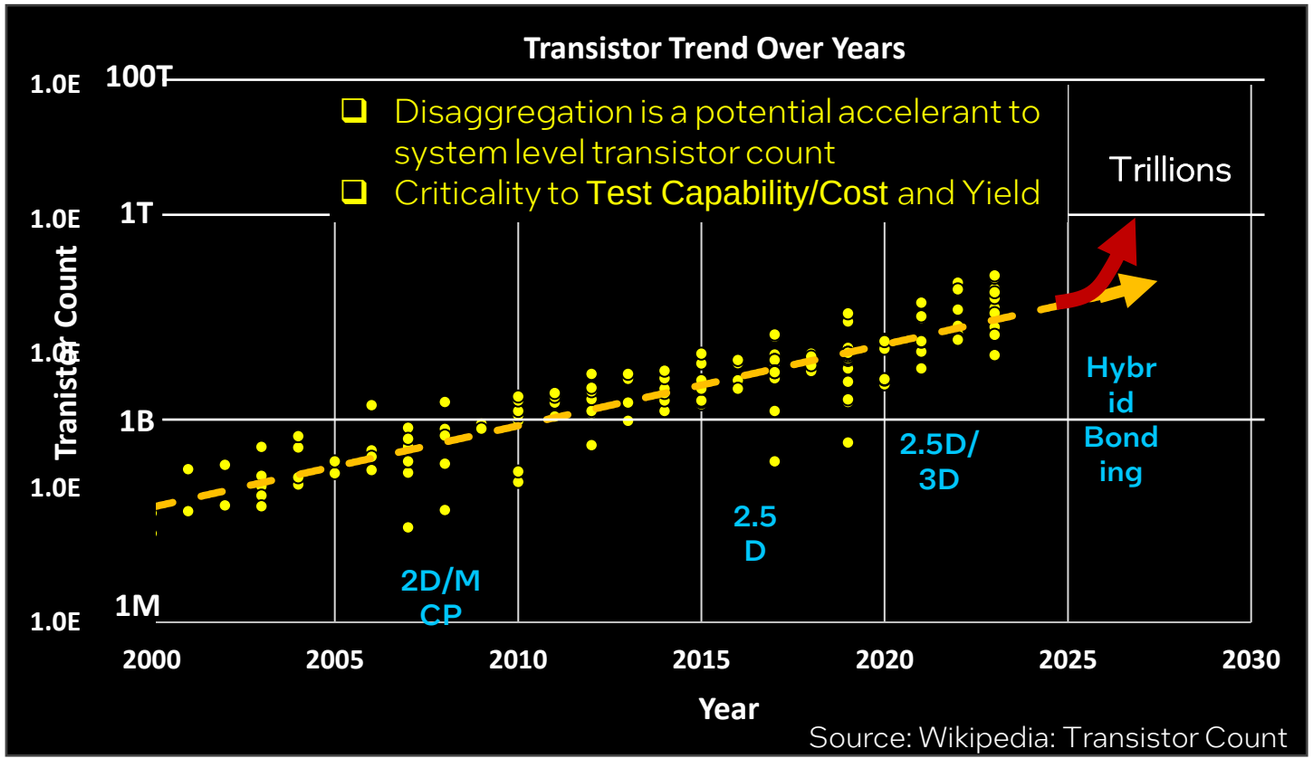
- Product Validation post chiplet re-integration,
  Are manufacturing screens needed
- Chiplet discrete reliability
- Integrated reliability
- MFG flow: Chip to wfr VS. wfr to wfr
- 3D stacking?
- Package architecture & memory integration
- Si Bump to bump connection;
- IO Si bump scaling
- Testing for interconnect quality/reliability

Scaling trends due to CHIPLETs

Chiplet count & integration complexity growing



Trending > 1Trillion transistors per package

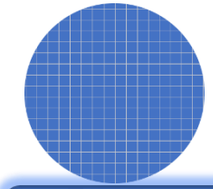


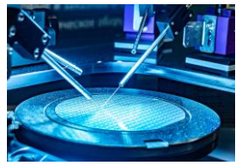
Advancements in Sort & test required to ensure cost effective solutions for manufacturing

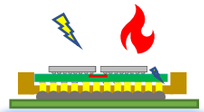
Importance of Sort/Test in Chiplet era

Typical Manufacturing Test flow

Single die in package:
Sort Missed screens linearly hit Package yields







Wafer Fabrication → Wafer Sort → Assembly → Burn-In → Final Test → SLT → Finish

Wafer Sort → Si Defects

Burn-In → Early Life Fails

Final Test → Electrical Defects

SLT → Electrical Defects

Sort designed to screen majority of silicon defects prior to package

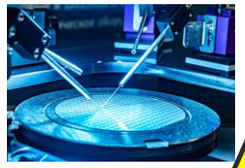
Burn-in designed to accelerate latent defects (voltage/temperature)

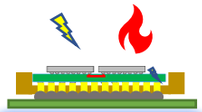
Final test screens fully-packaged units at use conditions (high temp, at use speed)

System level test (SLT) screens units for DPM-level defects using configurations similar to customer

Typical Manufacturing Test flow

TWO die in package:
Each die contributes to Si and Pkg losses for missed screens





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Wafer Sort → Si Defects

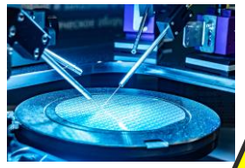
Burn-In → Early Life Fails

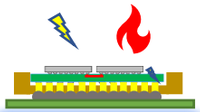
Final Test → Electrical Defects

SLT → Electrical Defects

Typical Manufacturing Test flow

Many die in package:
EXPONENTIAL LOSSES for Si and Pkg for missed screens





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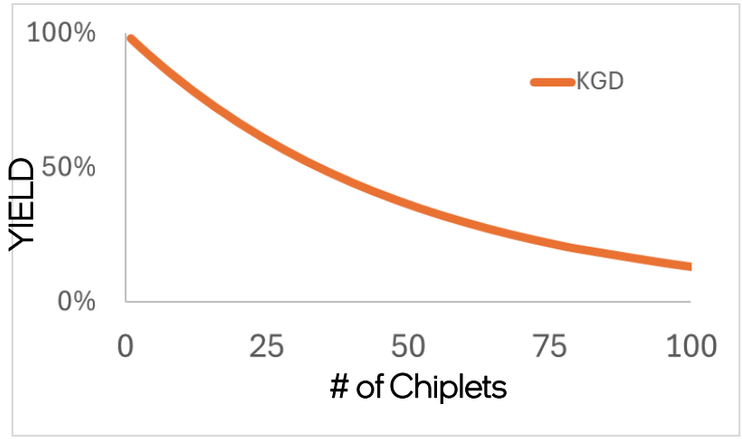


Evolution of Known Good Die

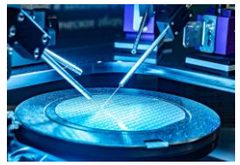
- Classic KGD:
  - Sort screens for die prior to packaging for defect & parametric issues in silicon
  - Include some electrical stress (as needed)
  - Wafer & die at fixed temp for screens, Tj varies by content/silicon variation

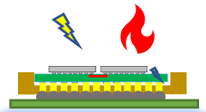
- Evolution of KGD to KGRD requires:
  - Expanded electrical & thermal stress (as needed)
  - Include Tj control for more effective parametric screens
  - Emulate final assembled & packaged product at the CHIPLET level

Chiplet & Adv Packaging requires Known Good & Reliable Die (KGRD)

Die Sort technology to enable KGRD

Intel Foundry's Die Sort Manufacturing Test flow





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Si Defects

Early Life Fails

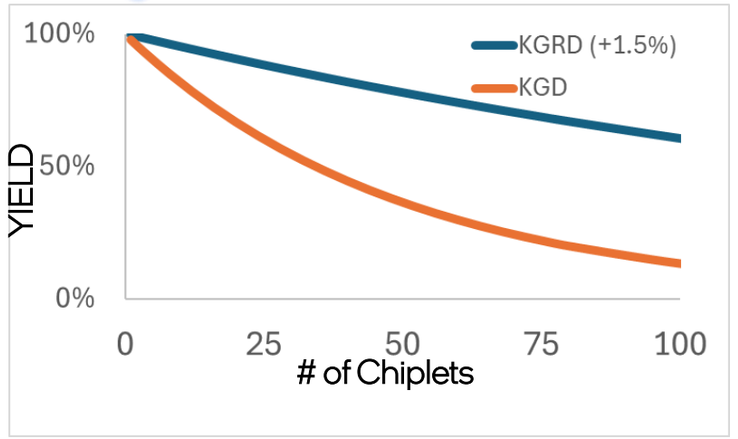
Electrical Defects

Electrical Defects

3D Stack

Singulate → Die Sort

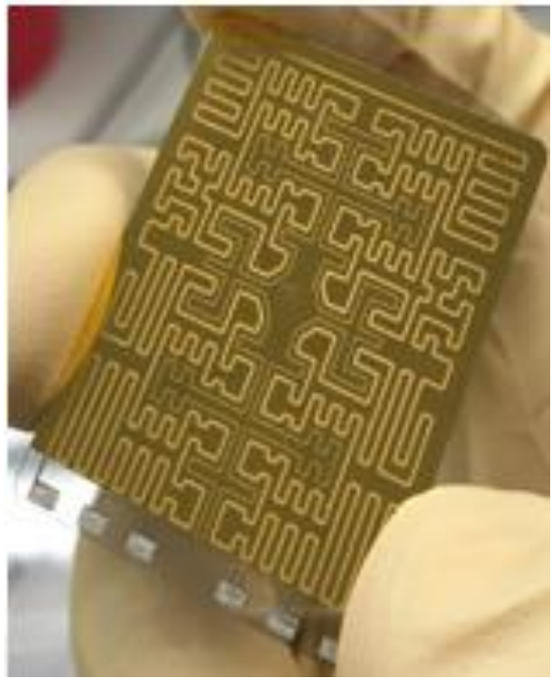
Package screens moved upstream



Intel Foundry's Die Sort solution delivers KGRD today

- Singulated Die Sort/Test (SDx) ensures only Known Good & Reliable Die survive to advanced packaging downstream manufacturing

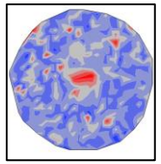
- What is SDx?
  - At its core, SDx is a novel thermal system which provides extreme thermal conductivity and response
  - Incorporates special die handling capability
  - SDx allows full final test (post-package) content and stress test at Sort (pre-package)
  - Based on Intel developed HDMT tester (High Density Modular Tester)

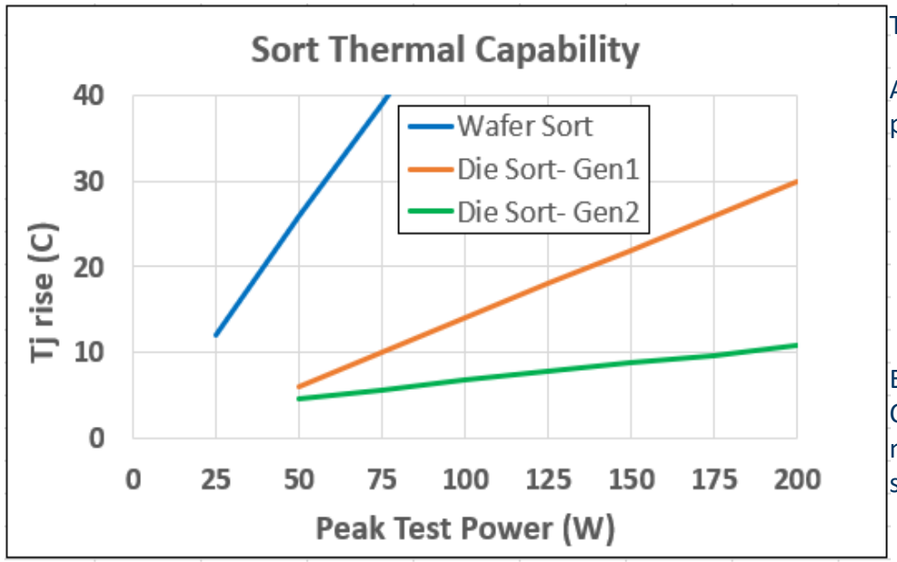


Intel Foundry's Die Sort solution delivers Thermal control at SORT

Best-in-class thermal capability

- 125C temp swing (cold to hot) in 1-2 secs
- >100x more effective thermal capability than wafer sort-based industry solutions





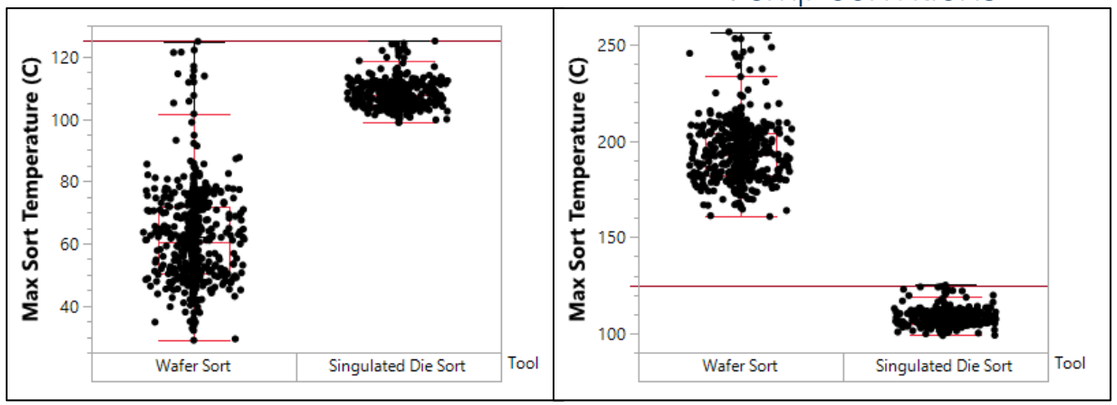
Tj rise =

Actual Temp – Set point

Example: Compute die (200 mm2) with hot spots

Optimize Max Temp based On distribution

Wafer sort set to Die Sort Temp conditions



Simulation on Tjrise comparing Wafer sort & Die Sort

SDx enables final test content & stress at Sort

- Enables KGRD screening with Tj control
- Enables efficient Stress deployment with Tj control
- Tests both singulated die and **singulated stacked die**

Intel Foundry Die Sort Factory

HDMT based SDx capability

Die Sort factory

Intel Foundry Die Sort solution to KGRD

- Chiplet & Adv Packaging is accelerating, here to stay & accelerating scaling
- Imperative to have Known Good & Reliable Die (KGRD) prior to Adv packaging
- Intel Foundry's Die Sort equipment & HDMT platform solution provide KGRD
- Cost effective solutions to deliver KGRD into complex products as important as ever

Thank you

Questions & Feedback: Patrick.j.Pisano@intel.com

Backup

Intel Foundry HDMT tester

- High Density Module Tester is another key component of Intel Sort/Test
  - Intel Foundry designed and manufactured test platform

Parameter	Capability
# Digital IO Channels	896 @1.5 Gpbs up to 2240 @ 2 Gpbs
# HC/LC DPS Channels	308 total independent resources (HC: 70, LC: 238) up to 484 total independent resources (HC: 110, LC: 374)
Vector Memory (per pin pattern depth)	4GV with 8x channel linking up to 4GV with bottomless
Simultaneous power to DUT (W)	1.3 kW up to 4.3 kW

HDMT Tester

Summary

- Modular/configurable/upgradable design
- Small footprint, competitive cost-of-test solution
- 12,000+ testers in deployment
  - >1,500 product test programs
- Use in Sort and package Test handler configurations
- SW & Instruments are configurable & capable