KEYSIGHT

KEYSIGHT

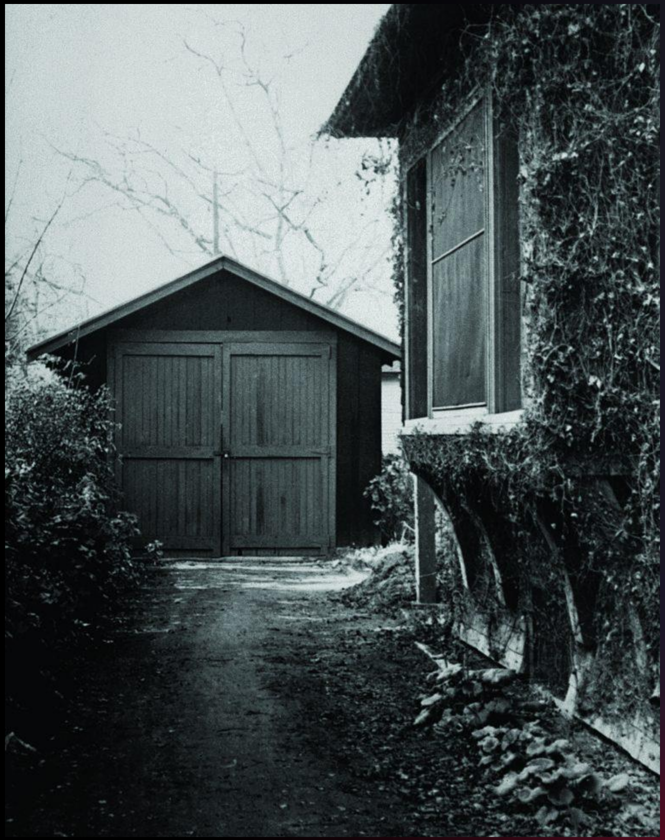
Using Design-to-Test Workflows and Managing the IP Lifecycle in Chiplet Designs

Nilesh Kamdar
General Manager, Keysight EDA

CHIPLET SUMMIT

January 21-23, 2025
Santa Clara Convention Center
ChipletSummit.com

The “oldest” 10-year startup in Silicon Valley



10 KEYSIGHT ANNIVERSARY

40-years of innovation in EDA

25 years at Keysight EDA
Partnerships & Collaboration

1

Simulating for Interoperability

2

Testing for Interoperability

3

Managing Chiplet Data

Future Predictions

KEYSIGHT

THEN

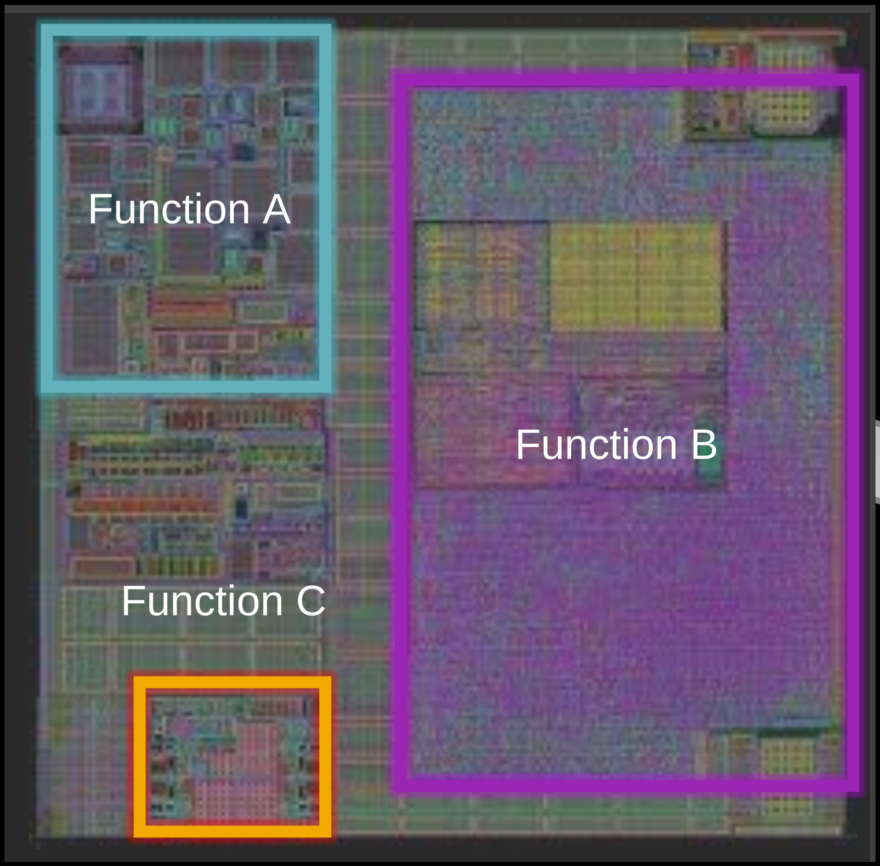
Single Vendor
Mainframe System

NOW

Multi-Vendor Ecosystems

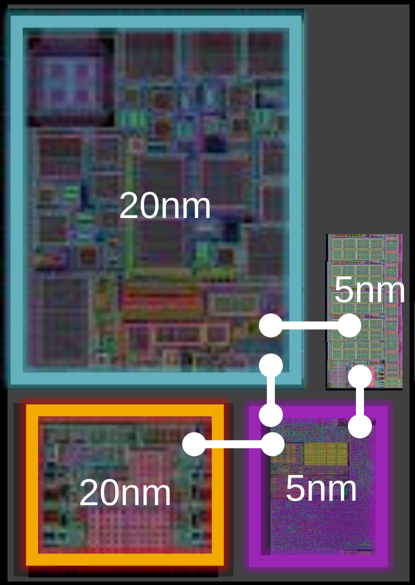
Some functions have a scaling advantage, some just add risk and engineering effort

Monolithic ASIC

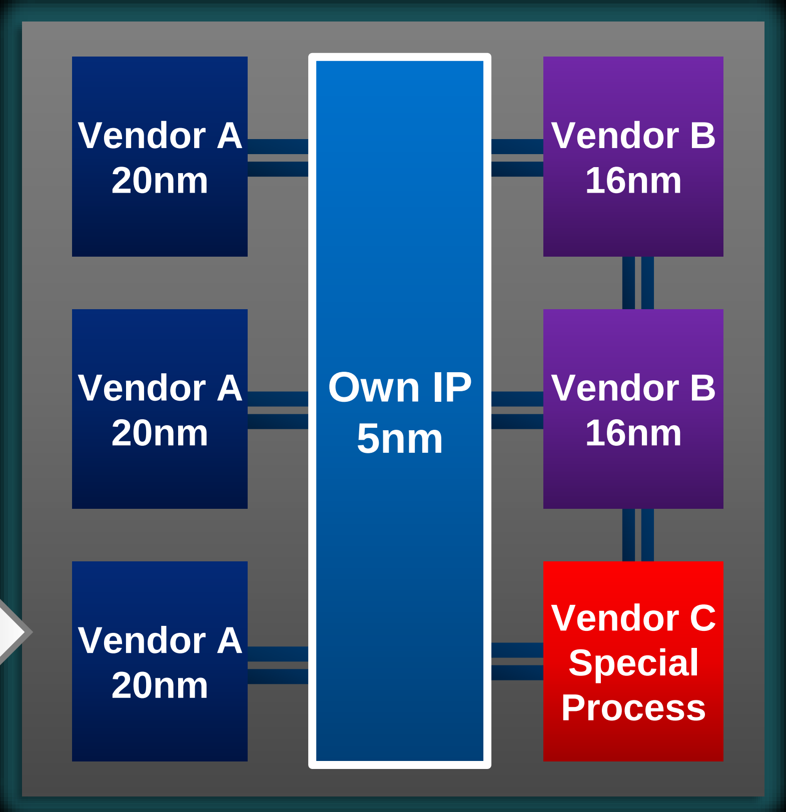


Single 20nm Process

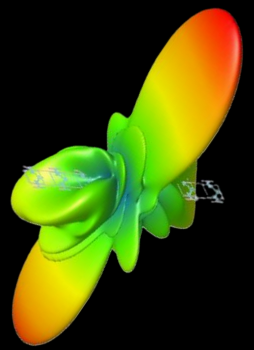
Chiplet System

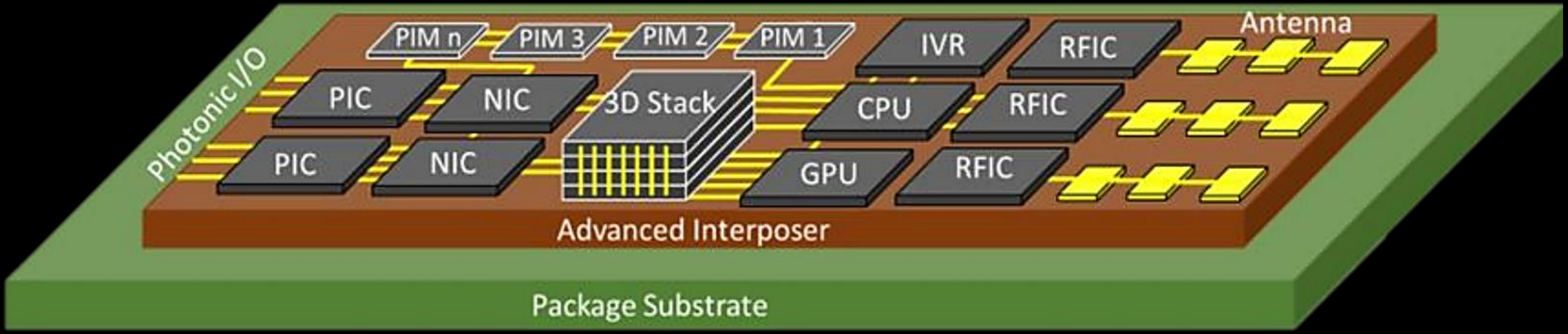


Multi-die SoC connected by Fast Interconnects



Multi-vendor, multiple process technologies
High-density fast interconnects





Source: Georgia Tech PRC Review 2022

1

Simulating for Interoperability

2

Testing for Interoperability

3

Managing Chiplet Data

Future Predictions

1 Simulating

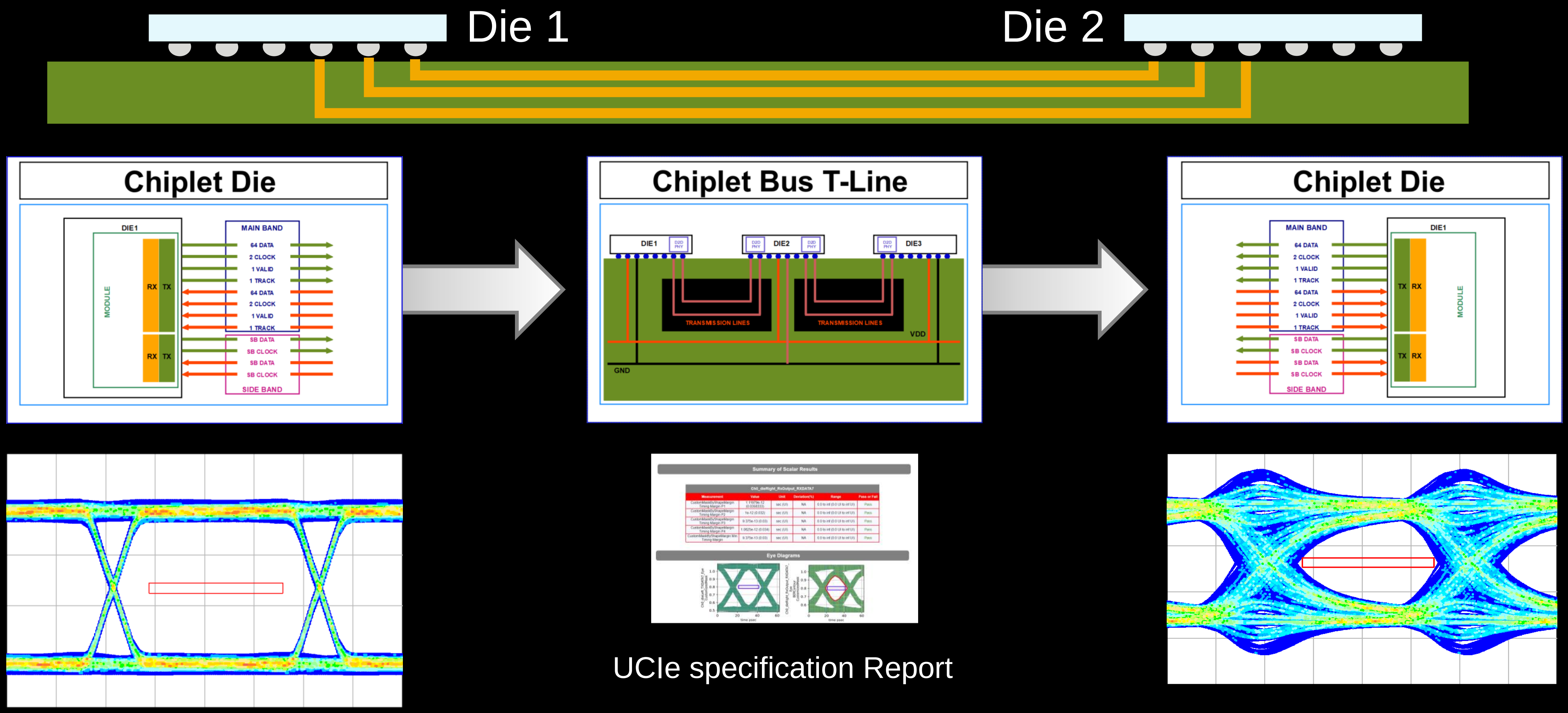
- Commercial PHY IP for UCIe Die-to-Die interconnects
- Standard and Advanced packages
- Tape-out a chiplet offering (Multi-standard IOs)

Why?

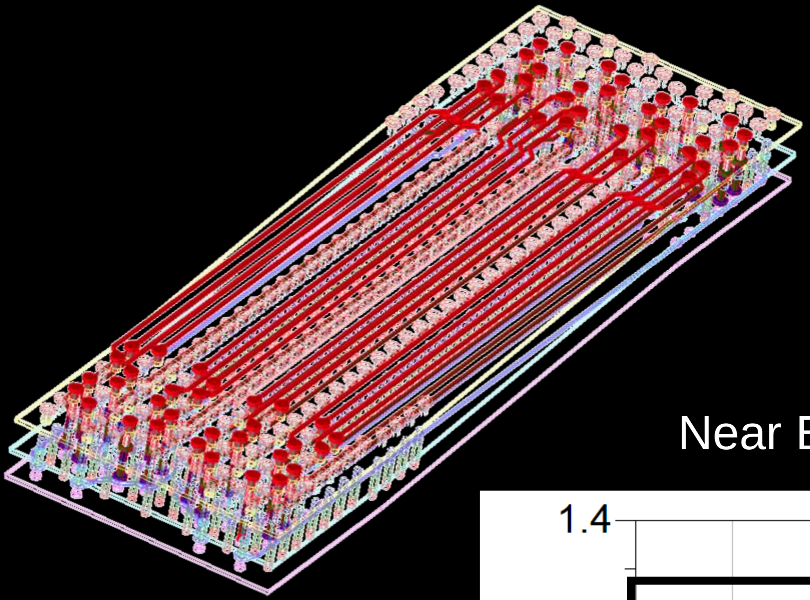
Alphawave Chiplets

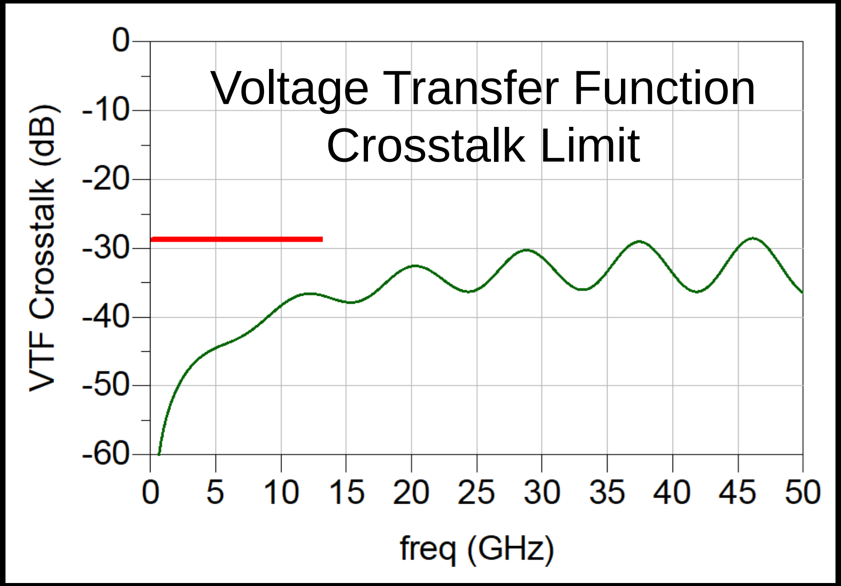
- ✓ Smaller, disaggregated SoCs
- ✓ Scalable architecture
- ✓ Reduced time-to-market
- ✓ Lower costs

1 Simulating

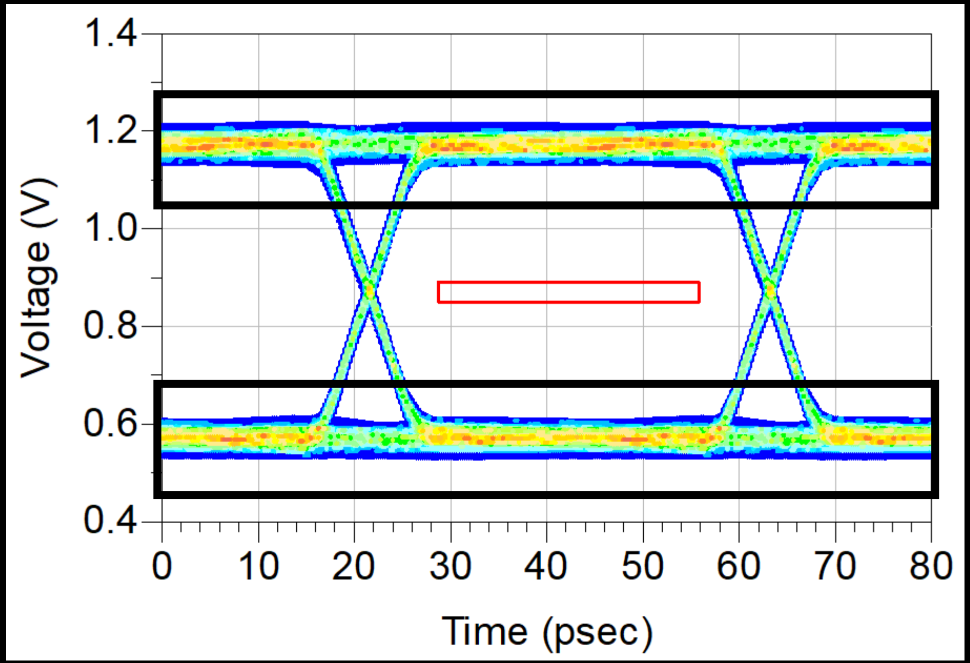


1 Simulating

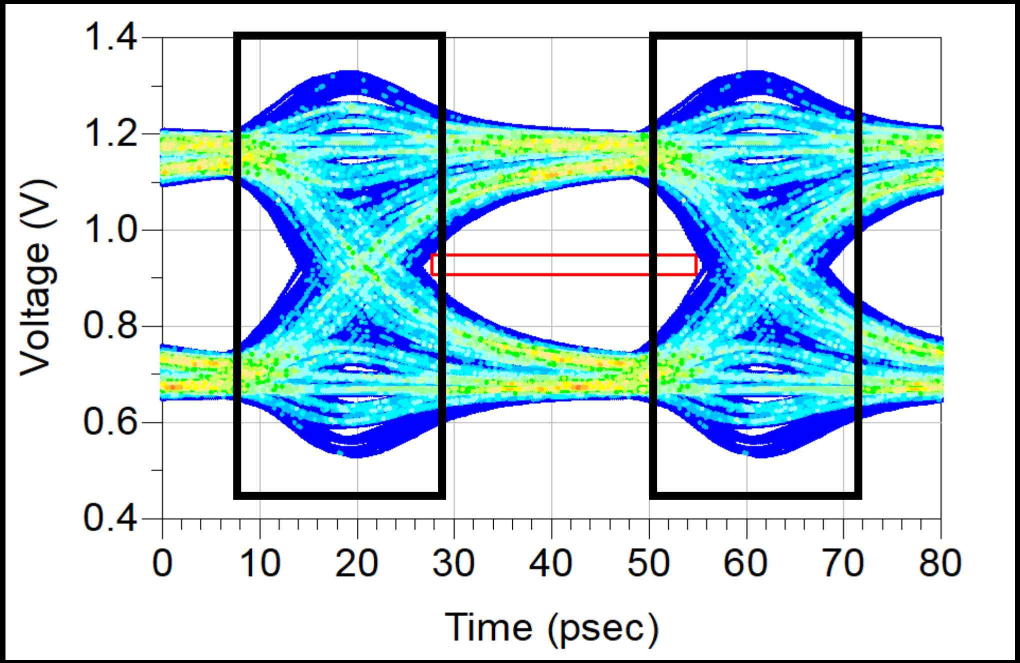




Near End Crosstalk Signature



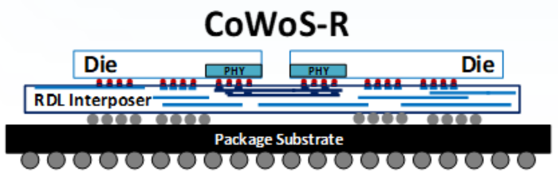
Far End Crosstalk Signature



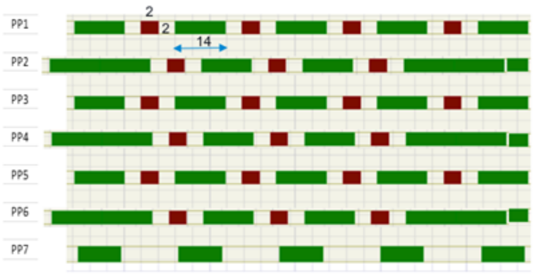
1 Simulating

ALPHAWAVE SEMI

CoWoS- R

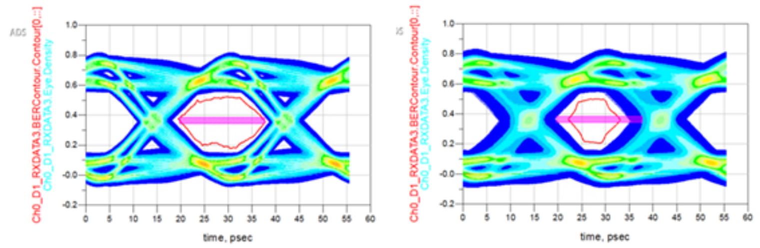


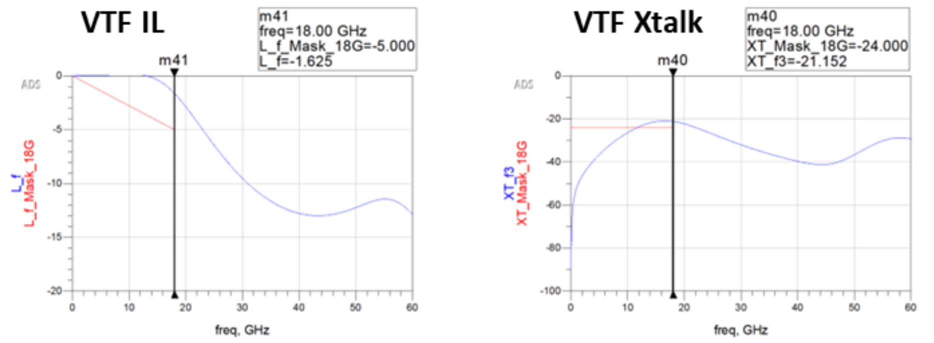
Advanced package cross-sections and example routing



Eye @RX uBump

Advanced packagelink performance at 36Gbps





UCIe Channel Specifications: Voltage transfer functions Insertions Loss (IL) and Crosstalk (X-talk)

Package Type	RX Term.	Pitch	Length
CoWoS-R or S	Open	45 um	1.5-2 mm

"…..Industry's First 64 Gbps UCIe IPs ….."
– Press Release, Dec 2024

Presented by Alphawave, DAC 2024

1

Simulating for Interoperability

2

Testing for Interoperability

3

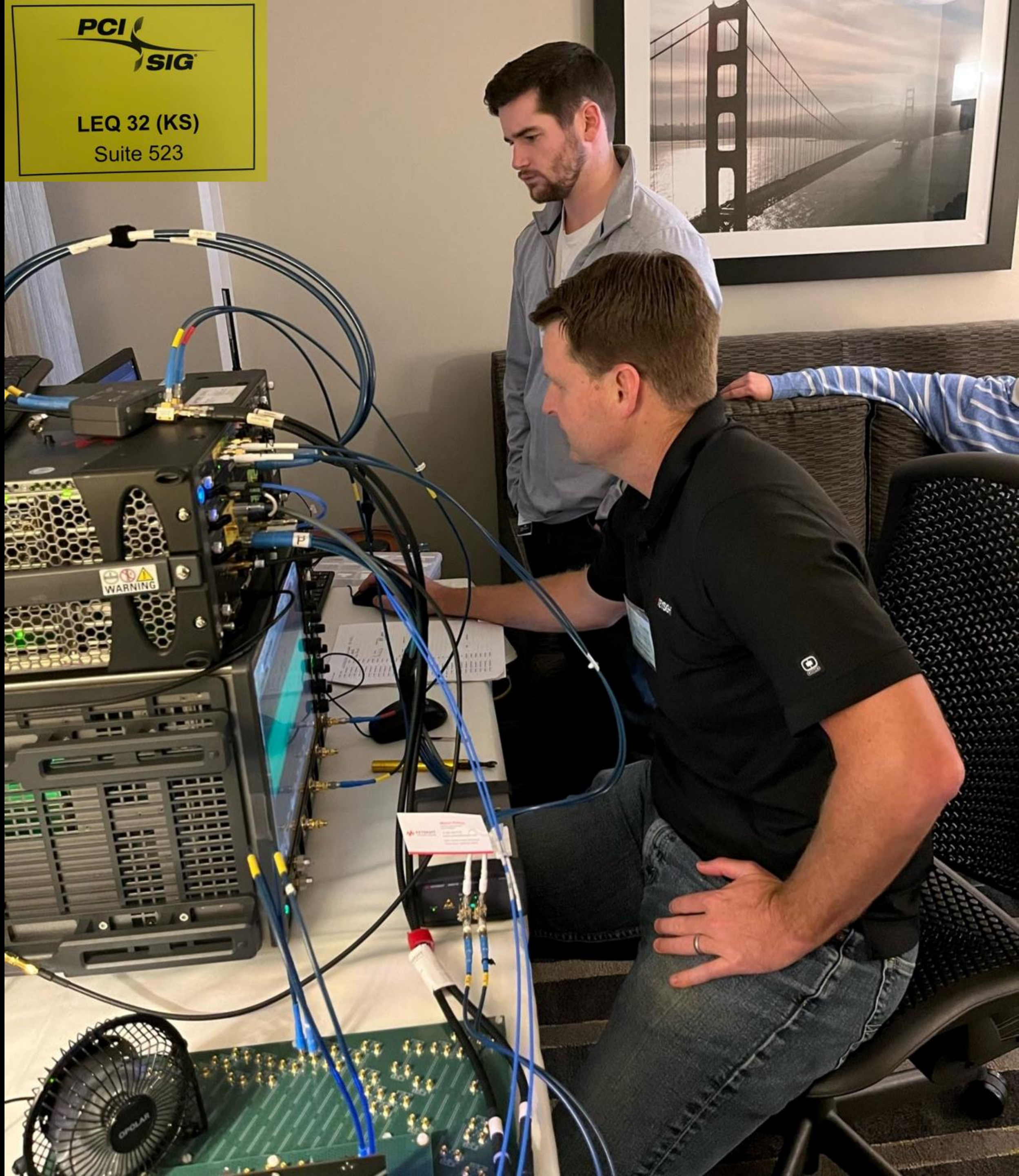
Managing Chiplet Data

Future Predictions

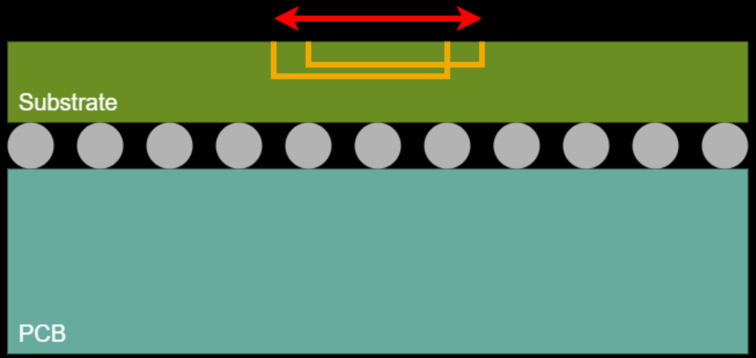
2 Testing

How do other digital standards ensure interoperability?

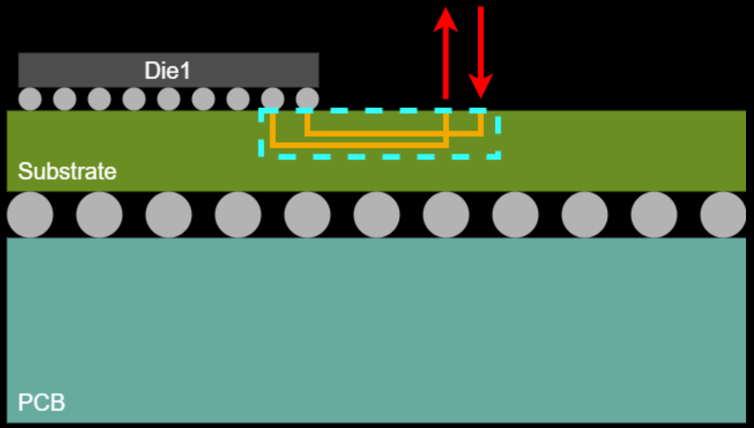
- Plugfests
- Standardized Compliance Tests



2 Testing



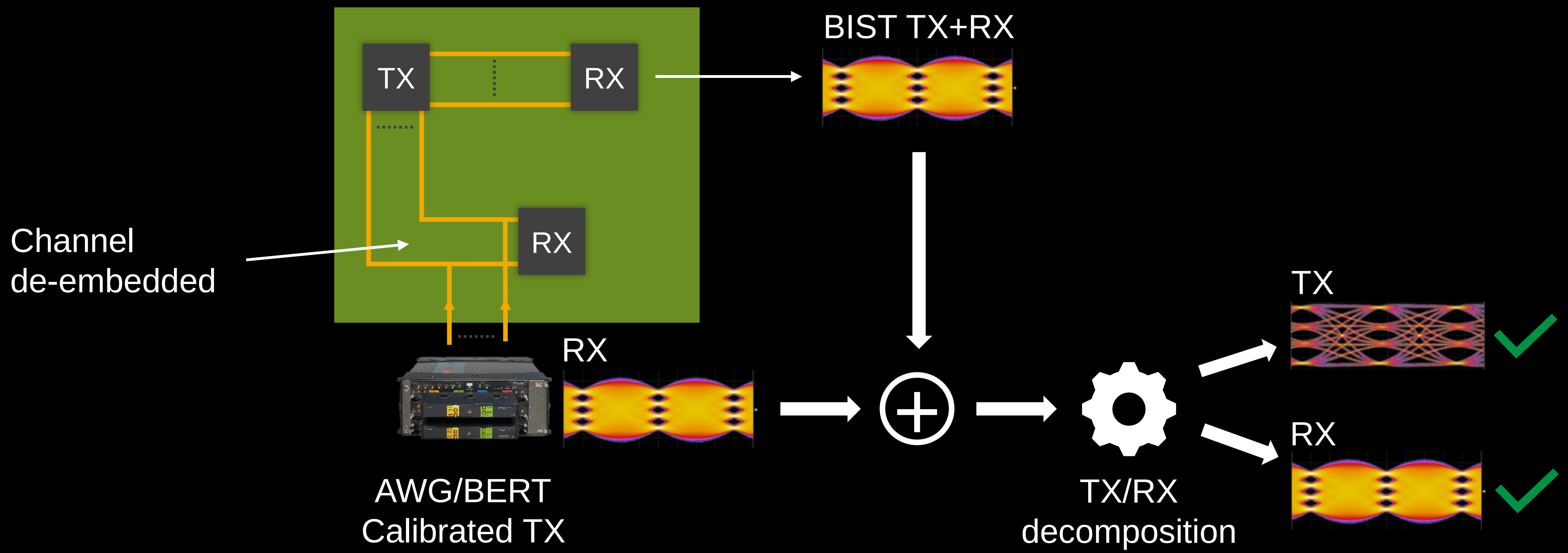
Channel Characterization
Vector Network Analysis
Wafer probing



Transmitter Test
Oscilloscope, De-embedded Channel
Wafer Probing

Receiver Test
BERT, injecting a UCIe Tx signal,
Calibrated against the Channel
Wafer Probing

2 Testing



TX
RX
RX
BIST TX+RX
Channel
de-embedded
RX
AWG/BERT
Calibrated TX
TX/RX
decomposition
TX
RX

1

Simulating for Interoperability

2

Testing for Interoperability

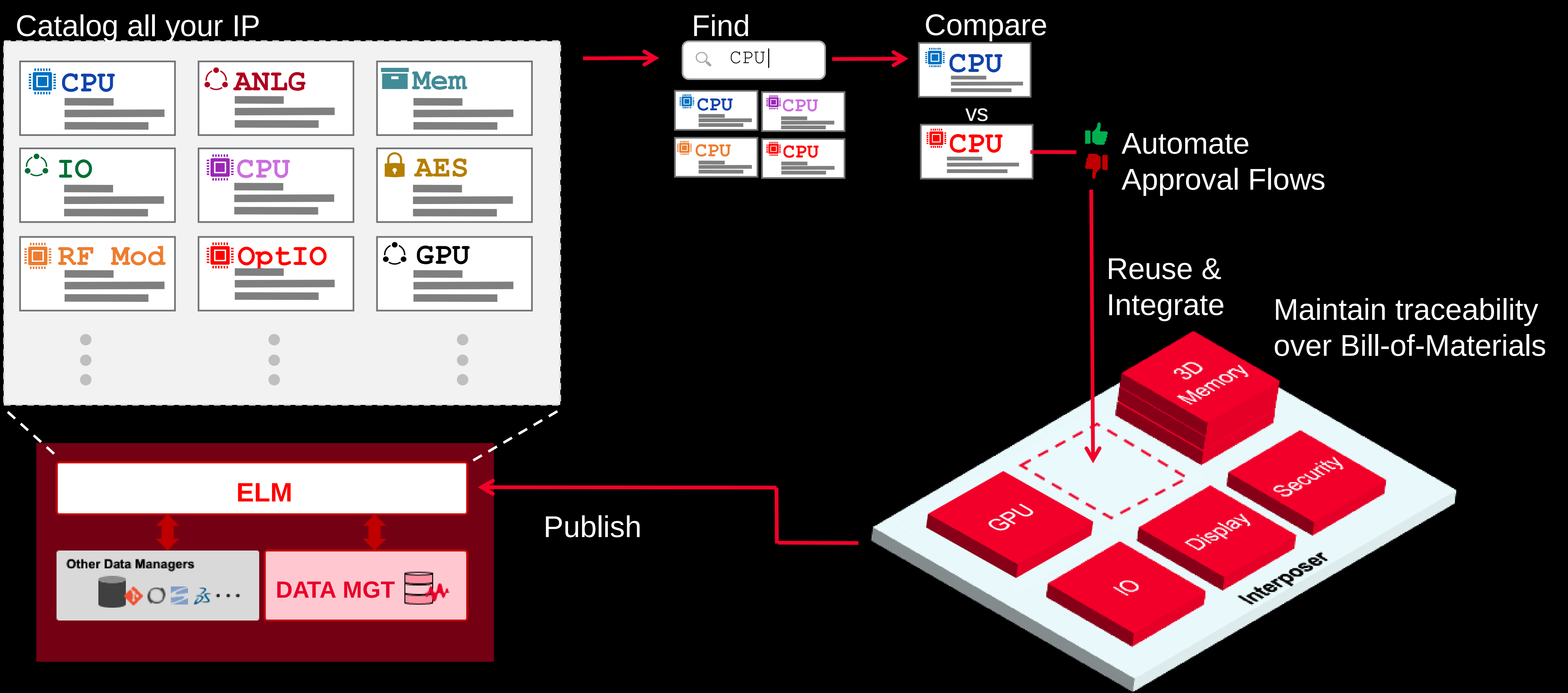
3

Managing Chiplet Data

Future Predictions

3 Data Management

Engineering Lifecycle Management (ELM) can oversee and fast-track your Chiplet lifecycle – slash time-to-market without compromising on compliance



KEYSIGHT

KEYNOTE BINGO

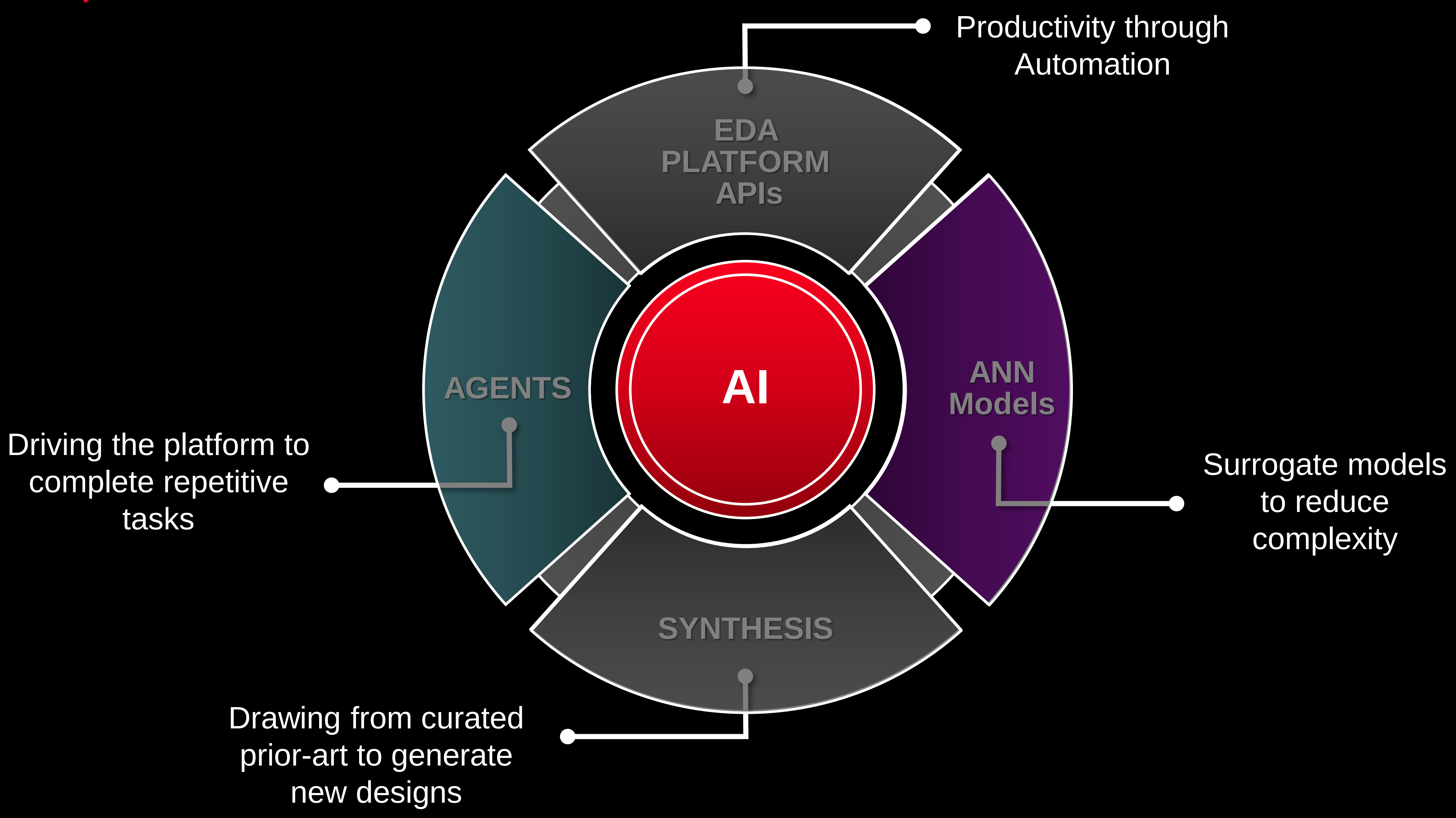
~~Moore’s Law~~	~~Scale~~	~~Disruptive~~
~~Risk~~	~~Power~~	~~Data~~

Future Predictions

Future of EDA in Chiplet Technologies

- **Heterogeneous Integration**: EDA tools will evolve to handle multi-die, multi-process chiplet systems, focusing on integration, power, and thermal management.
- **Advanced Physical Design**: Tools will optimize inter-chip connectivity, power distribution, and floorplanning for chiplet-based designs.
- **Standardized Interconnects**: EDA will support new high-bandwidth interconnect protocols and ensure compatibility across chiplet vendors.
- **System-Level Design**: Enhanced co-design and simulation tools will optimize both hardware and software for chiplet-based systems.
- **AI/ML Integration**: AI-driven tools will automate chiplet placement, design exploration, and performance optimization.
- **Design for Manufacturability (DFM)**: EDA will predict yield, manage process variations, and optimize designs for manufacturability.
- **Chiplet Ecosystem**: EDA tools will support modular chiplet integration and marketplaces, promoting flexible design and interoperability.

(From ChatGPT)



Productivity through Automation
EDA PLATFORM APIs
AGENTS
AI
ANN Models
Driving the platform to complete repetitive tasks
Surrogate models to reduce complexity
SYNTHESIS
Drawing from curated prior-art to generate new designs

KEYSIGHT

Thank you

Let's Partner!

nilesh_kamdar@keysight.com

Discuss with us at Booth #307